Signal Process. Renew. Energy., 2026; 10(1): 10-22

Signal Processing and Renewable Energy (SPRE)

https://doi.org/10.57647/spre.2026.1001.02

Research Article

A Low-Power CNTFET-Based Optical Communication Receiver for 40 Gbps Applications

Nazanin Zamani[1], Mehdi Amoon[1,2*], Zahra Alaie[1,2], Mahmoud Daneshvar Farzanegan[1,2]

[1] *Department Engineering, Na.C., Islamic Azad University, Najafabad, Iran*

[2] *Digital Processing and Machine Vision Research Center, Na.C., Islamic Azad University, Najafabad, Iran*

***Corresponding author:** m.amoon@iau.ac.ir

Article History:

Received:
10 October 2025

Revised:
01 December 2025

Accepted:
21 January 2026

Published in Issue:
31 March 2026

Abstract

This paper presents an optical receiver system for 40 Gbps communication applications in 32 nm carbon nanotube field-effect transistor (CNTFET) technology. The architecture consists of a modified regulated cascode (MRGC)-based transimpedance amplifier (TIA), followed by limiting amplifiers (LAs). The TIA is designed using the g_m/I_D methodology to optimize performance and power efficiency.

Simulation results indicate that the modified TIA achieves a transimpedance gain of 56.6 dBΩ, a −3 dB bandwidth of 28 GHz, an input-referred noise current of 14 pA/√Hz, and a power consumption of only 177 µW. The TIA is fully transistor-based and occupies a compact 2240 nm × 1216 nm chip area. The LA stage provides a voltage gain of 10.3 dB, a bandwidth of −3 dB at 32 GHz, and power consumption of 382 µW, in an area of 11.14 µm². The optical receiver system demonstrates a transimpedance gain of 86.9 dBΩ, a −3 dB bandwidth of 34.2 GHz, total power consumption of 1387 µW, and occupies a chip area of 48.40 µm². All simulations are performed at a supply voltage of ±0.45 V, with the photodiode and load capacitors set to 10 fF. The gain, bandwidth, and input-referred noise characteristics of the TIA are derived analytically and discussed using the g_m/I_D design methodology. Both analytical and simulation results confirm the suitability of the topology as a low-power optical receiver for next-generation communication systems.

Keywords: Optical Receiver; Transimpedance Amplifier; Low Power; CNTFET

Cite this article: Zamani, N., Amoon, M., Alaie, Z., & Daneshvar Farzanegan, M., A Low-Power CNTFET-Based Optical Communication Receiver for 40 Gbps Applications, *Signal Process. Renew. Energy. 10*(1) 10-22 (2026). https://doi.org/10.57647/spre.2026.1001.02

1. Introduction

The optical communication system, illustrated in Figure 1, comprises three primary components. In the transmitter section, a laser diode modulates the input electrical data onto an optical carrier. The modulated optical signal is then transmitted through an optical fiber to the receiver section, where a photodiode detects the incoming optical signal and converts it into a photocurrent [1]. This photocurrent is then converted to a voltage signal by a TIA and further amplified by an LA to levels suitable for digital processing [2].

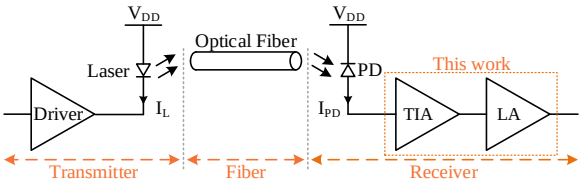

Figure 1. Block diagram of the optical communication system [2]

TIAs are critical components in optical receivers, with various architectural implementations, each offering different advantages and limitations. This article focuses on the design considerations and optimization of the TIA. Several circuit topologies have been proposed, including the following:

The inverter-based TIA provides high transconductance and low input impedance, but suffers from limited bandwidth [3]. The cascaded-inverter TIA provides improved gain, bandwidth, and noise performance compared to conventional inverter-based designs, though at the expense of significantly higher power consumption [4]. The fully differential TIA offers benefits such as common-mode noise rejection, improved linearity, high gain, and wide bandwidth; nevertheless, these advantages come at the expense of higher power dissipation [5].

The resistive-feedback TIA is known for its simplicity, ease of implementation, and low noise characteristics. Even though its high-frequency performance is limited by parasitic capacitance at the input node, and its stability can be a concern under certain conditions [6]. Similarly, the common-gate TIA provides design simplicity but is limited in bandwidth due to low input impedance and parasitic capacitance effects [2].

Among these, the RGC-based TIA offers several advantageous characteristics, including low input impedance, wide output voltage swing, and high output impedance, which have received considerable research attention [7]. In this work, the modified RGC-based TIA is employed as the core amplification stage. However, its bandwidth remains an important limitation.

The choice of an appropriate TIA architecture is primarily driven by application-specific requirements, including gain, bandwidth, noise performance, and power consumption. To ensure proper operation, the TIA bandwidth is typically designed to be approximately 70% of the target data rate [8]. To address the inherent bandwidth limitations, several enhancement techniques have been developed.

Stagger tuning improves the frequency response by incorporating passive inductors [9], while T-coil peaking employs coupled inductors to extend the bandwidth [10]. However, both techniques require a considerable area due to passive component integration. The Cherry–Hooper technique increases bandwidth through local feedback, but requires a high supply voltage for proper operation [2,11].

Moreover, the degeneration capacitor technique improves bandwidth by introducing a zero that shifts the output pole to higher frequencies [12]. Nevertheless, it comes at the cost of an increase in thermal noise due to the resistive components. The f_T doublers technique improves bandwidth by reducing the effective input capacitance, although it results in increased power consumption [13]. Similarly, the negative capacitance technique extends the bandwidth, but its effectiveness is constrained by practical limits on the sizing of feedback capacitors at the output node [14].

A particularly promising method is the active inductor technique, which synthesizes an inductive behavior at the output node. This approach resonates with the load capacitance to mitigate bandwidth limitations, providing a power-efficient solution without requiring additional power consumption [15]. Given the emphasis on low power consumption in this work, the active inductor approach is adopted to achieve the desired bandwidth enhancement.

Since the signals generated by TIAs generally exhibit low amplitude, an LA is employed to amplify these signals to levels suitable for subsequent digital processing. The gain of the LA must be sufficiently high to suppress noise contributions from preceding stages. Additionally, the bandwidth is a critical design parameter. When two LA stages with identical bandwidths are cascaded, the overall small-signal bandwidth is reduced. To mitigate this effect and maintain system performance, each LA stage is typically designed with a bandwidth of approximately 80% of the target data rate.

In addition to gain and bandwidth, the input-referred noise of the LA is another important design consideration, since LAs with wide bandwidths tend to introduce higher integrated noise. The total input-referred noise current of the cascaded TIA-LA system can be characterized by the noise bandwidths of the TIA and LA, denoted as (B_T) and (B_L), respectively, as expressed by: $\overline{I^2_{n.in.tot}} = \overline{I^2_{n.T}}B_T + \left(\overline{V^2_{n.L}}B_L/R^2_T\right)$ where, $I_{n.T}$ is the input-referred noise current of the TIA, $V_{n.L}$ is the input-referred noise voltage at the LA input, and R_T is the transimpedance gain of the TIA or LA. To minimize the second term in the total noise expression, it is essential to reduce $V_{n.L}$ as much as possible [2]. As electronic devices scale into the nanometer regime, conventional metal–oxide–semiconductor field-effect transistor (MOSFET) technology faces critical limitations. These challenges include significant short-channel effects, increased leakage currents, high electric field effects, lithographic constraints, and quantum confinement phenomena [16-18].

In contrast, CNTFETs have emerged as a promising alternative due to the exceptional electrical and structural properties of carbon nanotubes [19]. CNTFETs offer several advantages over traditional MOSFETs that position them as strong candidates for next-generation nanoelectronic applications. These advantages include: a high dielectric constant [20], superior gate electrostatic control [21], and symmetric, high carrier mobility in both

n-type and p-type devices [22,23].

In addition, CNTFETs exhibit ballistic transport without carrier scattering [24], high transconductance, high on/off current ratios [25], excellent thermal conductivity [26], and tunable threshold voltages [21]. Furthermore, the intrinsic electrical and thermal conductivities of CNTs contribute to improved performance at the device-level and circuit-level [27].

Despite these promising characteristics, CNTFET technology faces challenges; notably, fabrication complexity and sensitivity to structural defects in CNTs, which can negatively affect device reliability and manufacturing yield [28]. However, the structural and operational similarities between CNTFETs and conventional MOSFETs provide compatibility with existing CMOS fabrication processes. This compatibility allows the reuse of established MOSFET design methodologies, tools, and infrastructure, significantly lowering implementation barriers [29-31].

This paper is organized as follows: Section 2 describes the architecture and design methodology of the modified TIA, LA, and optical receiver topologies. The active inductor technique is introduced as a bandwidth enhancement strategy, and the input-referred noise of the modified TIA is analyzed through its equivalent noise circuit model. Section 3 details the g_m/I_D design methodology and demonstrates its application in optimizing the gain, bandwidth, and input-referred noise performance of the modified TIA. Analytical derivations and corresponding simulation results are provided to validate the approach. In Section 4, simulation results for the amplifiers and optical receiver are presented and compared with previously published designs operating at the 40 Gbps data rate. Section 5 concludes the paper.

2. Modified circuit architecture and design

2.1. Conventional RGC-based TIA topology

In TIA circuit design, the common-gate (CG) topology is widely used due to its inherently low input resistance, which allows for efficient current signal transfer from the photodetector to the amplifier while minimizing power dissipation across the source impedance [32]. As shown in Figure 2, incorporating a gain boosting stage—typically through a common-source (CS) amplifier—into the CG topology results in the RGC configuration. This structure further reduces the input impedance and increases the bandwidth of the amplifier.

Moreover, single-stage amplifiers offer advantages such as simplified design and the elimination of frequency compensation requirements [33].

The gain-boosting technique enhances the effective conductance of the transistor, thereby increasing the transconductance of the CG transistor by a factor proportional to the voltage gain of the CS amplifier, expressed as $(1 + A_{v.CS})$.

For the RGC-based TIA operating in the mid-band frequency range, the input impedance is defined by [7]:

$$R_{in} \approx \frac{r_{ds2}}{1 + g_{m2}\left(1 + g_{m4}(r_{ds4} \| r_{ds5})\right) r_{ds2}} \tag{1}$$

A comparison between the input impedance of the RGC amplifier and a conventional CG amplifier shows a significant reduction, approximately by a factor of $\left(1 + g_{m4}(r_{ds4} \| r_{ds5})\right)$. This reduction implies that the dominant pole of the amplifier is no longer located at the input node [34].

Based on the small-signal analysis of the conventional RGC structure, the low-frequency transimpedance gain is given by Eq. (2).

However, the RGC architecture introduces an operational constraint: the drain–source voltage of CNT1 must remain greater than or equal to the threshold voltage of CNT4 to ensure proper operation of the feedback loop. Additionally, because the input pole of the RGC amplifier typically resides in the low-frequency region [34], bandwidth enhancement techniques are often required to relocate the dominant pole to the output node. Assuming the output pole dominates, the −3 dB bandwidth can be approximated as:

$$\begin{aligned} f_{-3dB} &\cong \frac{1}{2\pi C_{out}} \times \frac{1}{R_{out}} = \\ &\frac{1}{2\pi\left(C_L + C_{dg3} + C_{db3} + C_{dg2} + C_{db2}\right)} \times \\ &\frac{1}{\left[g_{m2}\left(1 + g_{m4}(r_{ds4} \| r_{ds5})\right) r_{ds2} r_{ds1}\right] \| r_{ds3}} \\ &\xrightarrow{if\ r_{ds3} \ll g_{m2}\left(1 + g_{m4}(r_{ds4} \| r_{ds5})\right) r_{ds2} r_{ds1}} \\ &\approx \frac{1}{2\pi C_L r_{ds3}} \end{aligned} \tag{3}$$

where R_{out} and C_{out} are the effective output resistance and capacitance, respectively.

$$Z_T = \frac{V_{out}}{I_{PD}} = \frac{\left[\left(g_{m2} + \frac{1}{r_{ds2}}\right) + g_{m2} g_{m4}(r_{ds4} \| r_{ds5})\right]}{\left(\frac{1}{r_{ds2}} + \frac{1}{r_{ds3}}\right)\left[\left(g_{m2} g_{m4}(r_{ds4} \| r_{ds5})\right) + \left(g_{m2} + \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}}\right)\right] - \frac{1}{r_{ds2}}\left[\left(g_{m2} + \frac{1}{r_{ds2}}\right) + g_{m2} g_{m4}(r_{ds4} \| r_{ds5})\right]} \tag{2}$$

Furthermore, the input-referred noise current of the conventional RGC structure is given by:

$$\overline{I_{n.in}^2} = G_{in}^2 \times \overline{V_{n.in}^2} = \left(\frac{1}{R_{in}^2} + C_{in}^2\omega^2\right) \times 4KT\gamma \frac{(g_{m2}[g_{m4}(r_{ds4}\|r_{ds5}) + 1] + g_{m3})}{(g_{m2}[g_{m4}(r_{ds4}\|r_{ds5}) + 1])^2} \quad (4)$$

In Eq. (4), R_{in} is defined as in Eq. (1), and the total input capacitance, C_{in}, is given by the sum of $(C_{PD} + C_{dg1} + C_{db1} + C_{sg2} + C_{sb2})$.

2.2. Modified Transimpedance Amplifier

The MRGC-based TIA is illustrated in Figure 3, comprising transistors CNT1 through CNT5. This design incorporates a pass-transistor structure along anactive inductor technique to enhance bandwidth performance. In this configuration, CNT7 operates as a pass transistor to increase the gate voltage of CNT4, thus ensuring its proper operation. The active inductor is implemented using transistors CNT8 and CNT9, where CNT8 functions as a resistive element and provides the required bias voltage for CNT9. This active inductor is connected to the output node, forming a resonant network with the equivalent output capacitance. As a result, the overall −3 dB bandwidth of the circuit is effectively extended. To minimize power consumption, the TIA is a single-stage amplifier. Moreover, the use of active components contributes to reduced chip area.

The small-signal equivalent model and the frequency-dependent output impedance of the active inductor are depicted in Figure 4 [15].

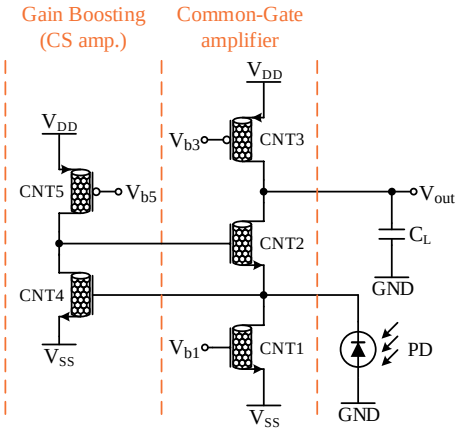

Figure 2. Conventional RGC-based TIA [33]

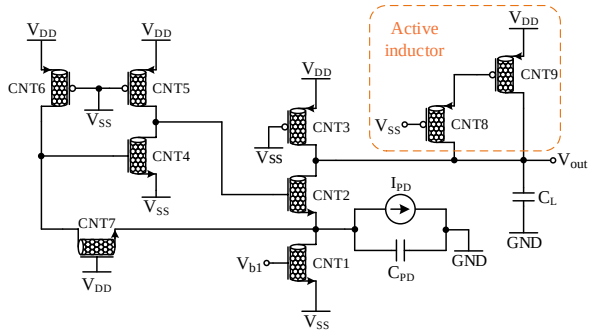

Figure 3. The MRGC-based TIA topology

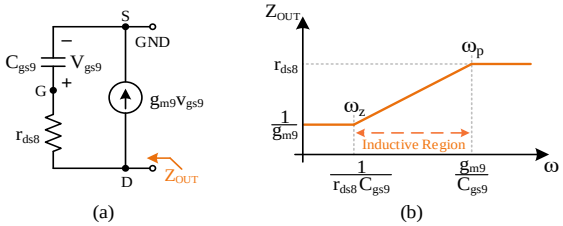

Figure 4. Active inductor implementation: (a) small-signal equivalent model, and (b) frequency-dependent output impedance [15]

The output impedance at the node indicated in Figure 4(a) is expressed as [15]:

$$Z_{OUT} = \frac{r_{ds8}\, C_{gs9}\, S + 1}{C_{gs9}\, S + g_{m9}} \quad (5)$$

The zero and pole introduced by the active inductor configuration are given by [15]:

$$\omega_z = -\frac{1}{r_{ds8}\, C_{gs9}} \quad (6)$$

$$\omega_p = -\frac{g_{m9}}{C_{gs9}} \quad (7)$$

At low frequencies, C_{gs9} exhibits high impedance and effectively behaves as an open circuit, causing CNT9 to operate in a diode-connected configuration. Under these conditions, the output impedance is approximately $Z_{OUT} \approx 1/g_{m9}$. At high frequencies, C_{gs9} provides a low-impedance path, effectively AC-grounding the gate of CNT9. As a result, the output impedance becomes dominated by $Z_{OUT} \approx r_{ds8}$. This frequency-dependent impedance behavior results in an active inductor whose impedance varies with frequency. When $1/g_{m9} < r_{ds8}$, i.e., the zero frequency ω_z is less than the pole frequency ω_p, the circuit exhibits inductive characteristics in the frequency range $\omega_z < \omega < \omega_p$, as shown in Figure 4(b). The equivalent inductance in this frequency region is given by [15]:

$$L_{eq} = \left(r_{ds8} - \frac{1}{g_{m9}}\right)\frac{C_{gs9}}{g_{m9}} \xrightarrow{if\ r_{ds8} \gg 1/g_{m9}} = \frac{r_{ds8}C_{gs9}}{g_{m9}} \quad (8)$$

The small-signal equivalent circuit of the modified TIA topology is presented in Figure 5.

By applying KCL at the output node, the input node, the gate node of CNT4, and the gate node of CNT2, respectively, the following equations are obtained:

$$g_{m9}V_{gs9} + \frac{V_{out} - V_{gs9}}{r_{ds8}} + \frac{V_{out}}{r_{ds3}} + g_{m2}\left(V_{g2} - V_{in}\right) + \frac{V_{out} - V_{in}}{r_{ds2}} = 0 \quad (9)$$

$$I_{PD} + \frac{V_{in}}{r_{ds1}} + \frac{V_{in}}{(1/g_{m7})} = g_{m2}V_{gs2} + \frac{V_{out} - V_{in}}{r_{ds2}} + g_{m7}V_{gs7} + \frac{V_{g4} - V_{in}}{r_{ds7}} \quad (10)$$

$$g_{m7}V_{gs7} + \frac{V_{g4} - V_{in}}{r_{ds7}} + \frac{V_{g4}}{r_{ds6}} = 0 \quad (11)$$

$$g_{m4}V_{gs4} + \frac{V_{g2}}{r_{ds4}} + \frac{V_{g2}}{r_{ds5}} = 0 \quad (12)$$

By expressing V_{g2}, V_{g4}, and V_{in} in terms of the output voltage using Equations (9), (11), and (12), and substituting them into the KCL expression at the input node, the output impedance gain of the modified topology can be derived as follows:

$$Z_T = \frac{\left[\left(g_{m2} + \frac{1}{r_{ds2}}\right) + g_{m2}g_{m4}\left(g_{m7} + \frac{1}{r_{ds7}}\right)(r_{ds4}\|r_{ds5})(r_{ds6}\|r_{ds7})\right]}{\left[\left(g_{m9} + \frac{1}{r_{ds2}} + \frac{1}{r_{ds3}}\right) \times \left(\left(g_{m2}g_{m4}\left(g_{m7} + \frac{1}{r_{ds7}}\right)(r_{ds4}\|r_{ds5})(r_{ds6}\|r_{ds7})\right) - \left(\frac{1}{r_{ds7}}\left(g_{m7} + \frac{1}{r_{ds7}}\right)(r_{ds6}\|r_{ds7})\right) + \left(g_{m2} + 2g_{m7} + \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + \frac{1}{r_{ds7}}\right)\right)\right] - \frac{1}{r_{ds2}}\left[\left(g_{m2} + \frac{1}{r_{ds2}}\right) + g_{m2}g_{m4}\left(g_{m7} + \frac{1}{r_{ds7}}\right)(r_{ds4}\|r_{ds5})(r_{ds6}\|r_{ds7})\right]} \quad (13)$$

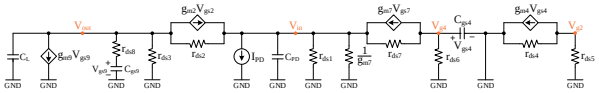

Figure 5. Small-signal equivalent circuit of the MRGC-based TIA topology

To facilitate comparison with the conventional TIA gain (Eq. (2)), Eq. (13) is rewritten as Eq. (14), where $(A) = \left(g_{m2} + \frac{1}{r_{ds2}}\right)$, $(B) = g_{m2}g_{m4}(r_{ds4}\|r_{ds5})$, and $(C) = \left(g_{m7} + \frac{1}{r_{ds7}}\right)(r_{ds6}\|r_{ds7})$.

If the coefficient $C > 1$ and the conditions $2g_{m7} + \frac{1}{r_{ds7}} \ll (A) + (B)(C) + \frac{1}{r_{ds1}}$ and $g_{m9} \ll \frac{1}{r_{ds2}} + \frac{1}{r_{ds3}}$ are satisfied, then the modified topology achieves a higher transimpedance gain than the conventional structure.

Furthermore, the gain can be further increased by increasing the transconductance of the driver transistor and the output resistors of the circuit. Under these design conditions—and assuming that r_{ds5} and r_{ds6} are relatively small—Eq. (13) simplifies to the following approximate form:

$$Gain = Z_T = \frac{V_{out}}{I_{PD}} \approx \frac{g_{m2}[1 + g_{m4}g_{m7}r_{ds5}r_{ds6}]}{g_{m9}\left[g_{m2}g_{m4}g_{m7}r_{ds5}r_{ds6} + g_{m2} + \frac{1}{r_{ds1}}\right]} \quad (15)$$

The frequency response of the modified topology is characterized by two poles and one zero. The input pole is given by:

$$\omega_{p.in} = -\frac{1}{R_{in}C_{in}} \quad (16)$$

where, R_{in} and C_{in} are the equivalent input resistance and capacitance, respectively, defined in Equations (17) and (18). Based on the previous assumptions, they are simplified to:

$$R_{in} = r_{ds1}\left\|\frac{1}{g_{m7}}\right\|\frac{r_{ds6} + r_{ds7}}{1 + g_{m7}r_{ds7}}\Bigg\| \frac{\left(\frac{1}{g_{m9}}\|r_{ds3}\right) + r_{ds2}}{1 + g_{m2}\left(1 + g_{m4}(r_{ds4}\|r_{ds5})\right)r_{ds2}} \approx \frac{1}{g_{m2}\left(1 + g_{m4}(r_{ds4}\|r_{ds5})\right)} \quad (17)$$

$$C_{in} = C_{PD} + C_{dg1} + C_{db1} + C_{sg2} + C_{sb2} + C_{sg7} + C_{sb7} \approx C_{PD} \quad (18)$$

The output pole, which acts as the dominant, is expressed as:

$$\omega_{p.out} = -\frac{1}{R_{out}C_{out}} \quad (19)$$

where R_{out} and C_{out} denote the equivalent resistance and capacitance at the output node, respectively, calculated and simplified as follows:

$$Z_T = \frac{(A)+(B)(C)}{\left[\left(g_{m9}+\frac{1}{r_{ds2}}+\frac{1}{r_{ds3}}\right)\left((A)+(B)(C)+\frac{1}{r_{ds1}}+2g_{m7}+\frac{1}{r_{ds7}}\right)\right]-\left[\frac{1}{r_{ds2}}\left((A)+(B)(C)\right)+\left(g_{m9}+\frac{1}{r_{ds2}}+\frac{1}{r_{ds3}}\right)\left(\frac{1}{r_{ds7}}(C)\right)\right]} \quad (14)$$

$$\begin{aligned} R_{out} = \; & \left[g_{m2}\left(1+g_{m4}(r_{ds4}\|r_{ds5})\right)r_{ds2}\right. \\ & \left.\times r_{ds1}\left\|\frac{1}{g_{m7}}\right\|\frac{r_{ds6}+r_{ds7}}{1+g_{m7}r_{ds7}}\right] \\ & \|r_{ds3}\|\frac{1}{g_{m9}} \approx \frac{1}{g_{m9}} \end{aligned} \quad (20)$$

$$\begin{aligned} C_{out} = \; & C_L + C_{dg9} + C_{db9} + C_{dg8} + C_{db8} \\ & + C_{dg3} + C_{db3} + C_{dg2} + C_{db2} \approx C_L \end{aligned} \quad (21)$$

Accordingly, the −3 dB bandwidth of the amplifier is given by $f_{-3dB} = \omega_{p.out}/2\pi$. Assuming the same effective load capacitance C_L for both conventional and modified topologies, the modified TIA achieves a higher bandwidth if $1/g_{m9} \ll r_{ds3}$, where r_{ds3} is the output resistance in the conventional structure.

A fundamental design consideration is the trade-off between gain and bandwidth. Specifically, increasing g_{m9} enhances the bandwidth but reduces the gain, and vice versa. To address this trade-off effectively, allocating more power to increase g_{m2}—the transconductance of the driver transistor—can improve gain, while bandwidth can be tuned by optimizing the design of transistors CNT8 and CNT9.

To evaluate the input-referred noise performance, the thermal noise equivalent circuit of the MRGC-based TIA is shown in Figure 6. The input-referred noise, is defined as the degree to which internally generated noise within the circuit mask the input signal, thereby setting the minimum detectable signal level for a given signal-to-noise ratio (SNR). As this parameter cannot be directly measured at the input, it is derived analytically using Eq. (22) [33].

$$\overline{I_{n.in}^2} = G_{in}^2\overline{V_{n.in}^2} \quad (22)$$

The output thermal noise voltage is given by $\overline{V_{n.out}^2} = \overline{I_{n.out}^2} \times |R_{out}|^2$, where $R_{out} = 1/g_{m9}$. The total output thermal noise current, is given by Eq. (23).

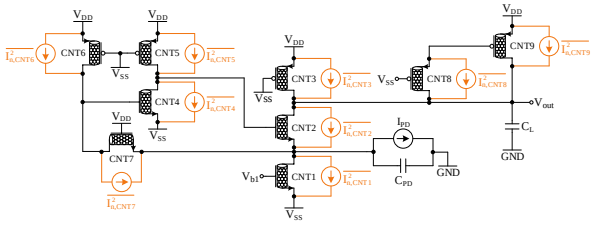

Figure 6. Thermal noise equivalent circuit of the MRGC-based TIA

$$\begin{aligned} \overline{I_{n.out}^2} = \; & \overline{I_{n.CNT2}^2} + \overline{I_{n.CNT3}^2} + \overline{I_{n.CNT8}^2} + \overline{I_{n.CNT9}^2} \\ = \; & 4KT\gamma g_{m2}\left(1+g_{m4}(r_{ds4}\|r_{ds5})\right) + \\ & 4KT\gamma g_{m3} + 4KT\gamma g_{m8} + 4KT\gamma g_{m9} \approx \\ & 4KT\gamma\left[g_{m2}\left(1+g_{m4}(r_{ds4}\|r_{ds5})\right)+g_{m9}\right] \end{aligned} \quad (23)$$

Therefore, the output thermal noise voltage contributions from both the driver and the load transistors, and can be expressed as:

$$\begin{aligned} & \overline{V_{n.out}^2} = \overline{I_{n.out}^2} \times |R_{out}|^2 = \\ & 4KT\gamma\left[g_{m2}\left(1+g_{m4}(r_{ds4}\|r_{ds5})\right)+g_{m9}\right]\frac{1}{g_{m9}^2} \end{aligned} \quad (24)$$

The input-referred thermal noise voltage is then calculated using $\overline{V_{n.in}^2} = \overline{V_{n.out}^2}/A_v^2$, where A_V denotes the voltage gain of the amplifier. For the modified topology, an approximate expression for A_V is given by:

$$\begin{aligned} |A_V| \; & = \frac{V_{out}}{V_{in}} = g_{m.Driver} \times R_{Load} \\ & \approx g_{m2}\left(1+g_{m4}(r_{ds4}\|r_{ds5})\right) \times \frac{1}{g_{m9}} \end{aligned} \quad (25)$$

Substituting into the following equation gives the input-referred noise voltage as [33]:

$$\begin{aligned} \overline{V_{n.in}^2} \; & = \frac{\overline{V_{n.out}^2}}{A_v^2} = 4KT\gamma \times \\ & \frac{\left[g_{m2}\left(1+g_{m4}(r_{ds4}\|r_{ds5})\right)+g_{m9}\right]}{\left[g_{m2}\left(1+g_{m4}(r_{ds4}\|r_{ds5})\right)\right]^2} \end{aligned} \quad (26)$$

Finally, the input-referred noise current is then obtained using:

$$\overline{I_{n.in}^2} = G_{in}^2 \overline{V_{n.in}^2} = \left(\frac{1}{R_{in}^2} + C_{in}^2 \omega^2\right) \overline{V_{n.in}^2} \quad (27)$$

To assess the improvement in noise performance, the input-referred noise current of the modified topology (Eq. 28) is compared to that of the conventional design (Eq. 4). Assuming identical effective input capacitance C_{PD} and that $g_{m3} \approx g_{m9}$, a significant noise reduction is observed. Notably, the input resistance of the modified amplifier is $1/g_{m9} \| r_{ds3}$ higher than that of the conventional architecture. This increased input resistance leads to a reduction of the conductance term G_{in}^2 within the input-referred noise current expression, thereby effectively lowering the overall input-referred noise.

2.3. Limiting Amplifier Stage

To achieve the required gain in the optical receiver system, three conventional LA stages are cascaded, as illustrated in Figure 7, which presents both the block diagram and the circuit-level implementation.

Each LA stage utilizes a conventional differential amplifier topology incorporating active inductor loads, as shown in Figure 7(b). At low frequencies, the voltage gain of each LA stage can be approximated by:

$$A_V = \frac{V_{out}}{V_{in}} = -g_{m1} \times \left(r_{ds1} \| \frac{1}{g_{m3}}\right) \quad (28)$$

1.1 Optical Receiver System

The architecture of the optical receiver is depicted in Figure 8. It consists of two TIAs based on the MRGC topology, followed by three cascaded LA stages. The two MRGC-based TIA blocks employ a fully differential configuration to suppress common-mode noise, thereby reducing the overall noise of the optical receiver system. This design approach is widely recognized as an architecture for low-noise optical receivers [2].

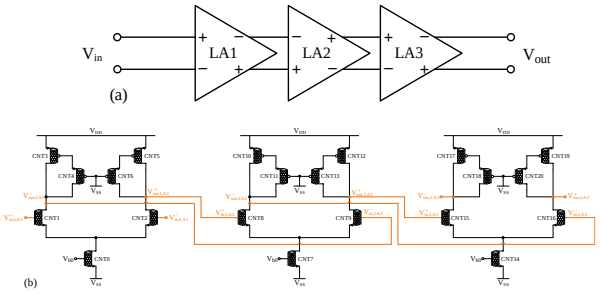

Figure 7. (a) Block diagram and (b) circuit-level implementation of the three-stage cascaded limiting amplifier

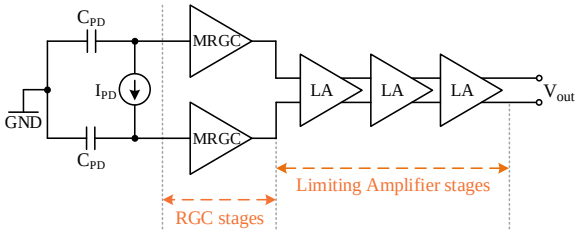

Figure 8. Block diagram of the low-noise optical receiver system employing the MRGC-based TIA followed by three cascaded LA stages [2]

3. g_m/I_D Design Methodology

The g_m/I_D design methodology is a well-established and widely adopted approach in analog integrated circuit design. In this technique, the ratio of the transistor's transconductance (g_m) to its drain current (I_D) is employed as a key design parameter to optimize performance characteristics, particularly in amplifier design [35]. This methodology provides several advantages, including: (1) reducing the number of design variables, (2) enabling systematic performance optimization, and (3) effectively balancing trade-offs between circuit performance and power consumption [36]. While extensively validated in analog MOSFET-based designs, this methodology presents distinct challenges when applied to CNTFET technologies. Unlike conventional MOSFETs, which support continuous scaling of the channel width, CNTFETs exhibit quantized width characteristics determined by the number of nanotubes, the spacing between nanotubes, and the diameter of the nanotubes [37].

Figure 9 presents the proposed g_m/I_D-based design flowchart for the modified TIA, outlining the methodology used to achieve the target performance metrics, including gain, bandwidth, and input-referred noise.

The design process begins by selecting appropriate g_m/I_D ratio and drain current values for each CNTFET according to its pre-defined role and the design constraints listed in Table 1. These parameters are substituted into analytical expressions for gain, bandwidth, and input-referred noise, all of which are formulated within the g_m/I_D framework. This design loop is iteratively executed until the required performance specifications are achieved.

After the design objectives are met, the bias voltages and number of nanotubes for each CNTFET are determined based on the required conductivity and current. The complete circuit is then simulated, and key performance metrics—including transistor operating regions, inductive peaking behavior, eye diagram characteristics, and total power consumption—are evaluated. If any metric deviates from the acceptable limits, the design parameters are

revised accordingly, and the process is repeated. Finalization occurs when the simulated results align with the established design targets.

The transimpedance gain, bandwidth, and input-referred noise of the MRGC-based TIA are reformulated using the g_m/I_D design methodology, as expressed in Equations (29)–(31):

$$Gain = \frac{I_{D2}\left[\frac{g_m}{I_D}\right]_2\left[1+A\left[\frac{g_m}{I_D}\right]_4\left[\frac{g_m}{I_D}\right]_7\right]}{I_{D9}\left[\frac{g_m}{I_D}\right]_9} \times \frac{1}{\left[AI_{D2}\left[\frac{g_m}{I_D}\right]_2\left[\frac{g_m}{I_D}\right]_4\left[\frac{g_m}{I_D}\right]_7 + I_{D2}\left[\frac{g_m}{I_D}\right]_2 + BI_{D1}\right]} \quad (29)$$

Where $A = 1/\lambda_5\lambda_6$, $B = \lambda_1$, and $\lambda = 1/r_{ds}I_D$.

$$f_{-3dB} = \frac{1}{2\pi C_L} \times \left[\frac{g_m}{I_D}\right]_9 I_{D9} \quad (30)$$

The input-referred noise at low-frequency (i.e., as s→0) is given by:

$$\overline{I_{n.in}^2} = 4KT\gamma \times \left[\left[\frac{g_m}{I_D}\right]_2 I_{D2}\left(1+\left[\frac{g_m}{I_D}\right]_4 C\right) + \left[\frac{g_m}{I_D}\right]_9 I_{D9}\right] \quad (31)$$

where $C = 1/\lambda_5$.

Table 1. Required and simulated g_m/I_D values for transistors in the MRGC-based TIA

	Required value	Simulated ($\mho/A$)
$[g_m/I_D]_1$	[3-9]	6.55
$[g_m/I_D]_2$	[3-9]	7.62
$[g_m/I_D]_3$	[0.05-3]	0.53
$[g_m/I_D]_4$	[3-6]	4.24
$[g_m/I_D]_5$	[0.05-3]	0.07
$[g_m/I_D]_6$	[0.05-3]	0.18
$[g_m/I_D]_7$	[3-6]	3.59
$[g_m/I_D]_8$	[500-700k]	677k
$[g_m/I_D]_9$	[6-9]	8.13

Table 2. Comparison of required specifications, simulation results, and g_m/I_D design parameters for the MRGC-based TIA

	A_V (dBΩ)	f_{-3dB} (GHz)	IRN $(A/\sqrt{Hz})$
Required value	> 50	≈ 28	< 20 p
Simulated (TIA)	56.6	28.0	14 p
g_m/I_D methodology	56.47	20.6	8 p

Table 1 summarizes the required parameter ranges and simulation results for each transistor in the MRGC-based TIA, obtained using the g_m/I_D design methodology.

Table 2 presents a comparison of the required specifications, simulation results, and corresponding g_m/I_D design parameters. The simulation results demonstrate excellent agreement with the required specifications and the analytical equations using the g_m/I_D methodology. The bandwidth deviation observed is attributed to the low-frequency approximation used in the analytical bandwidth expression.

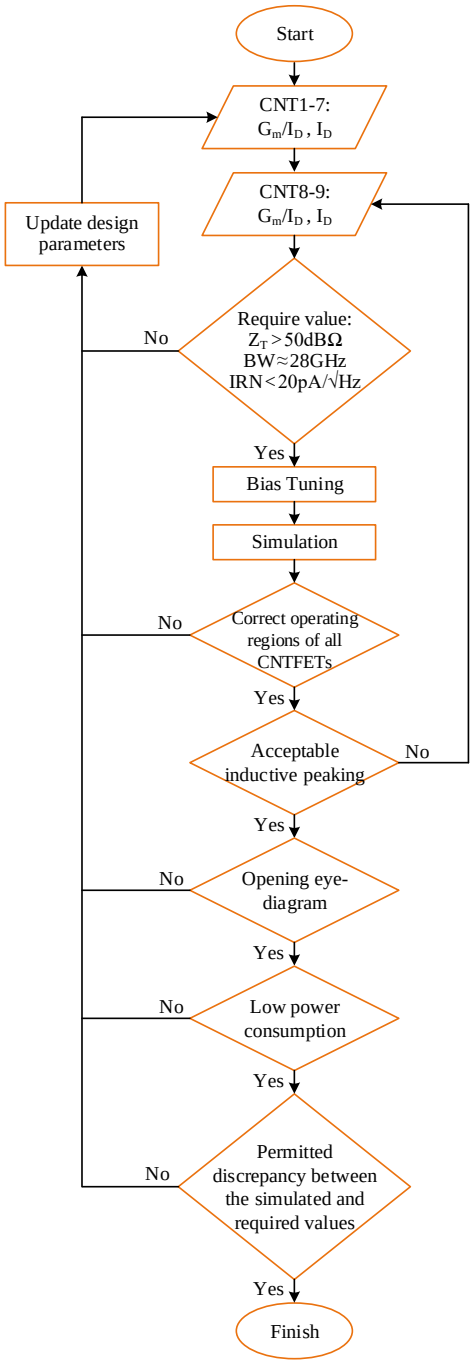

Figure 9. Proposed g_m/I_D-based design methodology

4. Simulation Results and Layout Implementation

4.1. The Modified TIA

The simulated frequency response of the MRGC-based TIA is illustrated in Figure 10. The amplifier achieves a transimpedance gain of 56.6 dBΩ and a −3 dB bandwidth of 28.0 GHz, with a power consumption of 177 µW. These performance levels are achieved using an active inductor technique, which enhances high-frequency operation without significantly increasing power consumption.

Figure 11 illustrates the input-referred and output noise characteristics of the modified TIA. As shown in Figure 11(a), the input-referred noise is approximately 14 pA/√Hz at low frequencies and increases to 24 pA/√Hz at the −3 dB bandwidth. These results represent a 27% improvement over the best previously reported value and a 70% improvement relative to the worst reported value in Table 5.

To evaluate signal integrity, eye diagram simulations were performed using a 27–1 NRZ PRBS at 40 Gbps. The input current amplitudes were set to 10 µA and 50 µA, with rise/fall times of 1 ps. As illustrated in Figure 12, for an input current of 10 µA, the vertical eye opening (ISI) is 6.91 mV, and the horizontal eye opening (jitter) is 22.76 ps. For a 50 µA input, the ISI increases to 36.48 mV, while the jitter remains nearly constant at 22.95 ps. These results confirm that the modified TIA maintains a wide and clearly defined eye opening under varying signal conditions.

Monte Carlo simulations were conducted to analyze the effect of the threshold voltage (V_{th}) variation in the amplifier's performance. The V_{th} of each transistor was modeled as a gate-connected voltage source with a Gaussian distribution of ±5% around its nominal value [37]. A total of 200 simulations were performed. Figure 13 presents the resulting variations in gain and bandwidth, including the frequency responses and corresponding histograms.

The layout of the modified TIA was implemented using CNTs with a chirality of (19,0), corresponding to a diameter of approximately 1.5 nm. The center-to-center distance between adjacent CNTs is 20 nm, and the edge distance of 10 nm beyond the outermost tubes. The effective gate width is defined as: $W_{gate} = [N \times (20nm + 1{,}5nm)]$, where N is the number of CNTs per device. Assuming a gate length of 32 nm and a feature size of λ = 16 nm, the normalized channel length becomes: $L(\lambda - based) = 32nm/16nm = 2$. The number of CNTs and the λ-based gate widths for each transistor are listed in Table 3.

The layout occupies an area of 140λ × 76λ, equivalent to 2240 nm × 1216 nm, as shown in Figure 14.

4.2. The LA Stage

Simulation results for the LA stage employing inductive loads show a voltage gain of 10.3 dB and a −3 dB bandwidth of 32.0 GHz, with a total power consumption of 382 µW. The frequency response is depicted in Figure 15.

Each transistor in the LA stage is implemented with a normalized channel length of 2λ. The number of CNTs and corresponding gate widths in λ-based are detailed in Table 4.

The LA layout occupies an area 573λ×76λ, which is equal to 9168 nm × 1216 nm, as illustrated in Figure 16.

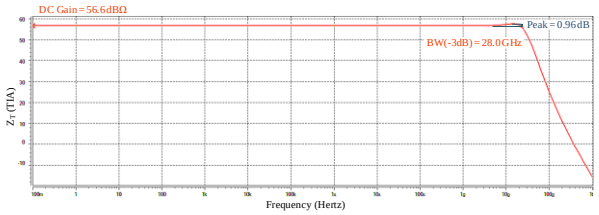

Figure 10. Simulated frequency response of the MRGC-based TIA

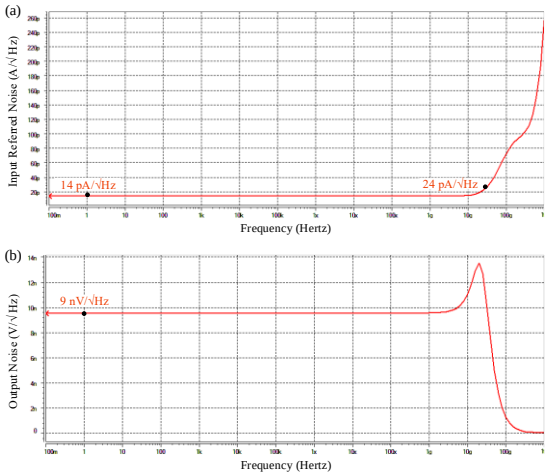

Figure 11. (a) Input-referred noise and (b) output noise of the MRGC-based TIA

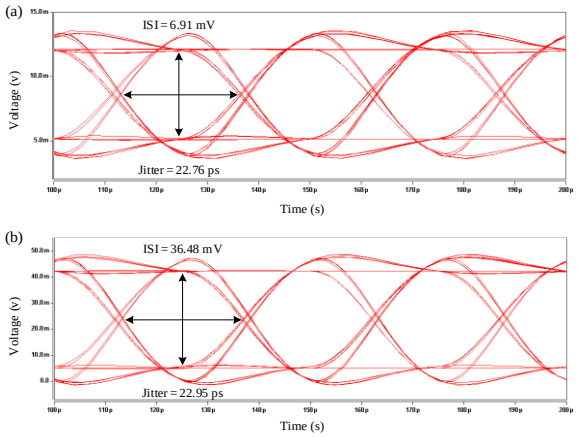

Figure 12. Eye diagrams of the MRGC-based TIA for (a) 10 µA and (b) 50 µA input currents

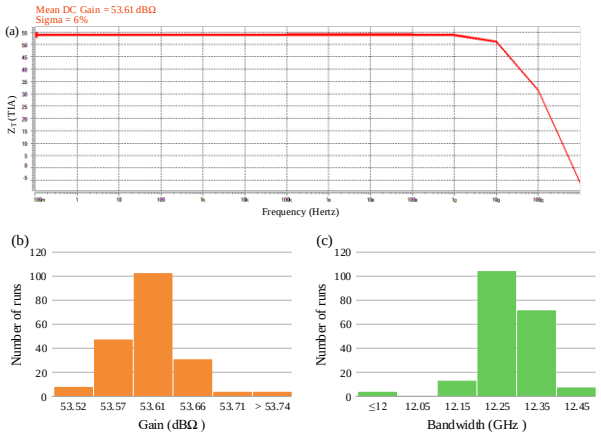

Figure 13. Monte Carlo simulation results: (a) frequency response, and histograms of (b) gain and (c) bandwidth under ±5% V_{th} variation for the MRGC-based TIA

4.3. The Optical Receiver System

The 40 Gbps low-noise optical receiver system achieves a transimpedance gain of 86.9 dBΩ and a −3 dB bandwidth of 34.2 GHz. The total power consumption is 1387 µW, and the input-referred noise current is 10.31 pA/√Hz. The frequency response is shown in Figure 17.

The layout of the optical receiver occupies an area of 9760 nm × 4960 nm, as illustrated in Figure 18.

4.4. 40 Gbps Performance Comparison

A comparative analysis of the simulated performance for the MRGC-based TIA, LA, and optical receiver (OR) against previously reported 40 Gbps designs is presented in Table 5.

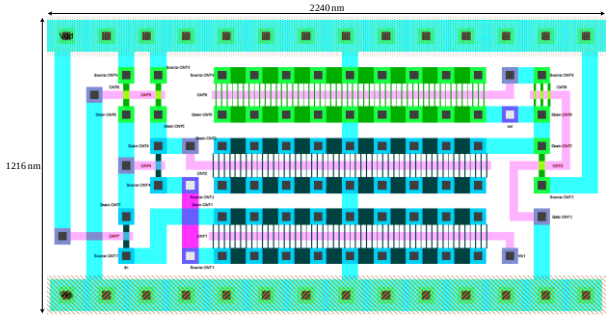

Figure 14. Layout of the MRGC-based TIA

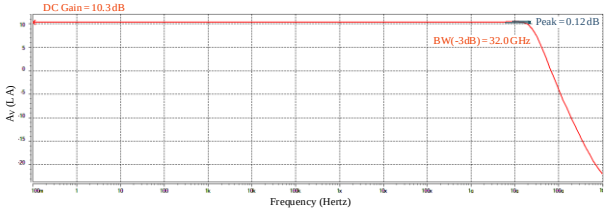

Figure 15. Frequency response of the LA with inductive loads

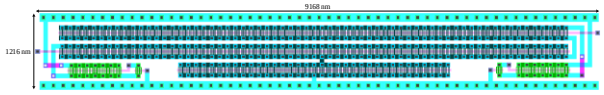

Figure 16. Layout of the LA

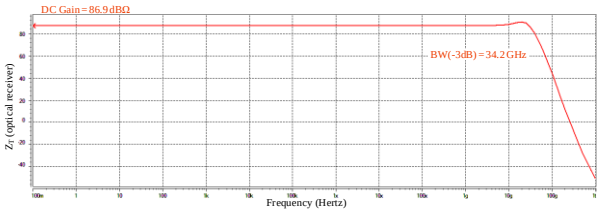

Figure 17. Frequency response of the 40 Gbps low-noise optical receiver system

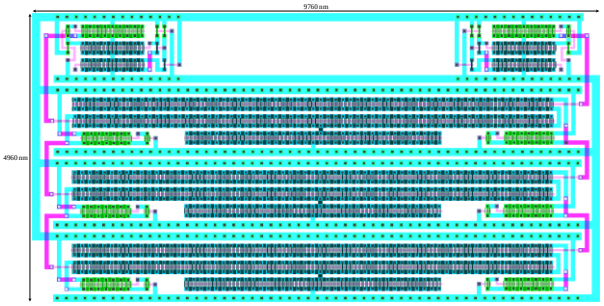

Figure 18. Layout of the low-noise optical receiver system

Table 3. Number of CNTs and λ-based gate widths for transistors in the MRGC-based TIA

	N	W(λ-based)
CNT1	51	68.53
CNT2	51	68.53
CNT3	1	1.34
CNT4	1	1.34
CNT5	1	1.34
CNT6	1	1.34
CNT7	1	1.34
CNT8	3	4.03
CNT9	50	7.18

Table 4. Number of CNTs and λ-based gate widths for transistors in the LA

	N	W(λ-based)
CNT0	205	275.46
CNT1	385	517.34
CNT2	385	517.34
CNT3	40	53.75
CNT4	4	5.375
CNT5	40	53.75
CNT6	4	5.375

Table 5. Performance comparison of the MRGC-based TIA, LA, and optical receiver system with previously reported 40 Gbps designs

	This work	[38]	[39]	[40]	[41]	[42]	[43]	[44]	[45]	[46]
Year	2025	2010	2010	2012	2012	2015	2015	2017	2021	2022
Process Technology	32 nm CNTFET	0.13 µm MOSFET	65 nm MOSFET	45 nm SOICMOS	65 nm MOSFET	65 nm MOSFET	0.13 µm BiCMOS	0.13 µm BiCMOS	0.18 µm BiCMOS	90 nm MOSFET
Supply voltage	0.9 V	1.5 V	1.2 V	1 V	1.2 V	1.2 V	2.3 V	2.3 V	3.3 V	1 V
Data rate Optical Receiver (OR)	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps	40 Gbps
Gain (TIA)	56.6 dBΩ	50 dBΩ	46.7 dBΩ	55 dBΩ	54 dB	50 dBΩ	13 dB	—	39.4 dBΩ	40 dBΩ
Bandwidth (TIA)	28.0 GHz	29 GHz	21.6 GHz	30 GHz	25 GHz	33.1 GHz	43 GHz	—	32.9 GHz	25.8 GHz
Power consumption (TIA)	177 µW	45.7 mW	39.9 mW	9 mW	—	—	8.5 mW	—	77 mW	29 mW
Input referred noise TIA (pA/√Hz)	14	51.8	30	20.47	—	—	20	—	37	25
Area (TIA)	2.72 µm²	0.4 mm²	7.5 mm²	0.29 mm²	—	—	—	—	0.45 mm²	0.16 mm²
FOM1 (TIA)	639.54	0.6125	4.100	8.95	—	—	—	—	0.4549	1.42
FOM2 (TIA)	6395.48	61.25	820.09	985.18	—	—	—	—	—	—
Gain (LA)	10.3 dB	—	—	—	10 dB	—	7 dB	7 dB	—	—
Bandwidth (LA)	32 GHz	—	—	—	52.8 GHz	—	—	—	—	—
Power consumption (LA)	382 µW	—	—	—	—	—	6.5 mW	6.5 mW	—	—
Area (LA)	11.14µm²	—	—	—	—	—	—	—	—	—
Gain (OR)	86.9 dBΩ	—	—	—	92 dBΩ	79 dBΩ	89.5 dBΩ	80 dBΩ	—	—
Bandwidth (OR)	34.2 GHz	—	—	—	35 GHz	29.6 GHz	—	—	—	—
Power consumption (OR)	1387 µW	—	—	—	168 mW	12.4 mW	77 mW	77 mW	—	—
Input referred noise OR (pA/√Hz)	10.31	—	—	—	14	53.47	—	—	—	—
Area (OR)	48.40 µm²	—	—	—	0.825 mm²	—	0.52 mm²	0.52 mm²	—	—
FOM1 (OR)	207.83	—	—	—	6.10 µ	3.5268	—	—	—	—
FOM2 (OR)	2078.31	—	—	—	36.24 µ	352.68	—	—	—	—
C_{PD}	10 fF	50 fF	200 fF	80 fF	60 fF	100 fF	17 fF	17 fF	—	—
Load	10 fF	—	50 Ω	50 Ω	—	—	—	50 Ω	50 Ω	50 Ω

Two figures of merit (FoMs) are used to quantitatively assess the performance improvements:

$$FOM1 = \frac{Gain\ (dB\Omega) \times BW\ (GHz)}{P_{diss}\ (mW) \times IRN\ \left(pA/\sqrt{Hz}\right)} \tag{32}$$

$$FOM2 = \frac{Gain\ (dB\Omega) \times BW\ (GHz) \times C_{PD}\ (fF)}{P_{diss}\ (mW) \times IRN\ \left(pA/\sqrt{Hz}\right)} \tag{33}$$

Both FoMs confirm the superior performance of the MRGC-based TIA and low-noise optical receiver in compared to existing state-of-the-art designs. These improvements are mainly attributed to an optimized circuit design, reduced supply voltage, and the high-efficiency ballistic transport properties of the CNTFET technology.

5. Conclusion

This paper presents the design and simulation of a 40 Gbps optical receiver implemented in 32 nm CNTFET technology. The receiver consists of two identical MRGC-based TIAs, followed by three cascaded differential LA stages. The active inductor technique is employed in both amplifier types to enhance high-frequency performance. All circuits operate with a ±0.45V supply. The modified TIA achieves a transimpedance gain of 56.6 dBΩ, a −3 dB bandwidth of 28 GHz, an input-referred noise current of 14 pA/√Hz, and a power consumption of 177 µW, occupying a chip area of 2.72 µm². The g_m/I_D design method was employed for analytical design and evaluation, which demonstrated strong agreement with the simulation results. The LA stage exhibits a voltage gain of 10.3 dB, a bandwidth of 32 GHz, a power consumption of 382 µW, and occupies 11.14 µm². The optical receiver achieves a transimpedance gain of 86.9 dBΩ, a −3 dB bandwidth of 34.2 GHz, a total power consumption of 1387 µW, and occupies 48.40 µm² of chip area. Simulation results, supported by theoretical validation, confirm that the optical receiver design provides high performance and low power consumption. These characteristics make it a strong candidate for integration into the next generation of energy-efficient optical communication systems.

Authors Contribution
All the authors have participated sufficiently in the intellectual content, conception, and design of this work or the analysis and interpretation of the data (when applicable), as well as the writing of the manuscript.

Availability of data and materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of interest
The author states that there is no conflict of interest.

References

[1] E. Säckinger, Analysis and design of transimpedance amplifiers for optical receivers, John Wiley & Sons, 2017.
DOI: 10.1002/9781119264422

[2] B. Razavi, Design of integrated circuits for optical communications, John Wiley & Sons, 2012.
isbn: 9781118439456

[3] W. Bae, "CMOS inverter as analog circuit: An overview", *Journal of Low Power Electronics and Applications,* vol. 9, no. 3, p. 26, 2019.
DOI: 2079-9268/9/3/26

[4] S. A. Hosseinisharif, M. Pourahmadi, and M. R. Shayesteh, "Utilization of a cascoded-inverter in an RGC structure as a low-power, broadband TIA", *Microelectronics Journal,* vol. 99, p. 104749, 2020.
DOI: j.mejo.2020.104749

[5] Y. Park and S. M. Park, "A dual-feedback folded-cascode fully differential transimpedance amplifier in 65-nm CMOS", *Journal of Semiconductor Technology and Science,* vol. 20, no. 3, pp. 281-287, 2020.
DOI: 10.5573/JSTS.2020.20.3.281

[6] M. Rajabzadeh, D. Djekic, M. Haeberle, J. Becker, J. Anders, and M. Ortmanns, "Comparison Study of Integrated Potentiostats: Resistive-TIA, Capacitive-TIA, CT ΣΔ Modulator", in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, IEEE, 2018, pp. 1-5.
DOI: ISCAS.2018.8351029

[7] R. H. Mekky, P.-V. Cicek, and M. N. El-Gamal, "Ultra low-power low-noise transimpedance amplifier for MEMS-based reference oscillators", in *2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS)*, IEEE, 2013, pp. 345-348.
DOI: 10.1109/ICECS.2013.6815425

[8] E. Säckinger, "Broadband circuits for optical fiber communication", John Wiley & Sons, 2005.
isbn: 9780471712336

[9] O. Ghasemi, "Stagger Tuning for BW extension in Transimpedance Amplifiers", in *2020 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, IEEE, 2020, pp. 1-4.
DOI: CCECE47787.2020.9255690

[10] M. M. Khafaji, G. Belfiore, and F. Ellinger, "A linear 65-GHz bandwidth and 71-dBΩ gain TIA with 7.2 pA/√Hz in 130-nm SiGe BiCMOS", *IEEE Solid-State Circuits Letters,* vol. 4, pp. 76-79, 2021.
DOI: 10.1109/LSSC.2021.3061535

[11] L. A. Valenzuela, A. Maharry, H. Andrade, C. L. Schow, and J. F. Buckwalter, "A 108-Gbps, 162-mW Cherry-Hooper Transimpedance Amplifier", in *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, IEEE, 2020, pp. 1-4.
DOI: 10.1109/BCICTS48439.2020.9392928

[12] Challayya Naidu, Pragada Venkata Satya, and C.-W. Lu, "Receiver Analog Front-End Cascading Transimpedance Amplifier and Continuous-Time Linear Equalizer for Signals of 5 to 30 Gb/s", *Electronics,* vol. 11, no. 10, p. 1546, 2022.
DOI: 10.3390/electronics11101546

[13] J. Han, B. Choi, M. Seo, J. Yun, D. Lee, T. Kim, Y. Eo, and S. M. Park, "A 20-Gb/s Transformer-Based Current-Mode Optical Receiver in 0.13- μm CMOS", *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 57, no. 5, pp. 348-352, 2010.
DOI: TCSII.2010.2047309

[14] C. Tao, L. Lei, Z. Hong, and Y. Huang, "Design of a 50MHz Bandwidth TIA Using Negative Capacitance", in *2022 IEEE 16th International Conference on Solid-State & Integrated Circuit Technology (ICSICT)*, IEEE, 2022, pp. 1-3.
DOI: ICSICT55466.2022.9963222

[15] B. Razavi, "The active inductor [A circuit for all seasons]", *IEEE Solid-State Circuits Magazine,* vol. 12, no. 2, pp. 7-11, 2020.
DOI: MSSC.2020.2987500

[16] M. Atalla and D. Kahng, "Metal Oxide Semiconductor (MOS) Transistor Demonstrated Silicon Engine", *Computer History Museum,* 1960,
metal-oxide-semiconductor

[17] N. Patil, J. Deng, S. Mitra, and H.-S. P. Wong, "Circuit-level performance benchmarking and scalability analysis of carbon nanotube transistor circuits", *IEEE Transactions on Nanotechnology,* vol. 8, no. 1, pp. 37-45, 2009.
DOI: 10.1109/TNANO.2008.2006903

[18] A. Imran, M. Hasan, A. Islam, and S. A. Abbasi, "Optimized design of a 32-nm CNFET-based low-power ultrawideband CCII", *IEEE Transactions on Nanotechnology,* vol. 11, no. 6, pp. 1100-1109, 2012.
DOI: 10.1109/TNANO.2012.2212248

[19] G. Cho, F. Lombardi, and Y.-B. Kim, "Modelling a CNTFET with undeposited CNT defects", in *Defect and Fault Tolerance in VLSI Systems (DFT), 2010 IEEE 25th International Symposium on*, IEEE, 2010, pp. 289-296.
DOI: 10.1109/DFT.2010.42

[20] A. Raychowdhury, S. Mukhopadhyay, and K. Roy, "A circuit-compatible model of ballistic carbon nanotube field-effect transistors", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 10, no. 10, pp. 1411-1420, 2004.
DOI: 10.1109/TCAD.2004.835135

[21] Q. Zhang, Carbon nanotubes and their applications, Pan Stanford Publishing, 2012.
isbn: 9789814303187

[22] M. Fuhrer, B. Kim, T. Duerkop, and T. Brintlinger, "High-mobility nanotube transistor memory", *Nano Letters,* vol. 2, no. 7, pp. 755-759, 2002.
DOI: 10.1021/nl025577o

[23] J. Appenzeller, "Electronic transport in carbon nanotube field-effect transistors", in *Semiconductor Device Research Symposium, 2003 International*, IEEE, 2003, pp. 410-411.
DOI: 10.1109/ISDRS.2003.1272157

[24] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors", *IEEE Transactions on Electron Devices,* vol. 50, no. 9, pp. 1853-1864, 2003.
DOI: 10.1109/TED.2003.815366

[25] J. Appenzeller, "AC and DC characteristics of carbon nanotube field-effect transistors", in *Bipolar/BiCMOS Circuits and*

Technology, 2004. Proceedings of the 2004 Meeting, IEEE, 2004, pp. 192-193.
DOI: 10.1109/BIPOL.2004.1365777

[26] R. Compano, L. Molenkamp, and D. Paul, "European Commission IST Programme", *Future and Emerging Technologies, Technology Roadmap for Nanoelectronics,* 2000.
DOI: 10.13140/RG.2.2.29861.47847

[27] A. Naeemi, R. Sarvari, and J. D. Meindl, "Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI)", *IEEE Electron Device Letters,* vol. 26, no. 2, pp. 84-86, 2005.
DOI:10.1109/LED.2004.841440

[28] G. Hills, C. Lau, A. Wright, S. Fuller, M. D. Bishop, T. Srimani, P. Kanhaiya, R. Ho, A. Amer, Y. Stein, D. Murphy, A. Chandrakasan, and M. Shulaker, "Modern microprocessor built from complementary carbon nanotube transistors", *Nature,* vol. 572, no. 7771, pp. 595-602, 2019.
DOI: 10.1038/s41586-019-1493-8

[29] A. Javey, R. Tu, D. Farmer, J. Guo, R. Gordon, and H. Dai, "High performance n-type carbon nanotube field-effect transistors with chemically doped contacts", *Nano letters,* vol. 5, no. 2, pp. 345-348, 2005.
DOI: 10.1021/nl047931j

[30] R. Ismail, M. T. Ahmadi, and S. Anwar, Advanced nanoelectronics, CRC Press, 2018.
isbn: 9781138072879

[31] A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, and H. Dai, "Self-aligned ballistic molecular transistors and electrically parallel nanotube arrays", *Nano letters,* vol. 4, no. 7, pp. 1319-1322, 2004.
DOI: 10.1021/nl049222b

[32] C. T. Chan, D. A. Johns, and M. W. Kenneth, Analog Integrated Circuits Design, John Wiley & Sons, Inc, 2011.
isbn: 9780470770108

[33] B. Razavi, Design of analog CMOS integrated circuits - Second edition, McGraw-Hill ed., 2016.
isbn: 9780072524932

[34] P. Karuppanan and K. Anuradha, "Study and Analysis of A Simple Self Cascode Regulated Cascode Amplifier", *International Journal of Engineering,* vol. 31, no. 10, pp. 1633-1641, 2018.
DOI: 82196_23b7156e8

[35] P. Jespers, The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches, Springer Science & Business Media, 2009.
isbn: 9780387471013

[36] F. P. Cortes and S. Bampi, "Miller OTA Design using a Design Methodology Based on the gm/Id and Early-Voltage Characteristics: Design Considerations and Experimental Results", in *Proceedings of XII Workshop Iberchip*, 2006, pp. 10-13.
DOI: 161.111.232.132

[37] M. Yasir and N. Alam, "Systematic design of CNTFET based OTA and Op amp using gm/ID technique", *Analog Integrated Circuits and Signal Processing,* vol. 102, no. 2, pp. 293-307, 2020.
DOI: 10.1007/s10470-019-01492-0

[38] J. Kim and J. F. Buckwalter, "Bandwidth enhancement with low group-delay variation for a 40-Gb/s transimpedance amplifier", *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 57, no. 8, pp. 1964-1972, 2010.
DOI: 10.1109/TCSI.2010.2041502

[39] S. Bashiri, C. Plett, J. Aguirre, and P. Schvan, "A 40 Gb/s transimpedance amplifier in 65 nm CMOS", in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, IEEE, 2010, pp. 757-760.
DOI: 10.1109/ISCAS.2010.5537465

[40] J. Kim and J. F. Buckwalter, "A 40-Gb/s optical transceiver front-end in 45 nm SOI CMOS", *IEEE Journal of Solid-State Circuits,* vol. 47, no. 3, pp. 615-626, 2012.
DOI: 10.1109/JSSC.2011.2178723

[41] S.-T. Chou, S.-H. Huang, Z.-H. Hong, and W.-Z. Chen, "A 40 Gbps optical receiver analog front-end in 65 nm CMOS", in *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, IEEE, 2012, pp. 1736-1739.
DOI: 10.1109/ISCAS.2012.6271598

[42] K. Park and W.-S. Oh, "A 40-Gb/s 310-fJ/b inverter-based CMOS optical receiver front-end", *IEEE Photonics Technology Letters,* vol. 27, no. 18, pp. 1931-1933, 2015.
DOI: 10.1109/LPT.2015.2447283

[43] Z. Xuan, R. Ding, Y. Liu, T. Baehr-Jones, M. Hochberg, and F. Aflatouni, "A low-power 40 Gb/s optical receiver in silicon", in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, IEEE, 2015, pp. 315-318.
DOI: 10.1109/RFIC.2015.7337768

[44] Z. Xuan, R. Ding, Y. Liu, T. Baehr-Jones, M. Hochberg, and F. Aflatouni, "A low-power hybrid-integrated 40-Gb/s optical receiver in silicon", *IEEE Transactions on Microwave Theory and Techniques,* vol. 66, no. 1, pp. 589-595, 2017.
DOI: 10.1109/TMTT.2017.2712144

[45] H.-W. Hsu, X.-Y. Ye, J.-J. Jou, and T.-T. Shih, "A 40-Gb/s NRZ Inductorless Transimpedance Amplifier in a 0.18-μm SiGe BiCMOS Technology", in *2021 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*, IEEE, 2021, pp. 1-2.
DOI: 10.1109/ISPACS51563.2021.9650922

[46] J.-J. Jou, T.-T. Shih, and H.-W. Hsu, "32-Gb/s NRZ and 40-Gb/s PAM-4 transimpedance amplifier paralleling with a differentiator for bandwidth enhancement in 90-nm CMOS technology", *Circuits, Systems, and Signal Processing,* vol. 41, no. 2, pp. 621-635, 2022.
DOI: 10.1007/s00034-021-01826-2