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A Squarer Circuit's Topological Innovations for Signal Processing Transcendence

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Abstract

In this study, we embark on an exploration of the versatile applications of a CMOS squaring circuit, unveiling its potential as an invaluable asset in the realm of analog signal processing. The reconfigurable nature of this circuit bestows upon it a remarkable malleability, rendering it a fundamental analog cell, a veritable canvas upon which a myriad of building blocks can be meticulously crafted. These building blocks encompass a diverse array of functionalities, including multipliers, logarithmic modules, dividers, and exponential function generators, each a vital component in the symphony of analog signal manipulation. Moreover, this innovative circuit presents an ingenious solution for the implementation of analog logarithmic and exponential functions, characteristics that have long eluded seamless integration into CMOS technology. The proposed circuits have been meticulously simulated using the industry-standard HSPICE, with the BSIM3v3 model tailored for a 0.35µm MOS process. Furthermore, the resulting simulations have been validated through rigorous analysis and cross-referencing with MATLAB-derived data, ensuring the utmost accuracy and reliability of our findings.

Keywords: Mathematical function, Current-mode, Fundamental cell, Signal processing applications

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1. Introduction

In the contemporary landscape of analog signal processing, computational circuits have emerged as indispensable workhorses, their versatility enabling the realization of a myriad of mathematical functions that undergird numerous applications [1]-[7]. The exponential function, a paragon of utility, finds its calling in the realms of telecommunications, medical equipment, disk drives, and hearing devices, its influence permeating a diverse array of domains [1]-[3]. Concurrently, the multiplication and squaring stand as fundamental operations, their presence woven into the very fabric of applications in the processing of signals, including frequency translation, signal modulation, and the intricate architectures of fuzzy systems and complicated networks for neurons [4], [5]. Additionally, architecture predicated upon principles of fuzzy demands the integration of division functionality within its output stage, a critical component aptly termed the defuzzification block [6]. Simultaneously, in the realm of analog signal processors (ASPs), the logarithmic function assumes a pivotal role, its implementation enabling the realization of logarithmic amplifiers [7]. Concomitantly, an overarching aspiration within the domain of integrated analog designs is the pursuit of modularity, wherein a single cell can be harnessed for multiple applications. This paradigm of reusability holds the promise of significantly reducing the design costs associated with each implemented function, a tantalizing prospect that has catalyzed the exploration of novel architectures. In this vein, the squaring circuit emerges as a preeminent candidate for the role of a "Fundamental cell," its versatility and utility rendering it a valuable

asset. This circuit has been realized through a panoply of approaches. The first draws upon the feature inherent to metal oxide semiconductor transistors operating within the saturated regime [7]-[10]. Additionally, novel squarer circuits have been proposed, wherein voltage signals are accepted as inputs, and current signals are produced as outputs [11]. These circuits exhibit a commendable simplicity of structure, requiring fewer transistors, yet necessitating the integration of threshold voltage generator circuits. The circuit presented in [4] leverages the trans linear loop principle, thereby attaining a desirable combination of wide bandwidth and high dynamic range. However, this architecture necessitates the inclusion of auxiliary circuits to generate the requisite input signals, a consequence of which is an increased power dissipation profile. Within the pages of this scholarly endeavor, we embark on an exploration of the multifaceted applications of a current-mode squaring circuit, unveiling its prowess as an invaluable asset in the realm of analog signal processing.

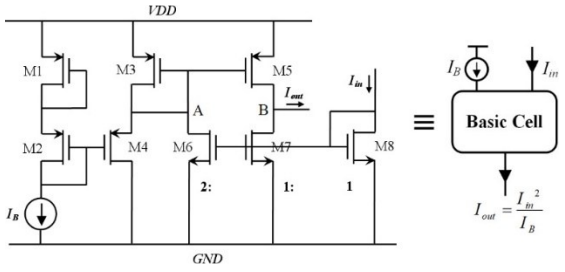
This pioneering circuit architecture finds its foundation in the intricate interplay of dual trans linear loops, harnessing their synergy as a "Fundamental cell" from which a myriad of computational circuits can be realized. Design experiences garnered over years of dedicated inquiry have illuminated the significant advantages that circuits predicated upon "dual trans linear loops" – an architectural paradigm that harmoniously weaves together N-type and P-type MOS– can offer when compared to their regular counterparts. These latter structures, constrained by the utilization of either N-type or P-type alone, often exhibit limitations [11]-[16]. In contrast, the "dual trans linear loop" approach transcends these boundaries, ushering in a new era of enhanced performance. The presented cell is meticulously designed to realize a diverse array of building blocks that form the bedrock of analog signal processors. These include multipliers, dividers, logarithmic modules, and exponential function generators, each a vital component in the intricate symphony of analog signal manipulation. Moreover, this work proposes an ingenious method in the configuration of EXP and LOG characteristics that have long eluded seamless integration into CMOS technology. By harnessing the power of this reconfigurable cell, these elusive functions can now be seamlessly woven into the fabric of a unified, configurable architecture. The current-mode implementation of these circuits offers a path of elegant simplicity, yielding configurations that are both intuitive and straightforward, thereby facilitating their practical realization and integration into larger systems. The performance of these circuits has been meticulously characterized using the industry-standard simulators, operating in 3.3V and leveraging the BSIM3v3 model tailored for the 0.35μm CMOS process. This comprehensive characterization ensures a thorough understanding of the circuits' behavior, paving the way for their seamless integration into practical applications.

2. Explanation of Fundamental Cell

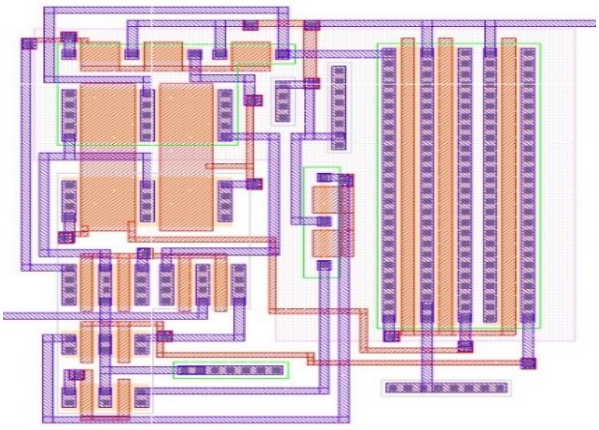
Fig. 1 demonstrates a fundamental cell that is utilized to realize mathematical functions as well as the layout of the circuit. When operating within the saturation region, the current for PMOS is analytically explained as follows:

$$I_{SD} = K_p(V_{SG} - |V_{tp}|)^2 \tag{1}$$

$$V_{SG} = |V_{tp}| + \sqrt{\frac{I_{SD}}{K_p}} \tag{2}$$



(a)



(b)

Figure 1. The circuit of a squarer, which is used as the "fundamental cell", (a) transistor level and (b) in layout

This elegant formulation encapsulates the fundamental relationship that underpins the cell's operation, providing a theoretical framework upon which the architectural intricacies are meticulously constructed. However, it is prudent to note that in practical

realizations, the influence of these secondary effects cannot be entirely neglected, necessitating a nuanced consideration of their impact on the circuit's performance characteristics. With this theoretical bedrock firmly established, we turn our focus to the exquisite choreography that unfolds within the dual translinear loop, where currents and voltages engage in a delicate equilibrium, orchestrating the realization of the squaring function with remarkable precision.

Let us consider the exquisite equilibrium that unfolds within the loop comprising the transistors M.1 through M.5. By considering this harmonious ensemble, we arrive at the following elegant relationship:

$$V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \tag{3}$$

All transistors are biased to operate within the saturation regime. Invoking the foundational principles elucidated in Eqs. (1) and (2), and acknowledging the condition $I_{SD1}=I_{SD2}=I_B$, we can derive:

$$\sqrt{I_{SD1}} + \sqrt{I_{SD2}} = \sqrt{I_{SD3}} + \sqrt{I_{SD4}} \tag{4}$$

This analytical expression encapsulates the delicate balance that must be maintained within the dual translinear loop, a harmony that underpins the circuit's operation.

To witness the resonance of precision that this architectural paragon achieves, let us turn our attention to the simulation results depicted in Fig. 2. Here, we observe the input signal at 1MHz, its corresponding out, and the meticulous value of error – a testament to the circuit's unyielding pursuit of accuracy. The bottom plot in this figure shows the value of the measured error, indicating that the mean value of the output error is 0.26%.

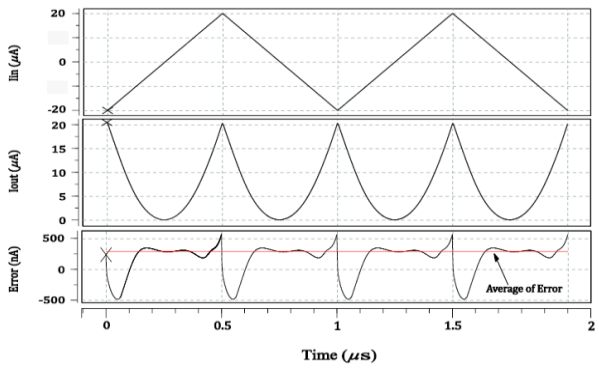


Figure 2. Signals for squarer circuit: a) input, b) output, and c) error

$$I_{SD3} = I_{SD5} = I_{out} + I_{in} \tag{5}$$

$$I_{SD4} = I_{SD3} - 2I_{in} = I_{out} - I_{in} \tag{6}$$

By exchanging these expressions into Eq. (4) and raising both sides to the power of two times, we unveil:

$$16{I_B}^2 - 16I_B I_{out} + 4{I_{out}}^2 = 4{I_{out}}^2 - {I_{in}}^2 \tag{7}$$

Then the output can thus be elegantly expressed as:

$$I_{out} = \frac{{I_{in}}^2}{4I_B} + I_B \tag{8}$$

This iconic relationship, encapsulated in Eq. (8), represents the expected output. That is noteworthy that the output current will be harnessed in the form of I_{in2}/I_B, facilitated by the judicious integration of a deductor circuit, meticulously dimensioned to achieve the desired outcome. The simulation results in the frequency of 1MHz are demonstrated for 10μA constant current in Fig. 2. Also, the average of power consumption is 0.185mW.

3. Introducing Some Applications

Considering "fundamental cell" as our architectural cornerstone, and the judicious integration of additional current mirrors whenever necessary, we can orchestrate a symphony of analog building blocks, each a vital component in the intricate tapestry of signal processing.

3.1. Exp Function

In this section, an innovative estimation function is introduced to refine the operational scope of the Taylor expansion, facilitating the efficient design of the exponential computation module. The standard Taylor series poses implementation challenges due to its intricate structure, while simultaneously demanding numerous polynomial terms to achieve satisfactory precision. To address these limitations, a novel mathematical model derived through the *linear least squares regression* technique in MATLAB is proposed, expressed as follows:

$$e^x \approx 1.45x^2 + 0.1x + 1.17 \qquad 0 < x < 2 \tag{9}$$

This optimized approach significantly simplifies circuit realization while maintaining high computational accuracy. The MATLAB-derived approximation function for exponential computation is depicted in Fig. 3. Circuit form for approximated function is demonstrated in Fig. 4, as well as the layout of the circuit, while the Fundamental cell, as well as some current mirrors, implement the function.

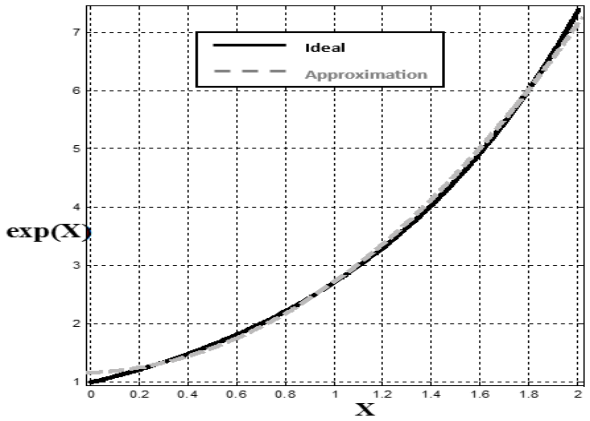
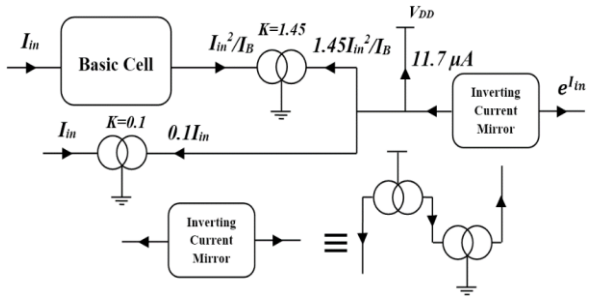


Figure 3. MATLAB-derived approximation function for exponential computation



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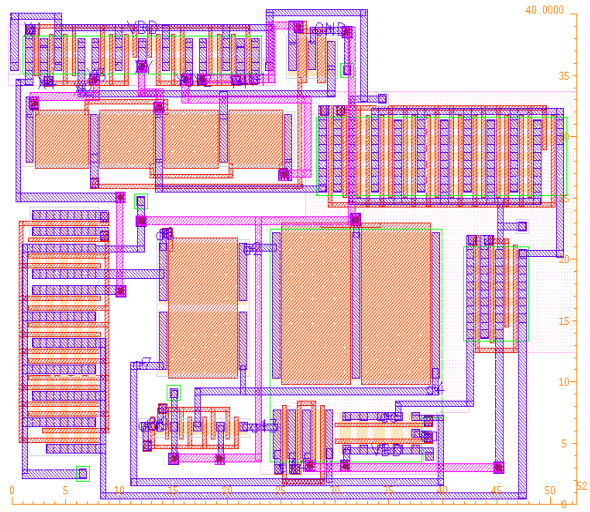


(b)

Figure 4. The circuit that realizes the Exp, (a) transistor level and (b) layout

To illustrate circuit efficiency, HSPICE results have been shown in Fig. 5.

In this figure, the ideal output as well as the approximated output resulting from HSPICE are shown in the same chart. Also, the error quantity shows the precise applicability of the design. The average of the error is 1.2 μA.

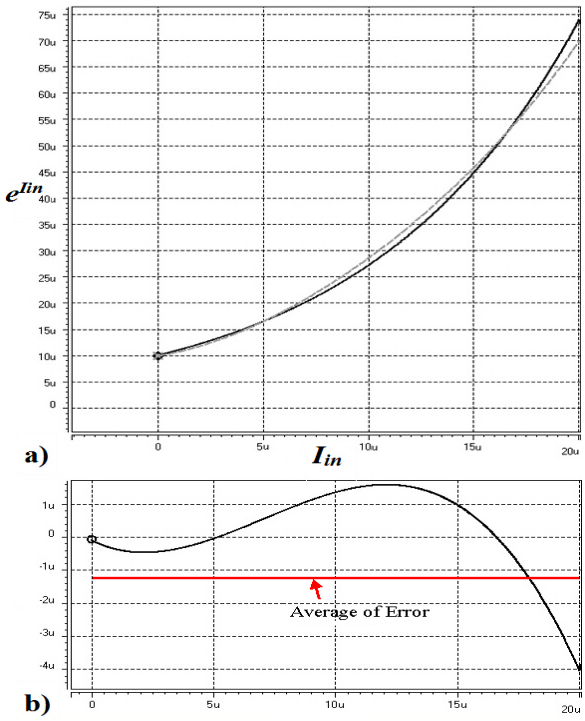


Figure 5. The results of EXPFG: a) input vs. output, and b) the error results

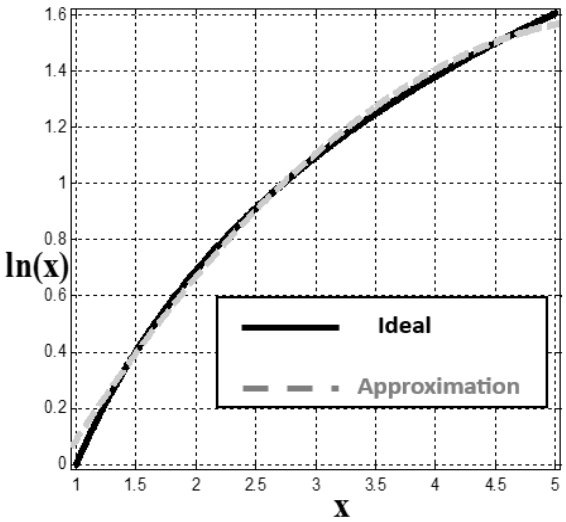


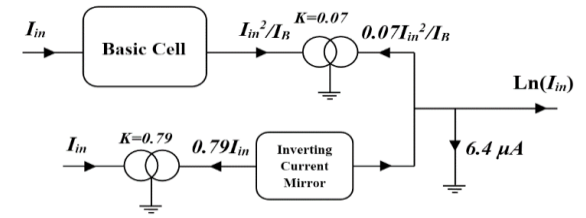
Figure 6. Logarithmic function approximation obtained through MATLAB curve-fitting optimization

3.2. Logarithmic Function

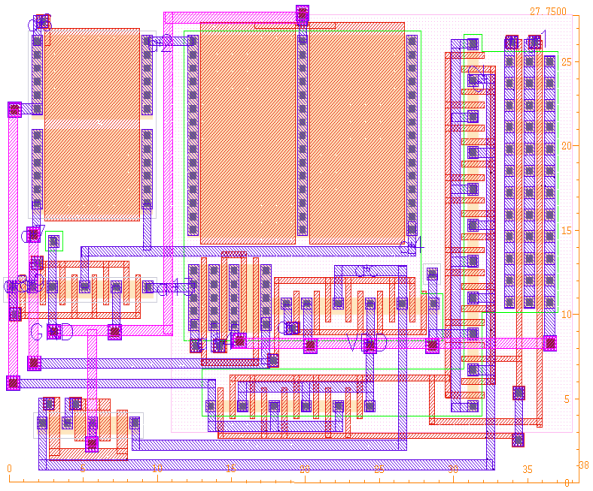
For the logarithmic function, we applied the same methodology previously used for the exponential function optimization. The derived approximation, formulated using MATLAB's computational analysis, is given by:

$$Ln(x) \approx -0.07x^2 + 0.79x - 0.64 \quad (10)$$

$$1 < x < 5$$



(a)



(b)

Figure 7. CMOS implementation of the proposed logarithmic approximation circuit, (a) transistor level and (b) layout

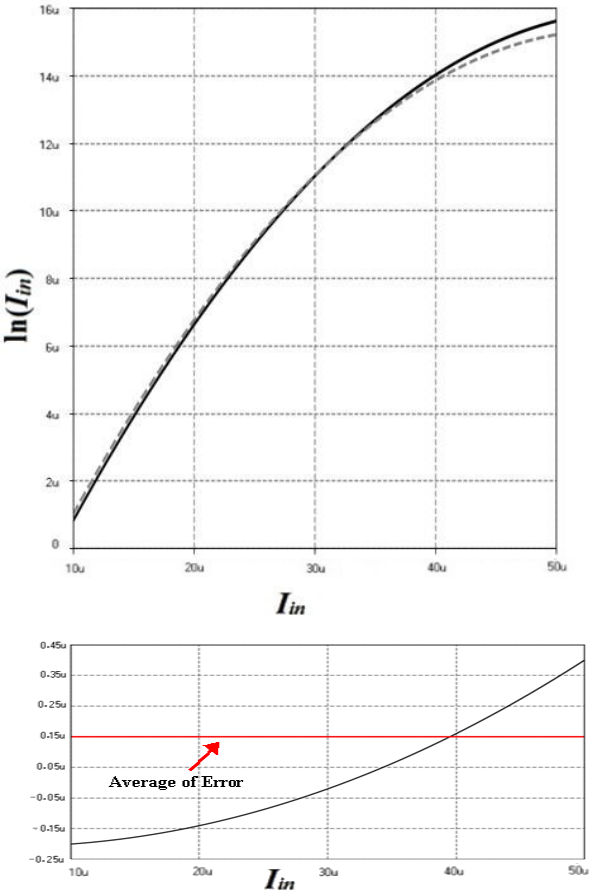


Figure 8. Input vs. output of the LOG function, as well as the circuit error

The MATLB-generated results, illustrated in Fig. 6, demonstrate the effectiveness of the proposed function. Fig. 7 shows the implemented function via the Fundamental cell and also several additional simple circuits, as well as the layout of the circuit. Additionally, the circuit simulation outcomes in Fig. 8 confirm successful hardware implementation, validating both accuracy and feasibility. The average of the error for this circuit is 0.15 μA.

3.3. Analog Multiplier

The idea underpinning the working of this multiplying circuit is rooted in synergy between the "Fundamental cell" and a mathematical relation:

$$(x+y)^2-(x-y)^2=4xy \tag{11}$$

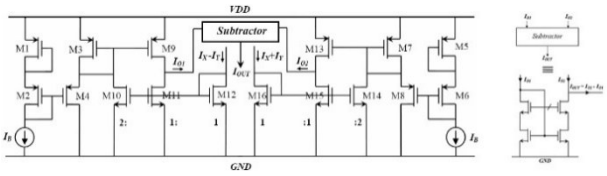
Behold the realization of this circuit as well as the layout of the circuit, depicted on the illustrious Fig. 9. This architectural marvel is predicated upon the harmonious interplay of 2 loops:

$$I_{O1}=\frac{(I_x-I_y)^2}{4I_B}+I_B \tag{12}$$

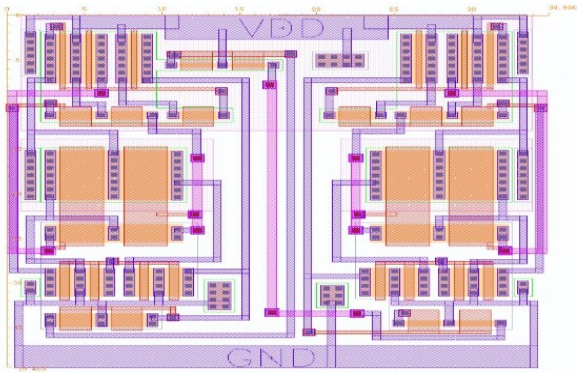
$$I_{O2}=\frac{(I_x+I_y)^2}{4I_B}+I_B \tag{13}$$

$$I_{out}=I_{O2}-I_{O1} \tag{14}$$

$$I_{out}=\frac{I_xI_y}{I_B} \tag{15}$$



(a)



(b)**Figure 9.** Multiplying by employing two “Fundamental cells”, (a) transistor level and (b) layout

As the eloquence of (15) unveils, this intricate configuration results in the expected output. Fig. 10 illustrates the output results of the multiplier circuit with the measured error; I_x and I_y are the sinusoidal inputs at 200 kHz with amplitudes of 10 and 5 µA, respectively. The output signal that is indicated in red is a high-accuracy sinusoidal signal. The mean absolute value of the measured error is equal to 47.1nA.

3.4. Divider Function

Turning our attention to Eq. (15) once more, we uncover the inherent potential for division.

By judiciously maintaining the current I_Y (or I_X) as an input, the resulting signal is depicted in Fig. 9. Thus, the division function is revealed, a paradigm that necessitates a prudent consideration of the bias signal that cannot decrease from a known voltage.

Multiplication ability to seamlessly transition into a divider function is elegantly portrayed in Fig. 11. With I_Y normalized to unity, and for various I_X, the desired output unveils the circuit's versatility and adaptability. power consumption is 0.185mW.

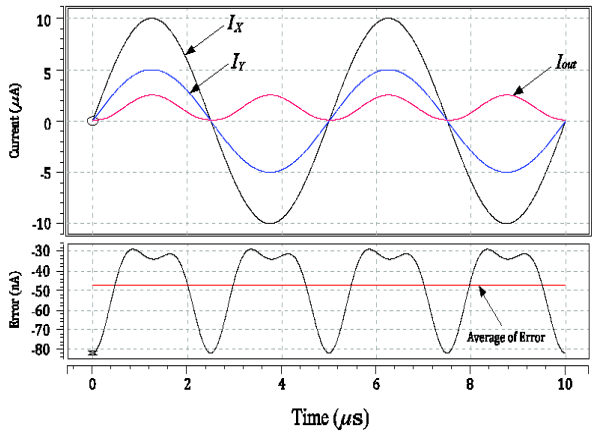


Figure 10. Simulation of proposed multiplier circuit at 200 kHz with the measured error

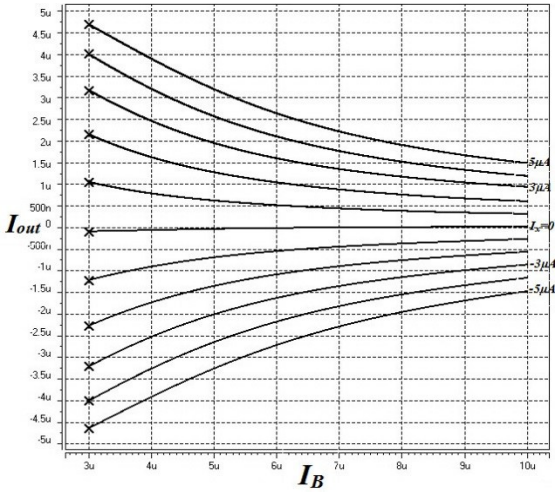


Figure 11. Circuit simulation result for division

4. Introducing Some Applications

Fundamental cell analysis considering channel length modulation, voltage of threshold, and Input range is presented in this part.

4.1. Mismatch of Threshold Voltage

The analysis considers the mismatch of Δ in the voltage of threshold in transistor1 through 4 in the trans linear. The voltage of source gates is given as $V_{SGn} = V_{tn} + \Delta V_n$, where $V_{tn} = V_t + \delta_n$.

Rewriting Eq. (3):

$$V_{SG1} + \delta_1 + V_{SG2} + \delta_2 = V_{SG3} + \delta_3 + V_{SG4} + \delta_4 \quad (16)$$

Considering $\delta_1 + \delta_2 = \Delta_{12}$ and $\delta_3 + \delta_4 = \Delta_{34}$:

$$V_{SG1} + V_{SG2} + \Delta_{12} = V_{SG3} + V_{SG4} + \Delta_{34} \quad (17)$$

Supposing $\Delta_{12} - \Delta_{34} = \Delta$, then:

$$4I_B I_{out}\Delta - 4{I_B}^2 - 2I_B\Delta^2 - 8I_B\Delta + 4I_B I_{out}\Delta^4 - 2I_B\Delta^3 + I_{out}\Delta^2 - 4{I_B}^2\Delta^2 = {I_{in}}^2 \quad (18)$$

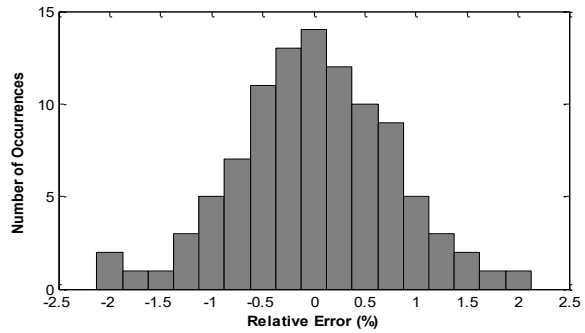
Because Δ is very small (< 10 mV), then Δ^2, Δ^3, and Δ^4 can be negligible. The output can be derived as:

$$I_{out} = \frac{{I_{in}}^2}{4I_B(1+\Delta)} + \frac{I_B + 2\Delta}{1+\Delta} \quad (19)$$

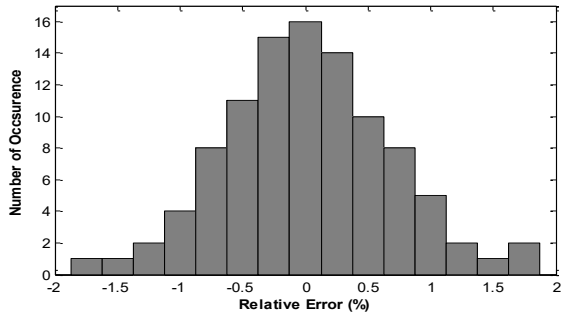
Considering 1>>Δ, the output of "Fundamental cell" is:

$$I_{out} \approx \frac{{I_{in}}^2}{4I_B} + I_B + 2\Delta \quad (20)$$

This shows that the threshold voltage mismatch causes 2Δ as offset voltage. The Compensation of this DC offset is done via controlling an appropriate bias current (I_B). A Monte-Carlo simulation with 100 iterations was conducted to evaluate the influence of transistor dimensions on circuit performance. The ideal mismatch-free output served as the reference for error calculation. Introducing a ±5% variation in transistor sizing parameters revealed that 86% of the cases exhibited deviations within ±1%, leaving 14% of instances with errors beyond this margin. These outcomes are illustrated in Fig. 12(a). Additionally, a similar statistical assessment was carried out to examine threshold voltage mismatch effects. Under identical conditions and a ±5% variation in threshold voltage, 91% of samples showed an error margin within ±1%. The corresponding results are presented in Fig. 12(b).



(a)



(b)

Figure 12. a) Results of Monte-Carlo analysis for the a) aspect ratios of transistors b) threshold voltage considering ±5% mismatch (for 100 samples)

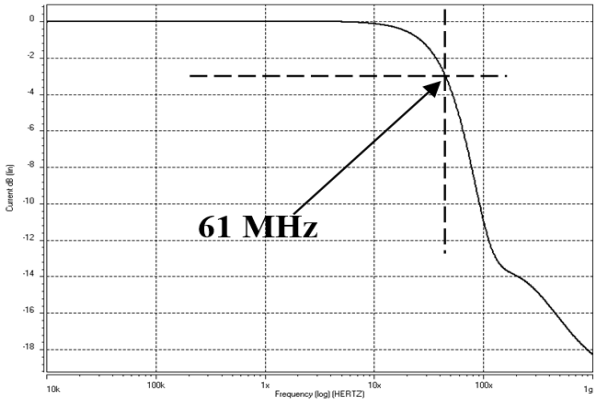


Figure 13. Frequency response of the fundamental circuit

4.2. Modulation in Channel Length

Modulation in the Channel Length is presented as follows:

$$I_{SD} = K_p(V_{SG} - |V_{tp}|)^2(1 + \gamma V_{SD}) \quad (21)$$

In this equation, λ introduces the modulation coefficient. It is obvious that with low V_{SD}, this effect becomes low. In our proposed circuit, because of employing long lengths for transistors, this error can be considered negligible.

4.3. Input Scale for Fundamental Cell

The issue for this subject is limited via transistors M-1 to M-4, which operate in saturated which is expressed as [14]:

$$2\sqrt{I_B} \geq \sqrt{I_{out} + I_{in}} + \sqrt{I_{out} - I_{in}} \quad (22)$$

Considering $I_{in}=XI_B$ and then substituting Eq. (8) in Eq. (22), the parameter of X, which is the maximum value for the circuit, is obtained:

by solving the above equation, X= and, X=±2, where the value of X=+2 is right, hence: $I_{in} \leq 2I_B$. Thus, the range of the input signal is restricted to $2I_B$. The result of the circuit bandwidth simulation is shown in the Fig. 13, where an attempt has been made to achieve an acceptable value compared to previous works. In this simulation, the -3dB frequency of the fundamental circuit is equal to 61MHz.

$$2\sqrt{I_B} \geq \sqrt{\frac{X^2 {I_B}^2}{4I_B} + I_B + XI_B} + \sqrt{\frac{X^2 {I_B}^2}{4I_B} + I_B - XI_B} \quad (23)$$

5. Conclusion

In this scholarly endeavor, the exploration delved into the myriad applications of a CMOS squaring circuit within the realm of analog signal processing. This circuit, christened the "Fundamental cell", was harnessed as the foundational element for realizing LOG, EXP, Division, and Multiplication architecture, each a testament to its versatility. This ingenious solution encompassed the seamless integration of these functions into a configurable cell, a feat that exemplified the synergy between innovation and practicality. The circuits were brought to life through a current-mode realization, an approach that bestowed upon them a simplicity and intuitive nature, qualities that are coveted in the realm of design and implementation. The proposed circuits underwent a meticulous design and simulation process, facilitated by the HSPICE simulator, a powerful tool that leveraged the BSIM3v3 of the 0.35µm MOS Process. This rigorous process ensured the circuits' adherence to industry standards and paved the way for their practical realization.

To further validate the integrity of the simulation results obtained from HSPICE, the researchers employed MATLAB, a renowned computational software, to verify and corroborate the findings. This

cross-validation ensured the robustness and reliability of the proposed circuits, reinforcing their potential for real-world applications.

A comparison between the fundamental block of this work and similar works is shown in Table 1.

Table 1. Comparison between this work and previous works

Ref.	Technology (μm)	Supply Voltage (V)	Input range (μA)	Power consumption (mW)	Bandwidth(MHz)
[17]	0.8	1.5	0–10	NA	NA
[18]	2.4	1.5	0–10	0.21	5
[19]	0.35	3.3	±10	NA	4.49
[20]	0.18	0.7	±30	0.08435	56
[21]	0.18	0.85	±120	0.225	15
This work	0.35	3.3	±180 (depends on I_B)	0.185	61

Authors Contribution
All the authors have participated sufficiently in the intellectual content, conception and design of this work or the analysis and interpretation of the data (when applicable), as well as the writing of the manuscript.

Availability of data and materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of interest
The author states that there is no conflict of interest.

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