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Optimized Reversible Parity-Preserving Multiplier Circuits in Nanotechnology

Meysam Mappar [1], Ehsan PourAliAkbar [2,*]
Amin MehranZadeh[1], Mohammad Mosleh[1]

[1] *Department of Computer Engineering, Dez.C., Islamic Azad University, Dezful, Iran*
[2] *Department of Computer Engineering, MaS.C., Islamic Azad University, Masjed Soleiman, Iran*

***Corresponding author:** pour.ali@iau.ac.ir

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Abstract

Reversible logic, as one of the new technologies, plays a significant role in designing quantum computers due to the absence of energy loss, as well as using reversible circuits in low-power CMOS circuits, quantum calculations, and DNA computing. Multipliers are among the most critical circuits in computer calculations. This study proposes an optimized unsigned and signed reversible parity-preserving multiplier circuit. In addition, this study seeks to present a reversible block, as well as reversible signed and unsigned multiplier circuits using the presented block and the proposed design. The presented circuits reduce the quantum cost and are considered parity-preserving. In order to utilize the designs presented in variable sizes, two circuits in n×n sizes are provided. Further, a number of equations are presented to calculate the quantum costs, along with the number of constant inputs and garbage outputs in the proposed circuits.

Keywords: Quantum computing, Signed multiplier, Reversible multiplier, Reversible logic, Parity-preserving, Unsigned multiplier

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1. Introduction

VLSI circuits are designed to reduce energy loss. R. Landauer proposed that irreversible computations in hardware result in significant energy loss. The energy dissipated when a single bit of information is erased amounts to KTLN2 joules. In this equation, K refers to Boltzmann's constant, which is equal to $1.3806505 \times 10^{-23}$ $m^2kg^{-2}K^{-1}$ (joules per Kelvin), and T represents the absolute temperature during the process [1]. Reversible logic circuits exhibit virtually no internal power consumption, as they operate without any significant energy loss. Furthermore, Bennett (1973) argued that when the circuit is designed using a reversible approach, it avoids incurring KTLn2 energy loss [2]. A one-to-one relationship is observed between equal inputs and outputs in reversible logic, allowing output values to be derived from input values and vice versa. As observed in Eq. (1), the input vector Iv and output vector Ov demonstrate the input and output of a reversible logic circuit, respectively [3].

$$IV = (I_1, I_2, I_3, \dots, I_n)$$
$$OV = (O_1, O_2, O_3, \dots, O_n) \quad (1)$$

Feedback and fan-out cannot be applied in reversible logic circuits. A reversible parity-preserving circuit requires the use of reversible parity-preserving gates and blocks. A gate is called parity-preserving when there is an equilibrium between its inputs and outputs. In other words, the XOR in the input values must be equal to that of the output ones in the gate [3]. Reversible logic can be utilized in quantum

calculations, designing low-power circuits, and DNA computing [4-7].

Multiplication has long been recognized as a fundamental operation in computing and logical systems, serving a wide range of purposes. Circuit speeds are considered challenging in the modern world, and multipliers are no exception. A clear relationship can be observed where an increase in speed enhances the performance of multiplier circuits, thereby improving the efficiency of various electronic systems. Designing a fast and optimal reversible unsigned and signed multiplier circuit has attracted a lot of attention in reversible logic.

So far, a large number of reversible logical multiplier circuits have been provided, some of which are observed in [8-32]. Some of the previously mentioned multipliers are considered unsigned [10], [13], [19], [22], [26-29], while others are discussed as signed [18], [20], [21], [23]. In addition, some of the above-mentioned multipliers are regarded as parity-preserving [20], [21], [23], [29].

Section 2 focuses on some basic concepts in logical reversible concepts. Section 3 offers a comprehensive summary of the current body of literature. Section 4 delves into an in-depth analysis of the proposed designs. Section 5 investigates the proposed circuits and their comparisons with previous works. At last the conclusion is reviewed in Section 6.

2. Basic definitions

The reversible logical basic introduction is studied here. Then, a number of reversible parity-preserving logic gates are evaluated. At last the multiplier reversible circuits are shown.

2.1. Reversible logic

Reversible logic is observed when an exclusive relationship is reported between equal inputs and outputs in a function so that the outputs can be achieved from the inputs and vice versa. The assessment of reversible logic circuits can be conducted by analyzing specific evaluation criteria. The inputs, which are summed to an n×k function to become an n×n one so that the aforementioned circuit can be reversed, are called constant input (CI) [33]. Unused outputs in a reversible circuit, which are not utilized in subsequent steps, are referred to as garbage outputs (GOs) [34].

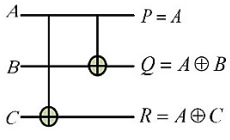


Figure 1. Reversible parity-preserving F2G gate

Quantum cost (QC) is considered a more critical criterion than can be evaluate reversible circuits. The QC in all of 2×2 circuits equal 1, while that of larger circuits equals the total QC of its 2×2 or 1×1 circuits. Generally, V and V+ are two QC in reversible logical circuits. The square root is regarded as another name for gate V.

Eq.(2) is established for V and V+ quantum gates [35].

$$V \times V = V^{+} \times V^{+} = NOT$$
$$V \times V^{+} = I \quad (2)$$

2.2. Reversible gates

Reversible logic has brought forth a diverse range of gates and building blocks, which are broadly classified into parity-preserving and non-parity-preserving variants. Using parity-preserving gates creates a parity-preserving circuit. Feynman [36], Toffoli [37], Peres [38], and HNG [10] are among the most significant non-parity-preserving reversible gates, while F2G [39], NFT [40], and FRG [41] are among the most critical parity-preserving ones. Several parity-preserving gates are provided here, aligning with the design of the proposed multiplier circuits, which are also classified as parity-preserving.

The Reversible Feynman Double Gate (F2G) is recognized as a three-input gate that produces three matching outputs. It is categorized as a parity-preserving gate, with its inputs and outputs determined by the mathematical expressions provided in Eq. (3).

$$Iv = (A, B, C) \quad (3)$$
$$Ov = (P = A, Q = A \oplus B, R = A \oplus C)$$

Fig. 1 shows the F2G gate, which can be utilized to generate fan-out in parity-preserving reversible logic. The QC in the F2G gate equals 2.

Fredkin gate (FRG) is among the 3×3 gates applied in reversible logic, which is regarded as parity-preserving. The input and output values within the FRG gate are determined using Eq. (4).

$$Iv = (A, B, C) \quad (4)$$
$$Ov = (P = A, Q = A'B \oplus AC, R = A'C \oplus AB)$$

Fig. 2 illustrates the FRG gate. The FRG can be utilized in reversible logic to produce the AND function in parity-preserving reversible logic. The QC in the FRG gate equals 5.

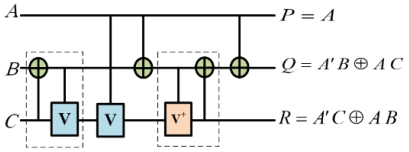


Figure 2. Parity-preserving Reversible FRG gate

The New Fault Tolerant Gate (NFT) is regarded as another type of reversible 3×3 gate. NFT gate is regarded as parity-preserving, whose inputs and outputs are calculated by Eq. (5).

$$Iv = (A, B, C) \quad (5)$$
$$Ov = (P = A \oplus B, Q = B'C \oplus AC', R = BC \oplus AC')$$

Fig. 3 demonstrates the NFT gate, which can be utilized to produce the AND in reversible parity-preserving circuits.

The QC in NFT gate equals 5.

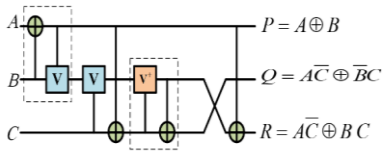


Figure 3. Reversible parity-preserving NFT gate

3. Literature review

This section provides an explanation of the multiplication operation. Following this, it delves into a discussion on the reversible unsigned and signed multiplier circuits previously introduced.

3.1. Irreversible multiplier

Multipliers are one of the most common operations in computing and can generally be classified into two types: unsigned and signed. In this method, the multiplication process is carried out in two phases known as partial product generation (PPG) and partial product addition (PPA) [42]. Fig. 4 displays the unsigned multiplication operation.

			X	X_3 Y_3	X_2 Y_2	X_1 Y_1	X_0 Y_0
				P_{30}	P_{20}	P_{10}	P_{00}
			P_{31}	P_{21}	P_{11}	P_{01}	
		P_{32}	P_{22}	P_{12}	P_{02}		
	P_{33}	P_{23}	P_{13}	P_{03}			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Figure 4. 4x4 Multiplication operation

3.2. Reversible Parity-preserving multiplier

Numerous reversible multiplier circuits, both signed and unsigned, have been introduced, with some being recognized as parity-preserving designs.

Thapliyal et al. (2006) proposed a non-parity-preserving unsigned reversible multiplier applying the TSG gate [22]. moreover, Haghparast and co-workers (2009) offered an unsigned reversible multiplier using PG, HNG, and TG gates [10]. Further, Moghadam et al. (2012) developed another circuit utilizing TG and PG logical gates [16]. moreover, Jigalur et al. (2015) presented a 4×4 unsigned reversible multiplier applying HNG and PG gates [13]. PourAliAkbar et al. (2019) designed a reversible unsigned multiplier circuit [19]. All of the above-mentioned circuits are regarded as non-parity-preserving.

In another study, Babazadeh et al. (2012) proposed a reversible parity-preserving unsigned multiplier circuit using FRG and MIG gates [25]. Jamal et al. (2013) offered another reversible unsigned parity-preserving multiplier circuit [29]. moreover, Valinataj (2017) offered reversible unsigned parity-preserving multiplier circuits [23].

Further, Qi et al. (2012) proposed a reversible signed parity-preserving multiplier [20]. Finally, PourAliAkbar et al. (2020) offered a reversible signed parity-preserving multiplier circuit in [21].

4. Proposed parity-preserving reversible multipliers

Here, four reversible parity-preserving multiplier circuits are discussed. The first proposed design focuses on two reversible unsigned multiplier circuits with parity-preserving capability. The second proposed design assesses two reversible parity-preserving signed multipliers. First, a proposed reversible parity-preserving block is offered. Then, a reversible 4×4 unsigned multiplier circuit is provided utilizing existing gates and blocks, as well as the proposed reversible block.

In the next step, the reversible parity-preserving unsigned multiplier in n×n sizes is evaluated. In the next procedure, a 5×5 reversible signed multiplier is examined. Valinataj (2017) offered a reversible parity-preserving signed multiplier circuit in the design presented in [23]. Finally, the circuit is expanded to an n×n size. Presenting the proposed designs in n×n sizes produces the proposed multiplier circuits in variable sizes.

4.1. Proposed block

The proposed block is considered a circuit with five inputs and five outputs, which exhibits parity-preserving capability due to its use in such circuits. Such a block is designed to provide a reversible circuit to produce a section of the outputs of a 2×2 multiplier. The output in the proposed block creates three bits out of four ones produced in a 2×2 multiplier circuit.

In fact, the outputs Q0, Q2, and Q3 can be produced in a 2×2 multiplier circuit in the PPA section after generating the product of the inputs in a 2×2 multiplier circuit in the PPG section. The QC reduces during the design of the proposed block. Fig. 5 shows the proposed block, which is called MEAM. The QC of the MEAM block equals 7.

Within the proposed approach, the circuit is designed such that the PPG section generates the P1 value. Subsequently, the MEAM block has been structured to produce the three remaining outputs P0, P2, and P3 in sequence from its first, second, and third outputs, respectively. In essence, the proposed block serves as a generator for three of the four components needed for a 2x2 multiplier, with the fourth component already provided. This approach has the potential to reduce quantum costs when performing sum-of-products operations in unsigned and signed reversible multiplier circuits. Furthermore, the proposed block can be utilized to optimize and enhance summation operations by aiming to minimize CI, GO, and QC in the process.

4.2. Proposed parity-preserving reversible 4×4 unsigned multiplier

A 4×4 parity-preserving unsigned multiplier circuit is presented here. The multiplication operation is divided into two sections. The PPG operation is performed in the first section, resulting in obtaining the AND results required for the multiplication operation, and the PPA circuit is offered in the second section.

Generally, 16 AND functions are required in the PPG section. Such functions are created by applying the FRG gates and E1 blocks.

A part of the PPA operation is performed in the PPG circuit. The sum value for PPA is calculated in two sections of the PPG circuit. More use of gates and blocks utilized in PPG results in achieving a part of the PPA operation during the previous step. Fig. 6 illustrates the PPG circuit.

As observed, the two proposed E1 blocks obtain the XOR result of two inputs in addition to producing an AND. The XOR result of functions x_0y_1 and x_1y_0 is achieved in block E1(A) in addition to producing x_0y_1, which is required as the sum in PPA, resulting in acquiring the output result of P_1.

Further, the XOR result of functions x_2y_1 and x_3y_0 is obtained in block E1(B) in addition to achieving x_2y_1, which is regarded as the sum result of the half adder (HA) function required in the PPA circuit. The aforementioned value is called M.

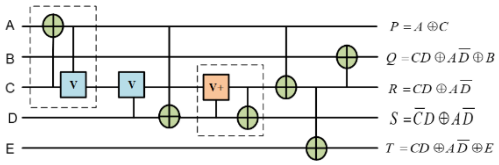


Figure 5. Our proposed reversible parity-preserving block (MEAM)

PPG design in a reversible unsigned multiplier requires 6 FRG gates and 10 E1 blocks.

The sum of products is calculated in the PPA stage. A PPA circuit is designed here, applying the results acquired from the AND production and the two sum values obtained in the PPG section. An optimal circuit is created with parity-preserving capability using blocks with optimal QC. Fig. 7 demonstrates the PPA in the unsigned reversible multiplier.

Generally, four HA and eight full adder (FA) are required in the PPA section. ZPLG and MEAM blocks are utilized as FA production and a complement to the values acquired during the previous step, respectively. The QC reduces in the PPA stage by separating a part of the calculations and obtaining their results separately. To this aim, two sets related to the values of the products of the 2×2 multiplier are separated from the entire PPA set. Then, the results are calculated separately.

Finally, the achieved results are summed with the rest of the values and the final result is acquired. It is worth noting that some of the calculations for the above-mentioned 2×2 multipliers are obtained in the PPG section.

4.3. Proposed reversible unsigned parity-preserving n×n multiplier

The present study seeks to design a circuit which can be created in variable sizes, in addition to a 4×4 reversible unsigned multiplier. This study aims to create an n×n multiplier unsigned circuit which can be expanded to variable and arbitrary sizes.

The aforementioned circuit includes PPG and PPA sections, as well. The FRG gates and E1 blocks are applied to produce PPG. The PPG section requires producing n^2 of AND function, 2n-2 functions of which are generated by FRG gates, and the rest are created by E1 blocks. Fig. 8 displays the PPG circuit in n×n sizes.

In fact, n HA functions are needed in the unsigned multiplier circuit in the PPA section. Thus, $\frac{n}{2}$ of E1 blocks are used in the proposed PPG circuit so that the sum value of the HA function is produced in the PPG, and their result is transferred to the PPA section.

Generally, n HA blocks and n×(n-2) FA blocks are needed in the PPA circuit. In addition, the sum value for half of the Has is produced in the PPG stage.

The MEAM block is used as a complement to the achieved results to produce HA in the PPG section. Further, ZPLG blocks are utilized as generators of the FA function. Fig. 9 shows the n×n PPA producer circuit.

Here, three equations are presented for calculating the QC, as well as the number of CIs and GOs of the proposed design.

The above-mentioned criteria are calculated using the obtained equations and knowing the scale of the circuit. The circuit of the PPG section is offered utilizing E1 blocks and FRG gates. In addition, MEAM and ZPLG blocks are applied to sum the products in the PPA section. Finally, the total QC of the proposed PPG and PPA circuits in n×n sizes is achieved from Eq. (6).

$$QC = 14n^2 - 14.5n + 2 \quad (6)$$

In addition, the number of CIs in the reversible unsigned multiplier circuit is obtained by Eq. (7) which is calculated in the sum of PPG and PPA circuits.

$$No.CI = 4n^2 - 5.5n + 2 \quad (7)$$

Further, an equation is provided to generate the number of GOs to be acquired in any intended size. Eq. (8) shows the aforementioned value.

$$No.GO = 4n^2 - 5n \quad (8)$$

The efficiency evaluation criteria of the proposed n×n reversible parity-preserving unsigned multiplier in scalable sizes can be checked, as well as comparing its results with previous works by Eqs. (6-8). In fact, the aforementioned design can be used in any size, as well as knowing the costs and other criteria of the circuit by designing the circuit in large sizes and determining the equation for calculating its evaluation criteria for each size.

4.4. Proposed reversible parity-preserving 5×5 signed multiplier

The present study seeks to present a proposed reversible parity-preserving signed multiplier circuit. Similar to the above-mentioned design, the signed multiplier circuit has two sections including the PPG and PPA, in which a circuit is provided to produce the required ANDs and NANDs, and the products obtained from the previous section are summed, respectively.

A signed 5×5 multiplier circuit requires the generation of

17 AND functions and 8 NAND functions. FRG gates and E1 blocks are utilized to generate products in the PPG section. FRG gates are applied to produce the required ANDs due to less QC in the FRG gate compared to the E1 block. Fig. 10 illustrates the proposed PPG circuit.
As observed, the PPG circuit requires 6 FRG gates and 19 E1 blocks. The third input value of E1 blocks is regarded to be 1 in places where NAND function generation is required, resulting in producing the NAND function of the inputs by the third output. Further, the E1(A) and E1(B) blocks are used more optimally, resulting in generating the product of the inputs and producing the sum of an HA, the value of which is required during the PPA step.

MEAM and ZPLG blocks are utilized in the PPA section. The MEAM blocks are applied to complete the two values achieved in the PPG section, while the ZPLG blocks are used to generate the FA function. Fig. 11 demonstrates the PPA circuit.
As shown, the PPA circuit includes 2 MEAM and 16 ZPLG blocks. The circuits in Figs. 10 and 11 produce the proposed reversible parity-preserving 5×5 signed multiplier circuit.

4.5. Proposed reversible parity-preserving n×n signed multiplier

This work presents the design of an n×n reversible signed multiplier that is parity-preserving. The PPG section in the above-mentioned circuit requires the production of n^2 AND and NAND functions, which produce E1 blocks and their FRG gates.

A part of the work related to the PPA section is conducted by producing a sum of half of the required HAs during the next step. Fig. 12 displays the PPG circuit in n×n sizes.
As observed, the number of E1 blocks in the proposed n×n PPG and the number of FRG gates utilized equal (n-1)2+3 and 2n-4, respectively. In addition, the third input is given a value of 1 in 2n-2 block E1 so that the NAND function can be produced by the third output. In order to apply the used blocks more optimally, the ZPLG blocks are utilized to generate the FA function, and the MEAM block is applied to complete the sum results acquired from the PPG stage. $2 * \left\lfloor \frac{n}{2} \right\rfloor$ HA function is required in the PPA section, leading to the completion of the results using $\left\lfloor \frac{n}{2} \right\rfloor$ MEAM blocks are due to their sum production in the previous section. Finally, the sum of products is completed utilizing ZPLG blocks. Fig. 13 shows the PPA in n×n sizes.
As illustrated, $\left\lfloor \frac{n}{2} \right\rfloor$ MEAM blocks are applied. The number of ZPLG blocks for the multiplication operation in the proposed multiplier circuit for n×n sizes equal $(n-1)^2$. The circuits in Figs. 12 and 13 produce the operation of multiplying two parity-preserving reversible signed numbers with n×n size.
Here, three equations are presented to calculate the efficiency evaluation criteria in variable sizes after designing the n×n reversible circuit parity-preserving signed multiplier. The efficiency criteria can be calculated by putting the arbitrary size of the circuit in the presented equations.
E1 blocks and FRG gates are utilized in the PPG section, while ZPLG and MEAM blocks are applied in the circuit design in the PPA section. The QC of the proposed signed multiplier is computed using Eq. (9).

$$Qc = 14n^2 - 18n + 7 * \left\lfloor \frac{n}{2} \right\rfloor + 12 \quad (9)$$

where the QC of the proposed circuit is calculated in the aforementioned sizes by replacing the value of n with the intended one. In addition, Eq. (10) can be utilized to calculate the number of CIs in the above-mentioned design.

$$NO.CI = 4n^2 - 6n + \left\lfloor \frac{n}{2} \right\rfloor + 7 \quad (10)$$

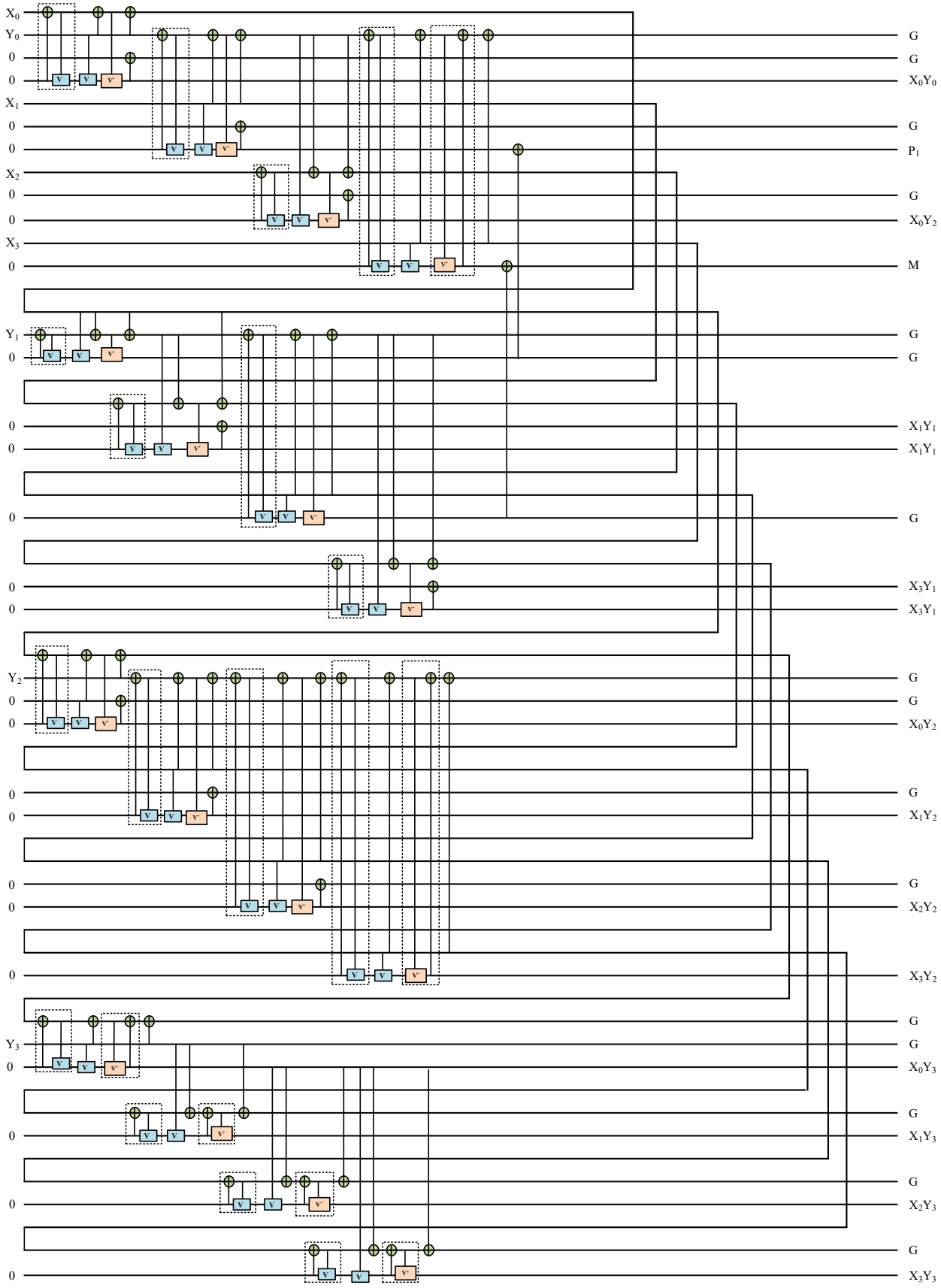
Further, Eq. (11) is applied to calculate in the reversible multiplier circuit the number of GOs.

$$NO.GO = 4n^2 - 6n + 2 * \left\lfloor \frac{n}{2} \right\rfloor + 5 \quad (11)$$

The CIs, GOs, and QC associated with the proposed reversible parity-preserving signed multiplier, irrespective of variable size or arbitrary dimensions, can be determined using Eqs. (9-11).
The proposed circuit might be designed in scalable and large sizes and its evaluation costs can be calculated by designing the proposed n×n multiplier circuit in Figs. 12 and 13 and presenting three calculation equations.

5. Evaluation and result of the proposed circuits

The present study focused on two reversible parity-preserving unsigned and signed multiplier circuits in 4×4 and n×n, as well as 5×5 and n×n sizes, respectively. The circuits included PPG and PPA sections. Here, the proposed circuits are assessed and compared with previous works.
Table 1 compares the reversible parity-preserving unsigned multiplier circuits.
As indicated, the proposed circuit has 44 CIs, 44 GOs, and a QC of 168, indicating its better results compared to previous works. The proposed circuit has 44 CIs, indicating a better result compared to the previous best work with 45 ones. In addition, the number of GOs in the proposed circuit (44) exhibits the best results compared to previous works. The number of GOs in the best result of previous works (45) means that the proposed design exhibits the best result. The QC in the proposed multiplier circuit (168) indicates the best result compared to previous works. The best QC before the proposed design equaled 169.



(A) Quantum design

Figure 6. Proposed PPG circuit in a reversible unsigned 4×4 multiplier circui.

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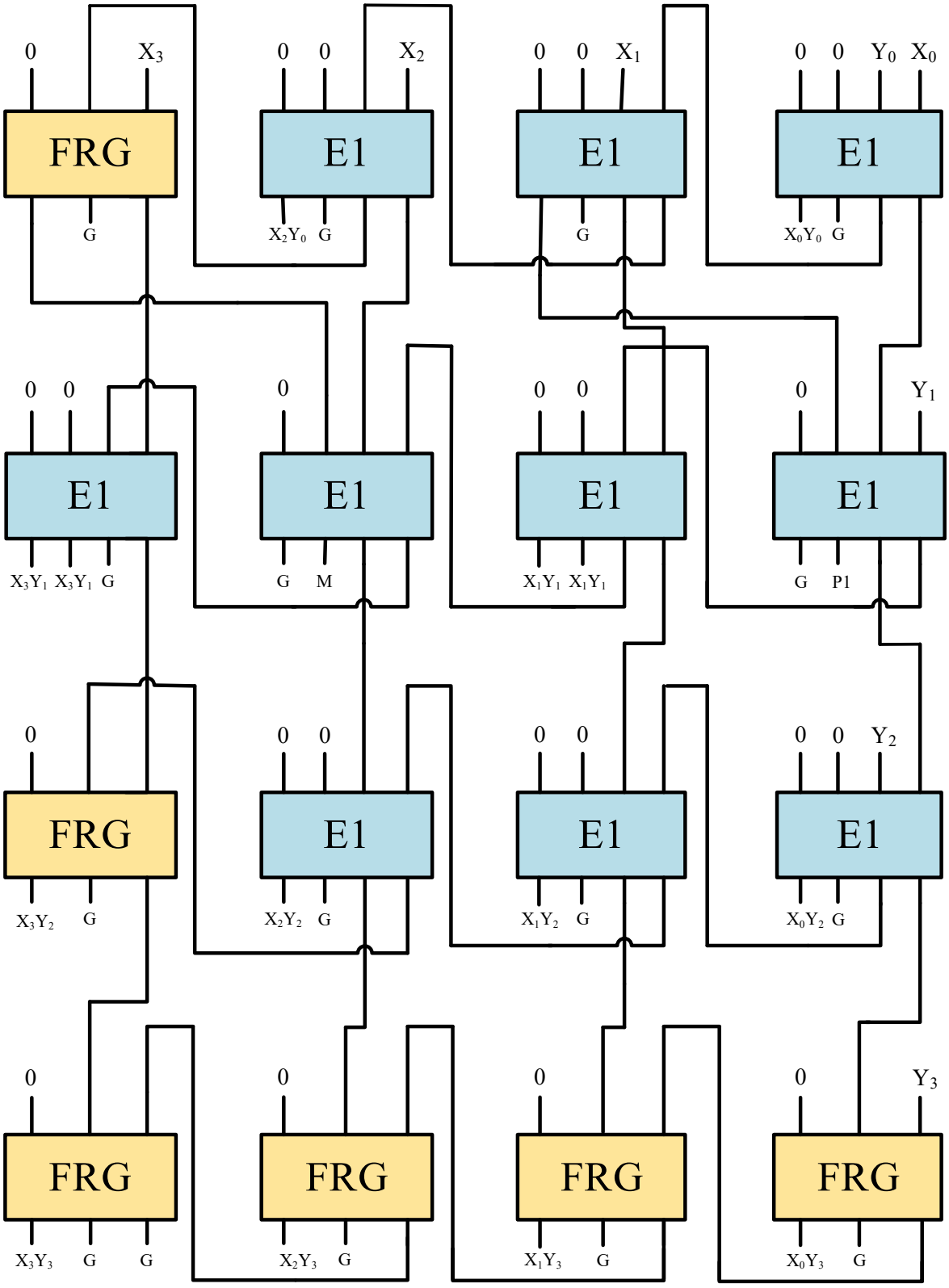
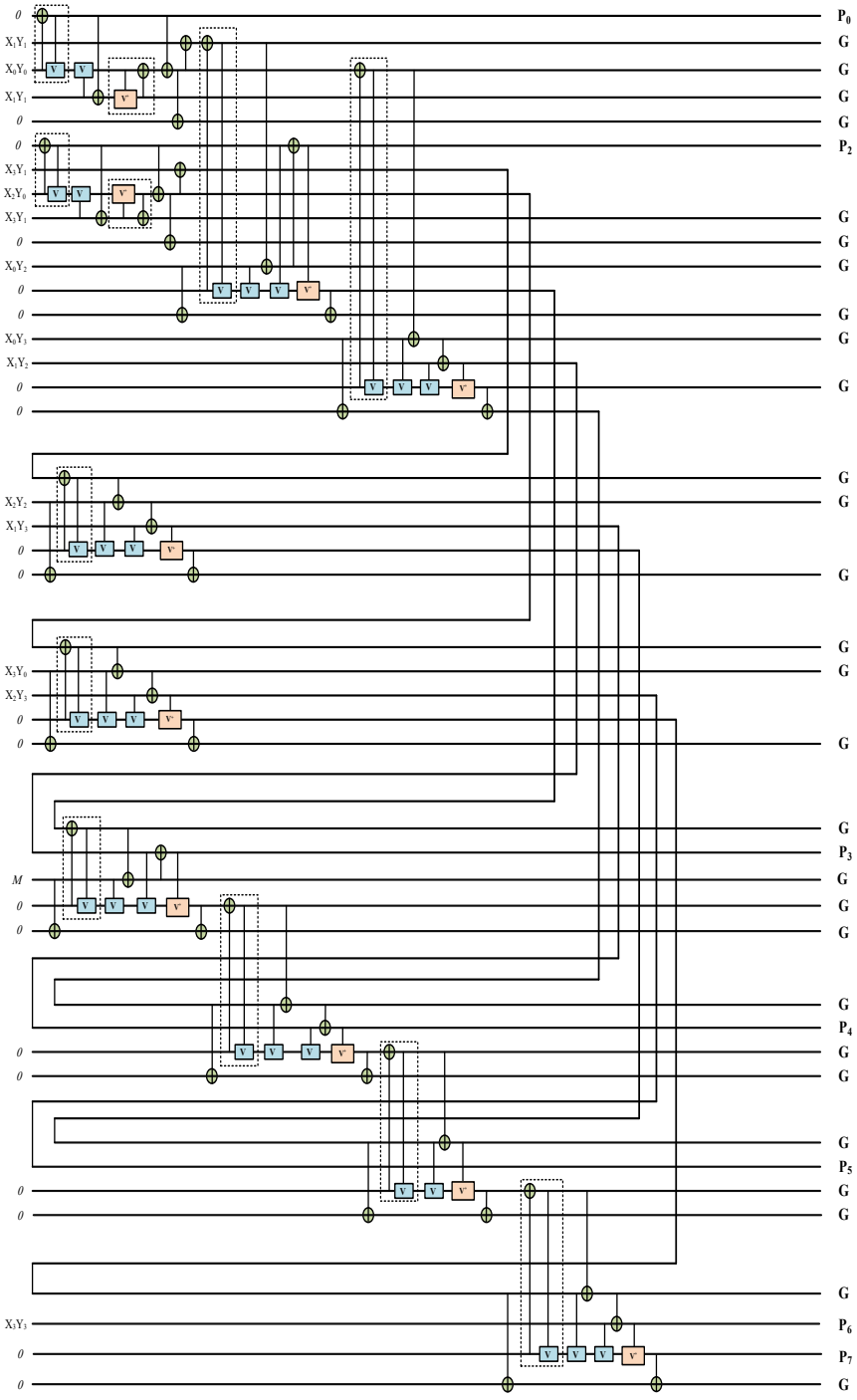


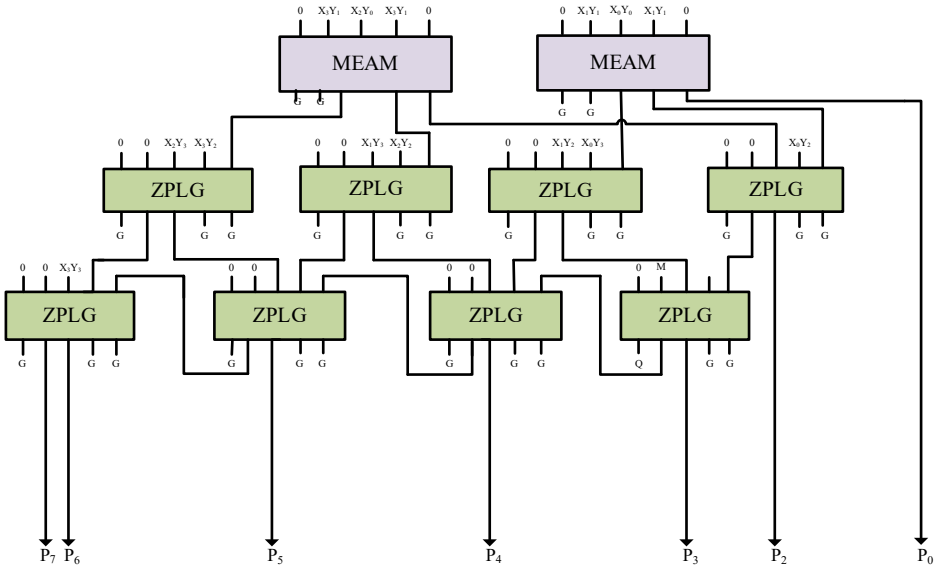
(B) Block diagram

Figure 6. Continued



(A) Quantum design

Figure 7. Proposed PPA in reversible unsigned 4×4 multiplier circuit



(B) Block diagram

Figure 7. Continued

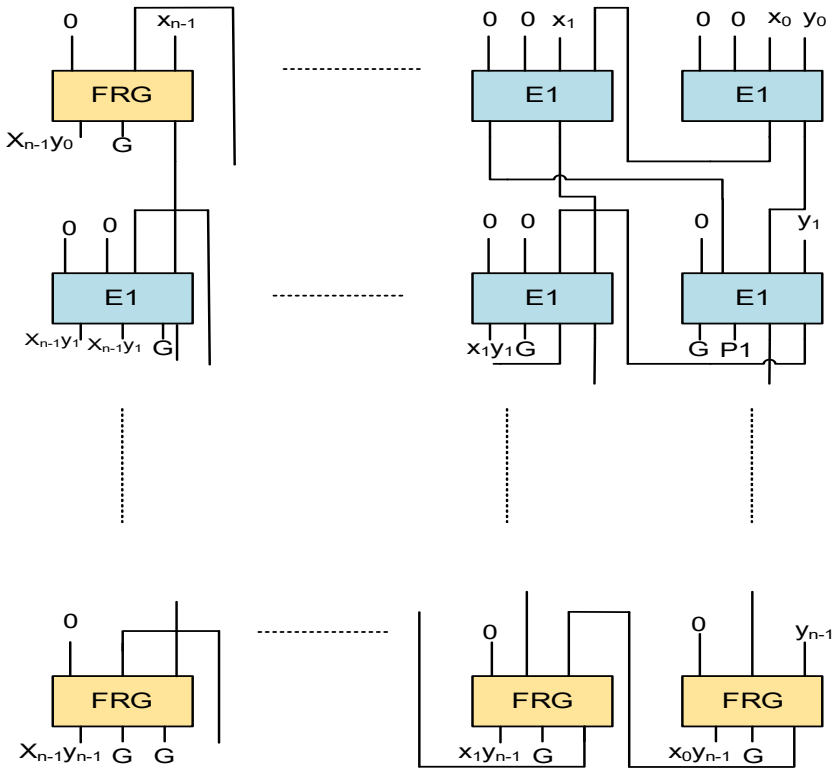


Figure 8. Proposed PPG circuit in reversible unsigned n×n multiplier circuit

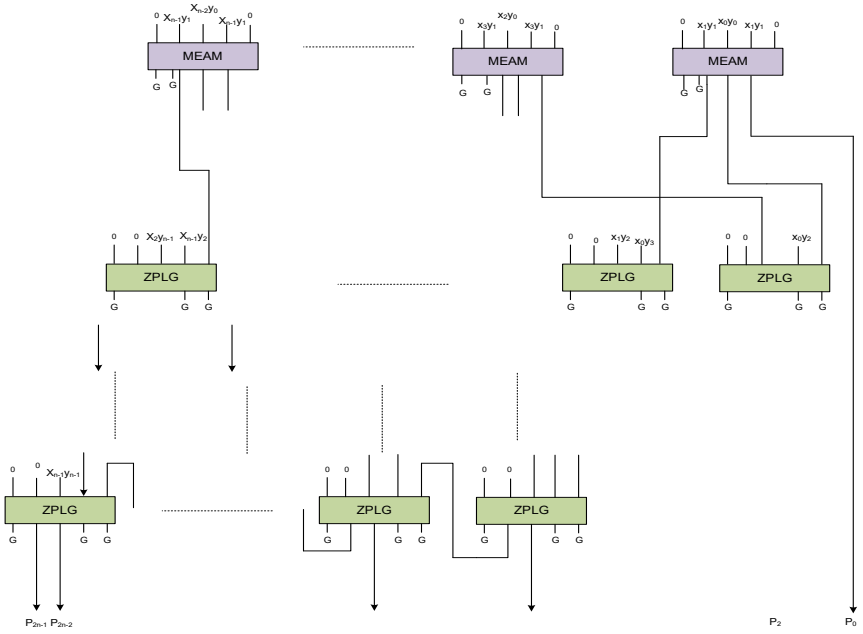
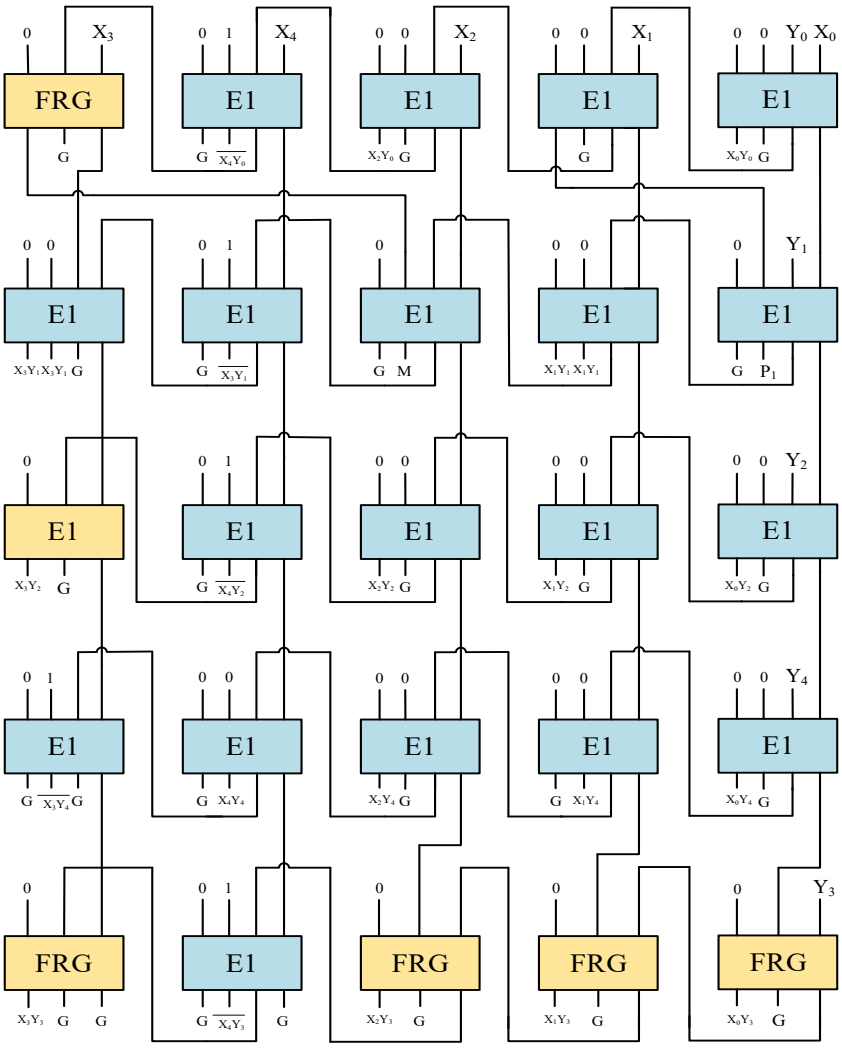


Figure 9. Proposed PPA circuit in a reversible unigned n×n multiplier circuit



(A) Block diagram

Figure 10. Proposed PPG circuit in a reversible signed 5×5 multiplier circuit

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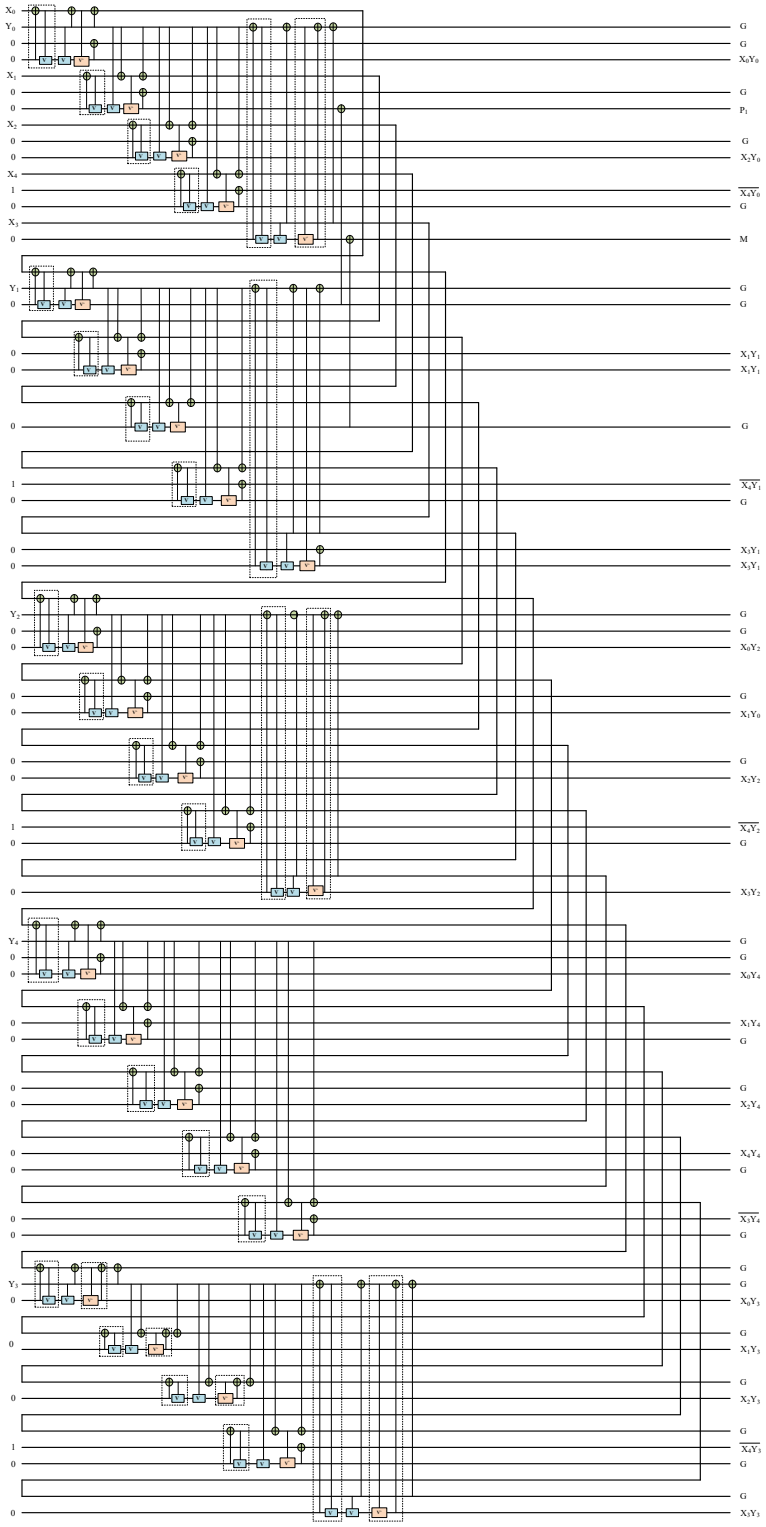

(B) Quantum design

Figure 10. Continued

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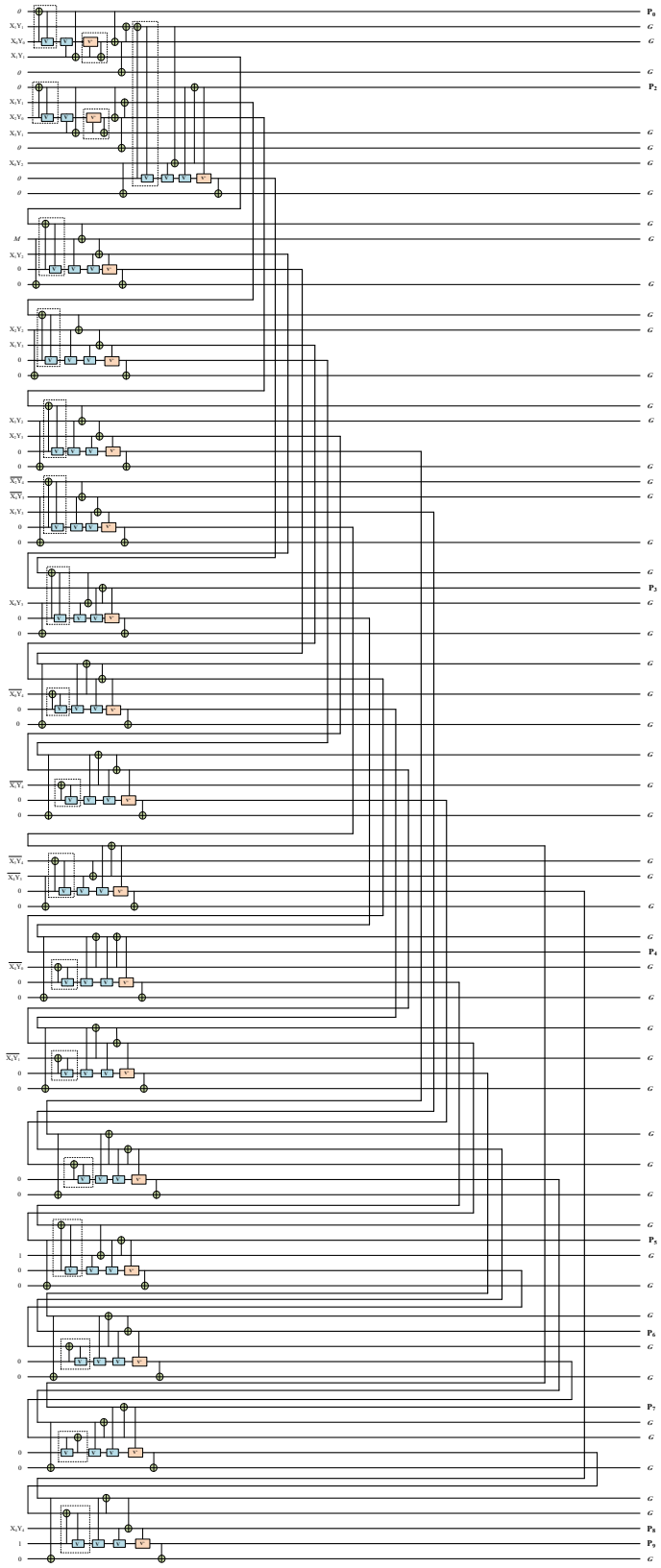
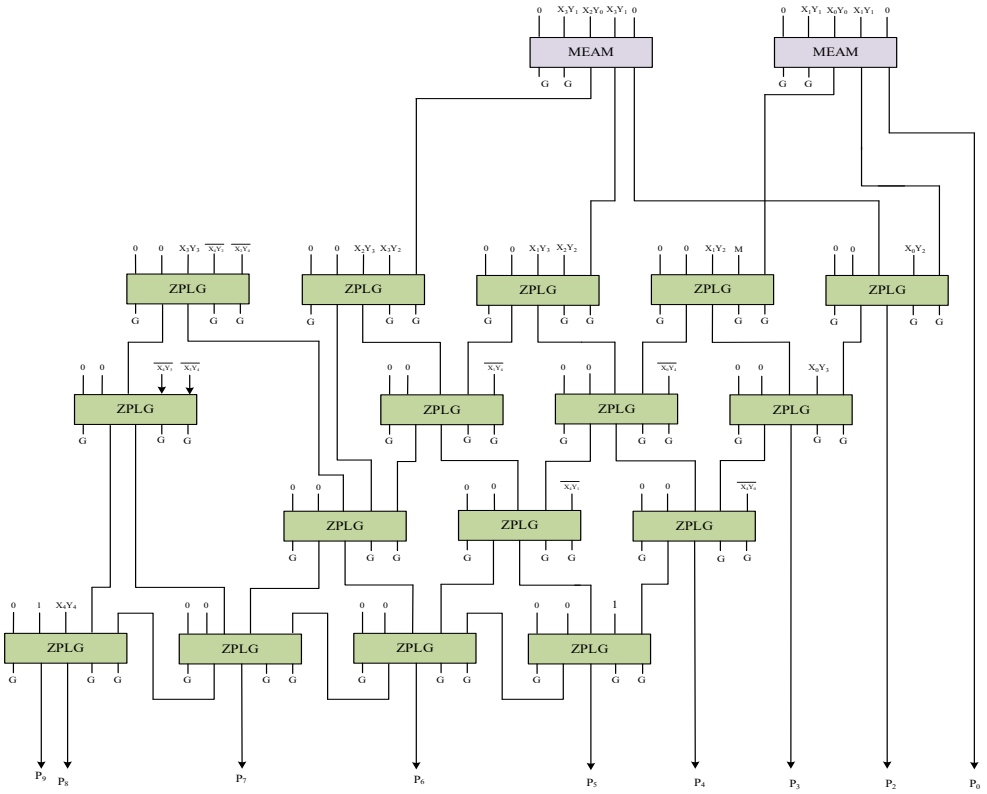


(A) Quantum design

Figure 11. Proposed PPA circuit in a reversible signed 5×5 multiplier circuit



(B) Block diagram

Figure 11. continued

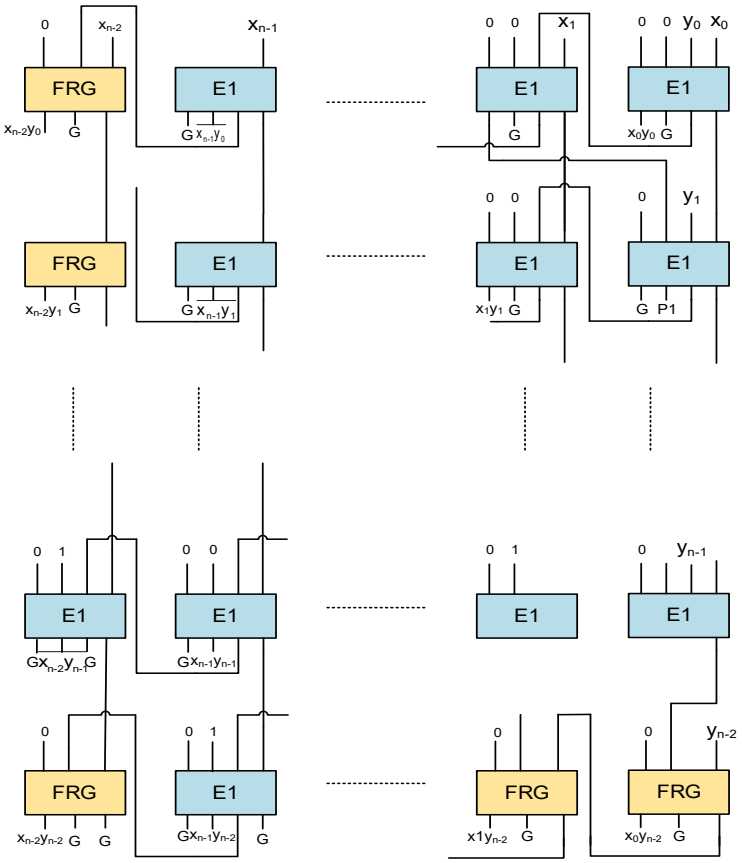


Figure 12. Proposed PPG circuit in n×n reversible signed multiplier circuit

Table 1. Comparative review of different reversible parity-preserving 4×4 unsigned multiplier

	N. of CI	N. of GO	QC
The Proposed Method	44	44	168
[21]	45	45	169
[29]	49	49	205
[23] (First Approach)	56	56	184
[23] (Second Approach)	49	49	177

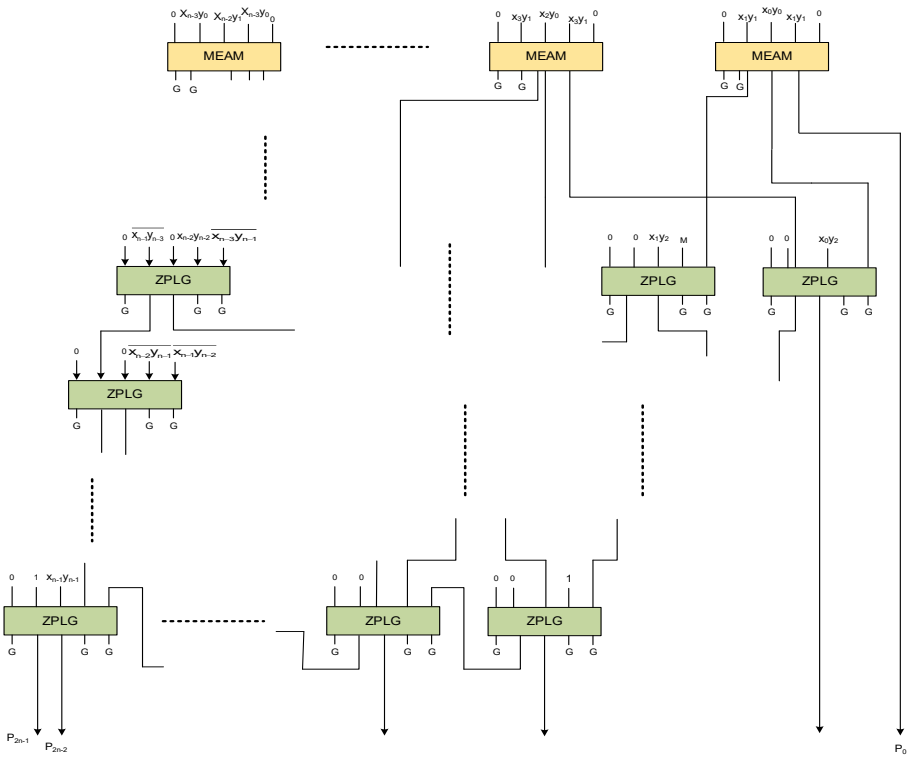


Figure 13. Proposed PPA circuit in n×n reversible signed multiplier circuit

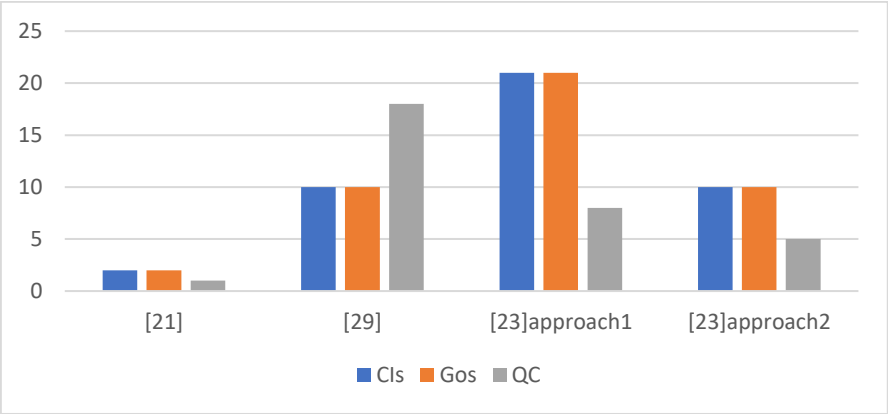


Figure 14. Improvement of the proposed 4×4 unsigned multiplier compared to previous designs

The diagram in Fig. 14 illustrates the percentage improvement of the proposed reversible unsigned multiplier circuit in terms of the number of CIs. Our work has achieved a %2 improvement compared to the best previous work [21].

In terms of GOs, as demonstrated in Fig. 14, our approach has resulted in a %10 enhancement over [29] which represents the most advanced existing work. Regarding quantum cost (QC), our proposed solution shows a %18 percent improvement compared to the [29], as detailed in Fig. 14.

The proposed reversible parity-preserving unsigned 4×4 multiplier demonstrates superior performance across all evaluation metrics compared to earlier designs.

The proposed reversible parity-preserving unsigned n×n multiplier is studied here. This study focuses on equations which help compute the QC, as well as the number of CIs and GOs of the circuit.

Table 2 represents the aforementioned equations compared to previous works.

Table 2 shows the efficiency improvement of the proposed design in the number of CIs and GOs, and also the QC.

The reversible 5×5 and n×n signed multiplier are reviewed here. Table 3 presents the 5x5 signed multiplier and related comparisons.

Table 2. Comparative review of different reversible parity-preserving n×n unsigned multiplier

	N. of CI	N. of GO	QC
The Proposed Method	$No.CI = 4n^2 - 5.5n + 2$	$No.GO = 4n^2 - 5n$	$QC = 14n^2 - 14.5n + 2$
[21]	$4n^2 - 5n + 1$	$4n^2 - 5n + 1$	$14(n^2 - n) + 1$
[23] (First Approach)	$3n^2 + 2n * (\lfloor \frac{n}{2} \rfloor - 1)$	$4n^2 - 3n$	$13n^2 + 2n * \lfloor \frac{n}{2} \rfloor + 10n$
[23] (Second Approach)	$4n^2 - 4n + 1$	$4n^2 - 4n + 1$	$14n^2 - 12n + 1$

Table 3. Comparative review of different reversible parity-preserving 5×5 sign multiplier

	N. of CI	N. of GO	QC
The Proposed Method	79	79	286
[21]	82	82	289
[20]	90	90	401
[23]	86	86	297

Table 3 indicates the proposed reversible 5×5 signed multiplier as for the number of CIs and GOs, as well as the QC, along with their results.

As observed, the number of CIs in the proposed circuit exhibits the best results compared to previous works. In addition, the number of GOs in the proposed design (79) shows the best efficiency compared to previous works.

The proposed circuit achieves a QC of 286, representing a significant improvement over previous implementations, which had values of 288 and 297.As depicted in Fig. 15, the proposed design demonstrates a %3 improvement in the number of CIs compared to the best previou work [21]. Similarly, according to Fig. 15, in terms of GOs, the presented method shows an improvement of %8 compared to [23]. Additionally, in terms of QC, our approach outperforms the best existing work, namely [21], as

illustrated in Fig. 15. According to the results, the proposed 5×5 reversible signed multiplier displays the best possible result as for the number of CIs and GOs, as well as the QC compared to previous works.

The n×n reversible parity-preserving signed multiplier circuits are analyzed here. As indicated, Eqs. (9-11) show the QC, as well as the number of CIs and GOs of the proposed design in n×n sizes. Table 4 represents the above-mentioned equation which are compared with previous works.

As presented in Table 4, the proposed reversible signed multiplier circuit exhibits a more optimal result than previous works in terms of QC, as well as the number of CIs and GOs.

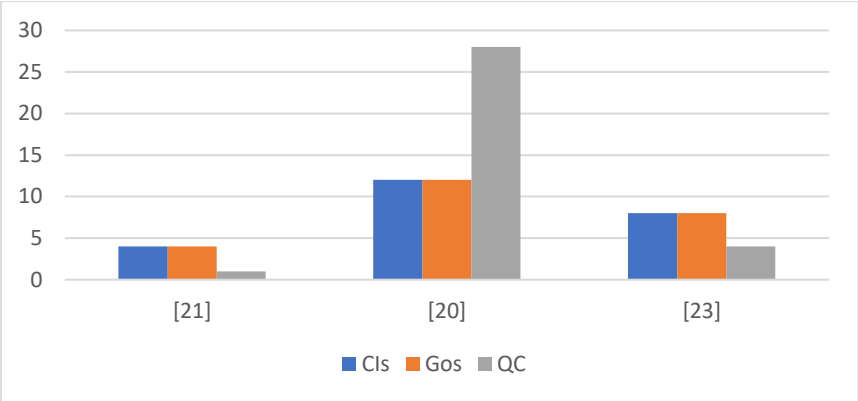


Figure 15. Improvement of the proposed 5×5 signed multiplier compared to previous designs.

Table 4. Comparative review of different reversible parity-preserving n×n sign multiplier

	N. of CI	N. of GO	QC
The Proposed Method	$NO.CI = 4n^2 - 6n + \lfloor \frac{n}{2} \rfloor + 7$	$NO.GO = 4n^2 - 6n + 2 * \lfloor \frac{n}{2} \rfloor + 5$	$Qc = 14n^2 - 18n + 7 * \lfloor \frac{n}{2} \rfloor + 12$
[21]	$4n^2 - 6n + 6 + 2 * \lfloor \frac{n}{2} \rfloor$	$4n^2 - 6n + 7 + 2 * \lfloor \frac{n}{2} \rfloor$	$14n^2 - 18n + 12 + 8 * \lfloor \frac{n}{2} \rfloor$
[23]	$4n^2 - 4n + 6$	$4n^2 - 4n + 6$	$14n^2 - 12n + 7$

4. Conclusion

The present study focused on reversible parity-preserving multiplier. First, a reversible parity-preserving block was presented. Then, the 4×4 reversible unsigned multiplier circuit was designed using the existing gates and the proposed block. as shown by the results, the proposed design exhibited the top results compared to the existing works in all of the fields of efficiency evaluation. In the next step, the reversible unsigned multiplier circuit was presented in n×n sizes, as well as providing 3 equations to calculate the costs of the circuit. The results indicated that the proposed unsigned multiplier circuit shown the top results in terms of QC, as well as the number of CIs and GOs relative to all of the previous works. In the next procedure, a 5×5 parity-preserving reversible signed multiplier circuit was offered, as well as proving that the proposed circuit shows the best efficiency relative to existing works. Then, a n×n signed reversible parity-preserving multiplier circuit was presented and 3 equations were created to calculate the evaluation criteria to estimate the costs of the circuit even before the design. Presenting the proposed unsigned and signed multiplier circuits in n×n sizes facilitated the use of the proposed designs in arbitrary sizes. Based on the results, all of the proposed designs exhibited the best results in terms of QC, as well as the number of CIs and GOs relative to previous works. In all the proposed designs discussed in this article, parity-preserving capability was incorporated into the circuits to prevent error occurrence. However, this implementation leads to an increase in circuit area and delay compared to non-parity-preserving circuits.

Authors Contributions
All authors have contributed equally to prepare the paper.

Availability of Data and Materials
The data that support the findings of this study are available from

Conflict of Interests
The authors declare that they have no known competing financialinterests or personal relationships that could have appeared toinfluence the work reported in this paper.

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