



A 12-bit Non-Uniform Sampling SAR ADC Using Switchable Sampling Frequency

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Original Research

Abstract

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In this study, a frequency-division based successive approximation register analog-to-digital converter (SAR ADC) with two tone input signals and 12-bit resolution is developed in 0.13 μ m CMOS technology. The sampling frequency is 24 KHz. The base of this concept is non-uniform sampling achieved by phase/frequency detectors, frequency divider blocks, and up/down thermometer counter. In this design, the power consumption of the data converter is significantly lowered without sacrificing the linearity of the system by decreasing the sample frequency when the input signal slows down, such as biological signals that do not change frequently. At a 1.2 V supply, a factor of merit (FOM) of fJ/conversion 6.95 is attained.

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Keywords: Analog-to-digital converter (ADC), Successive approximation register (SAR), Non-uniform sampling, Reduced frequency, Low power

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1. Introduction

With the growing demand for energy-efficient and high-speed electronics, the latest generation of ADCs follows the same trend. Analog-to-digital converters (ADCs) have become essential in wired and wireless communications, data storage, and numerous sensor-based applications, particularly in the healthcare sector. Common ADC architectures include delta-sigma, successive approximation, folding and concatenation, pipeline, and flash converters. Nyquist-rate converters offer improved area/power efficiency for medium- to high-resolution designs, despite requiring multiple active comparators. Successive approximation register (SAR) ADCs deliver high resolution while maintaining low power consumption. Their digital-heavy architecture further enhances efficiency, benefiting from advancing digital technology. SAR ADCs require several clock cycles for complete analog-to-digital conversion, which results in output delays[1][2][3][4][5][6]. A standard SAR ADC comprises three key components: a comparator, capacitive DAC (for

analog processing), and successive approximation register (for digital control). The SAR converter uses successive approximations to find the digital presentation of an analog input [7].

Recent decades have seen extensive research on power reduction in SAR ADCs. In optimized low-power uniform-sampling designs, each block's power contribution must be analyzed. Consequently, minimizing individual block power becomes essential for significant total power reduction [8].

The two-stage dynamic comparator described in [9] decouples the latch stage from the pre-amplifier stage. This technique significantly accelerates latch regeneration while decreasing comparator delay. However, its drawback stems from initiating the latch operation in the linear region of the input transistor, which degrades inter-stage gain and consequently elevates output noise and offset.

A bi-directional dynamic comparator eliminates pre-amplifier reset power by employing complementary NMOS/PMOS input pairs. In the initial pre-amplification phase, the PMOS pair charges the loads from ground to

$\frac{V_{DD}}{2}$, then seamlessly transitions to the NMOS pair to complete the process. This self-resetting action maintains initial load conditions without additional power expenditure [10].

A load-switching comparator with reconfigurable capacitor arrays achieves mismatch reduction by operating in either low-noise or low-power mode. The design shares input transistors between both configurations, significantly lowering offset mismatch. This approach enables correction through minimal LSB redundancy, eliminating the need for explicit offset calibration [11].

The proposed uniform switching technique reduces DAC power consumption by sampling signals on the capacitor upper plates while resetting the lower plates. This approach eliminates both MSB reconfiguration power and reset energy, requiring only single-side capacitor switching per conversion. While achieving 63% power reduction versus conventional designs, the technique constrains SAR linearity due to induced comparator performance variations (noise, offset, speed) [12].

An asynchronous SAR ADC timing scheme is presented in [13] that operates with only a set of global sampling clocks. The architecture internally generates all necessary timing signals for the comparator and DAC updating circuitry. While primarily designed for high-speed conversion, this approach also benefits low-power designs by requiring only a low-frequency system clock F_s , thereby minimizing clock generation and distribution power overhead.

An alternative low-power approach employs a novel non-uniform sampling technique in these converters.

Reference [14] analyzes a 180 nm CMOS SAR ADC employing non-uniform sampling at a maximum reference frequency of 40 MHz. The study leverages compressed sampling theory—enabling signal acquisition and reconstruction with fewer measurements than conventional Nyquist-rate methods (per Kotelnikov's theorem). Such systems, termed analog-to-information converters (AICs), comprise three core components: (1) a signal acquisition front-end, (2) an ADC, and (3) an information recovery backend. The AIC implementation employs a 16-bit SAR ADC operating at 1 MS/s, integrating: (1) a non-uniform sampling front-end, (2) an SAR-based conversion core, and (3) a GOMP algorithm for information recovery.

Simulations demonstrate 0.7% signal dispersion and 75 dB SFDR within a 20 MHz bandwidth using only 500 samples. However, the system lacks real-time processing capability due to computational complexity, requiring peripheral support and exhibiting elevated power consumption [15].

Reference [16] demonstrates a 2-subrange reconfigurable SAR ADC in 130 nm CMOS, achieving 5–14bit resolution with 13.5-bit maximum ENOB via non-subtractive dithering. The design employs: (1) an auxiliary segmented capacitor array with integrated switching logic, (2) non-uniform clock distribution, and (3) on-chip LMS-based perturbation calibration to mitigate capacitor mismatches, enhancing effective resolution by >10 dB. The ADC's resolution can be enhanced through SPI-controlled techniques including oversampling, non-subtractive dither [17], majority voting [18]. While the

capacitive implementation preserves code integrity and linearity while accelerating conversion, it necessitates additional comparison cycles and approximation steps.

Previous work developed a non-uniform sampling ADC architecture using intersection-level matching, with discrete analog components and an FPGA-based digital section. The design incorporates an IP core (implemented on an Altera Cyclone II FPGA) containing: (1) a quantization stage adaptation algorithm and (2) a level update algorithm.

The digital logic first generates initial crossover levels (reset state), then drives DACs to produce reference voltages for signal comparison. Then, it updates both quantization stages and crossover levels each clock cycle [19].

The proposed non-uniform sampling (NUS) ADC architecture incorporates a digital anti-aliasing (AA) filter to achieve combined voltage-time quantization, eliminating the need for conventional analog AA filters while maintaining compatibility with synchronous DSP systems. The digital implementation features a resettable, alias-free asynchronous filtering algorithm that processes time-stamped samples from parallel voltage and time quantizers. This algorithm simultaneously performs anti-aliasing and non-uniform-to-uniform sample conversion, with digital reconfigurability for response optimization. System performance is analyzed through comprehensive error modeling of voltage/time quantization noise, enabling precise characterization of theoretical limits and design trade-offs [20].

The system processes weak biological signals through pre-amplification and bandpass filtering before digitization using a successive-approximation non-uniform adaptive sampling ADC (SA-ADC). The proposed SA-ADC architecture incorporates a multiplexer, an N-bit adder, and a control logic block. The design requires two additional clock cycles per conversion to verify whether input signal variations exceed the threshold voltage V_{th} (determined by the SA-ADC). While enabling adaptive sampling, these extra clocks increase power consumption. For wireless transmission, the system employs a hybrid FSK/OOK transmitter [21].

These architectures demonstrate particular efficacy in medical applications, especially for processing signals with heterogeneous frequency characteristics and non-uniform power efficiency requirements.

We present a 12-bit SAR ADC employing non-uniform sampling at 24 kS/s, designed to address inherent noise and linearity constraints. The proposed architecture significantly reduces system power consumption through intelligent input clock frequency modulation.

The paper is organized as follows: Section 2 introduces the fundamental principles of the technique. Section 3 details the proposed SAR ADC implementation. Section 4 presents measurement results, and Section 5 provides concluding remarks.

2. SAR ADC Fundamental

2.1. Conventional SAR ADC

Successive approximation register (SAR) ADCs represent

one of the most efficient analog-to-digital conversion architectures, employing a binary search algorithm to approximate progressively the input signal. Through iterative comparison and refinement, the converter determines the optimal digital representation of the analog input, achieving high accuracy with minimal power consumption [22–24]. As noted, SAR ADCs comprise three key components: (1) an analog comparator, (2) a capacitive DAC, and (3) a digital successive approximation register. The conversion requires exactly N clock cycles to produce an N -bit digital output. Operation begins when the sample-and-hold circuit uniformly samples the input signal, which remains held for N comparisons. The register initializes with a mid-scale value (e.g., 100000000000 for 12-bit resolution) and progressively refines this estimate through binary search. The capacitive DAC converts the digital approximation to an analog voltage, which the comparator evaluates against the sampled input. A comparator output HIGH indicates the current bit trial (MSB-first) is valid, maintaining this '1' while setting the next significant bit to '1'. Conversely, a low output flips the current bit to '0' before proceeding to the next bit. This binary search iterates until completing the 12-bit conversion, as illustrated in the SAR ADC architecture schematic, Fig. 1 [25], [7].

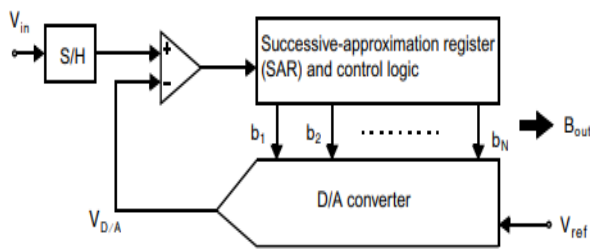


Figure 1. Conventional SAR ADC architecture [25]

2.2. The non-uniform sampling SAR ADC

Using switched input clock frequency while at higher clock frequencies improves bit resolution, they impose significant power trade-offs in the sample-and-hold circuit. To maintain stability at elevated frequencies, the operational amplifier requires:

- [1] Increased transconductance (g_m) through larger input transistors or higher bias currents.
- [2] Enhanced slew rate via greater output current.

These modifications introduce parasitic capacitances, necessitating larger compensation capacitors that paradoxically degrade slew rate. Consequently, designers must further increase bias currents to recover performance, leading to substantially higher power consumption in the sample-and-hold stage [26].

High-frequency operation significantly increases comparator power consumption. These circuits employ high-gain, uncompensated differential amplifiers optimized for speed, commonly used in SAR ADCs and oscilloscopes. Their fundamental limitation stems from continuous saturation biasing of input transistors to

maintain high gain, resulting in elevated static power dissipation. Comparator speed represents a critical design parameter, requiring both an adequate slew rate for high-frequency signal processing and fast settling time. To achieve this, transconductance (g_m) must be increased by using higher bias currents, which directly affects power consumption. Frequency reduction lowers current requirements, offering potential power savings. Notably, the digital-to-analog converter constitutes another major power contributor in the system.

Digital-to-analog converters (DACs) perform fundamental signal reconstruction by converting discrete digital code words into continuous analog voltages or currents with amplitude precision defined by their resolution. Their power consumption primarily stems from capacitor array switching activity. Frequency reduction decreases capacitor charging/discharging cycles, thereby reducing charge transfer between supply and ground. Consequently, lowering the sampling frequency emerges as an effective strategy for minimizing overall system power consumption [23].

For medical signals like ECGs, EEGs, and EMGs with prolonged quiescent or low activity periods, adaptive sampling significantly reduces power by lowering the rate during stable intervals. The sampling frequency (F_s) must satisfy two constraints: (1) $F_s < \frac{ADMCLK}{16}$ (where $ADMCLK$ is the SAR clock frequency and 16 represents the ADC resolution) to ensure complete bit conversion, and (2) $F_s > 2f_{max}$ (per Nyquist's theorem) to prevent aliasing, where f_{max} is the highest signal frequency component. Frequency domain analysis captures signal variations over extended durations. Many applications involve signals with prolonged silent periods punctuated by rapid transitions, making fixed Nyquist-rate sampling power-inefficient during quiescent intervals. Our method addresses this by segmenting signal analysis into two distinct frequency bands: (1) $\frac{F_s}{4}$ to $\frac{F_s}{2}$ (active band) and (2) below $\frac{F_s}{4}$ (silent band). The sampling frequency is adjusted dynamically between these bands to prevent aliasing while minimizing power.

A state machine circuit manages transitions between bands to maintain signal integrity. When maximum frequency components remain below $\frac{F_s}{4}$, oversampling is avoided, reducing power. While additional time frames could further decrease power consumption, this introduces circuit complexity that may offset the gains. Thus, an optimal trade-off exists between power reduction and implementation complexity. The proposed technique employs a Schmitt trigger and phase-frequency detector (PFD) to adjust dynamically the sampling frequency based on input signal characteristics. As shown in Fig. 2, the system compares the input signal frequency (after Schmitt triggering) against a reference clock at $\frac{F_s}{4}$ (where F_s is the base sampling frequency, equal to $\frac{1}{n}$ of the digital SAR clock frequency). There are three main sources of power consumption in SAR ADCs: analog power dissipated on OPAMPs and biasing circuits, digital power consumed on the Successive Approximation Register as digital circuit, and mixed power burned on comparators as mixed-mode

circuits.

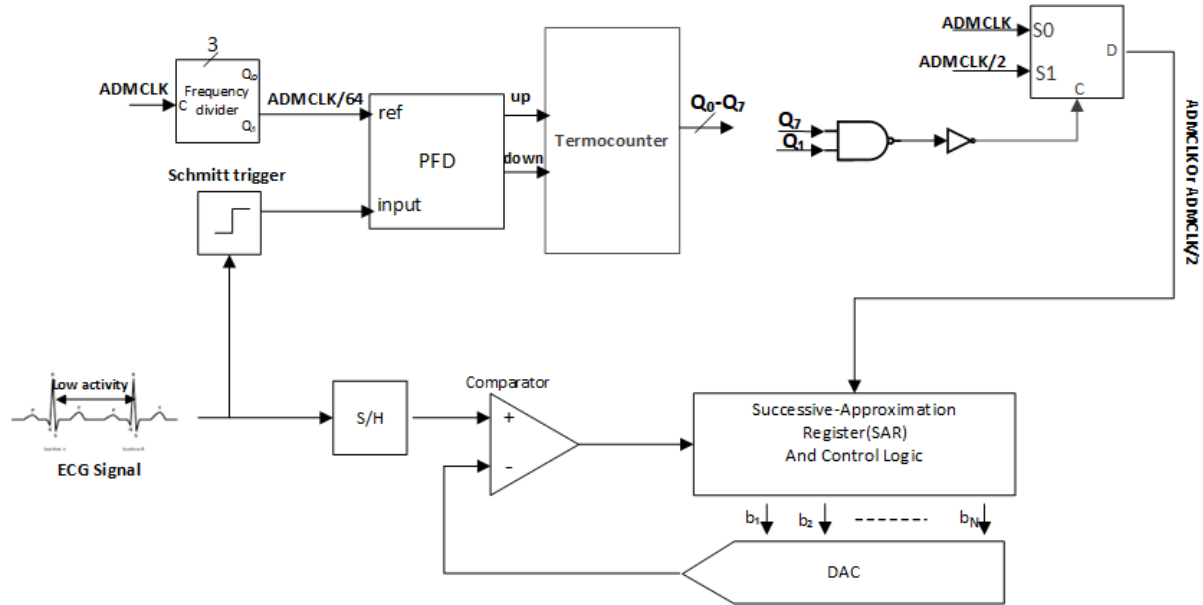


Figure 2. Block diagram of the proposed SAR ADC.

A. Analog power dissipation

Operational amplifiers contribute significantly to overall power dissipation, with consumption categorized as static and dynamic components. The static power required for biasing the analog circuitry remains frequency-independent but must increase to support higher-frequency operation. Dynamic power arises from the charging and discharging of capacitors at both output and internal nodes and is directly proportional to the signal frequency. Consequently, reducing operating frequency decreases dynamic power consumption while maintaining the static power floor.

B. Digital power consumption

SAR ADCs and their digital control circuits predominantly exhibit two power consumption components: static and dynamic. Static power, resulting from transistor leakage currents during idle states, typically represents a minor fraction (< 5%) of total digital power consumption in modern CMOS processes. Dynamic power represents the main component of power consumption and consists of two elements: the power used for charging and discharging internal nodes and the capacitive output loads, and the short-circuit power dissipated at zero-crossing points or during transitions between zero and V_{DD} . Reducing the frequency of $ADMCLK$ decreases dynamic power consumption. The equations for dynamic power and short-circuit power are as follows:

$$P_D = C_{eff} \times V_{DD}^2 \times f \quad (1)$$

$$P_{sc} = \frac{\beta}{12} \times (V_{DD} - 2V_T)^3 \times \frac{\tau}{T} \quad (2)$$

Here, β is the gain-factor of the transistor: $\beta = \frac{\mu \epsilon W}{L t_{ox}}$

V_T is the threshold voltage, and τ is the input transition time $T = 1/f$.

C. Mixed-mode power dissipation

Comparators exhibit mixed-signal power dissipation, combining analog static power and digital dynamic power. Dynamic comparators, while power-efficient, suffer from kickback noise, making them unsuitable for high-resolution applications (e.g., 10–16bit SAR ADCs). In such cases, static comparators are preferred despite higher power consumption because they ensure precision matching the ADC's resolution. This trade-off makes static comparators dominant in high-resolution Nyquist-rate ADCs. This study employs Auxiliary Latch comparator design optimized for both low-power operation and high-speed performance. The proposed technique uses an Auxiliary Latch to boost the pre-amplifier gain during initial comparison, enhancing comparator sensitivity. This innovation reduces the required comparator count for target resolution, thereby lowering total power consumption. Fig. 3 illustrates the block diagram of the Auxiliary Latch circuit. The suggested comparator design includes two pre-amplifier stages followed by a standard latch stage. The first pre-amplifier stage features a distinct design utilizing diode-connected loads and cross-coupled latch transistors (M_{L3} and M_{L4}) to achieve maximum voltage gain during the initial evaluation phase, building upon established techniques from prior research. The second stage maintains a standard latch configuration for signal regeneration. The conventional architecture exhibits instability due to uncontrolled negative resistance at output nodes. The proposed comparator addresses this through an innovative auxiliary latch (transistors M_{L1} and M_{L2}) that ensures stable voltage gain without additional power overhead. As shown in the schematic, this latch configuration simultaneously enhances dynamic performance by reducing propagation delay and improving response characteristics during the critical initial evaluation phase.

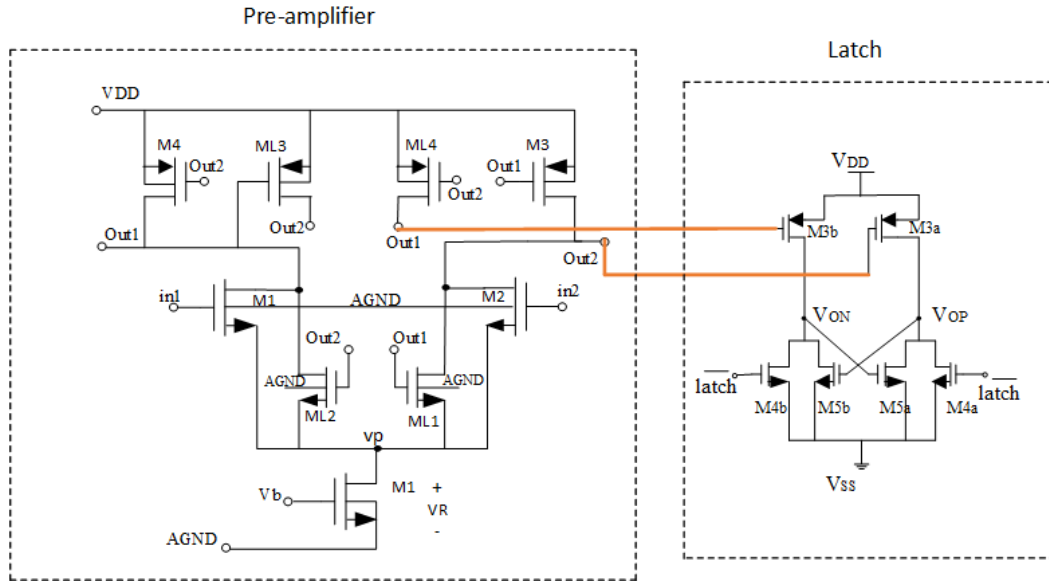


Figure 3. Schematic of the static comparator

At high frequencies, rapid input signal variations force more frequent comparator switching, increasing dynamic power consumption. This is exacerbated by short-circuit currents during transitions when both pull-up and pull-down networks briefly conduct simultaneously, creating additional power dissipation paths. At elevated frequencies, comparator bias conditions shift, leading to increased leakage currents.

While bias non-idealities primarily affect analog circuits, they contribute substantially to total power in high-speed comparators. Consequently, reducing operating frequency directly reduces ADC power consumption by mitigating both dynamic switching and leakage components.

Fig. 4 illustrates the switched clock frequency architecture. Biological signals like ECGs exhibit non-uniform spectral activity—prolonged quiescent periods (e.g., between QRS complexes) require less frequent sampling than rapid transitions (e.g., during depolarization). Fixed Nyquist-rate sampling wastes power during these low-activity intervals. This work aims to minimize power while maintaining 12-bit resolution and constraining dynamic errors through adaptive clocking.

3. Effect of clock frequency switching and comparator characteristics

Clock frequency and new comparator characteristics effect on resolution and performance of the proposed ADC. In this section, the effects of the phenomena would be considered and modeled.

3.1. Conventional SAR ADC

To analyze the effect of clock frequency switching (between f_s^{max} and $f_s^{max}/2$) on jitter we need to examine the switching mechanism and noise sources.

This analyzes involves the following steps:

a. Clock frequency switching model

- Our system has a two-state clock frequency switch:

State1:

$$f_s = f_s^{max} \quad (e.g., 1kHz). \quad (3)$$

State2:

$$f_s = \frac{f_s^{max}}{2} \quad (e.g., 500Hz). \quad (4)$$

- Switching is triggered based on the estimated input signal frequency.
- Switching times (t_{switch}):

$$t_{switch} = \left\{ t \mid f_{in}(t - \tau_{PFD}) \text{ crosses } \frac{f_s^{max}}{4} \right\} \quad (5)$$

- Instantaneous frequency change:

$$f_s(t) = \begin{cases} f_s^{max} & \text{if } f_{in}(t - \tau_{PFD}) \geq \frac{f_s^{max}}{4} \\ \frac{f_s^{max}}{2} & \text{otherwise} \end{cases} \quad (6)$$

b. Sources of jitter in frequency switching

The main sources that contribute to jitter in the system are Switching-Induced Jitter, Sudden frequency changes cause phase discontinuities, derived as follows:

When switching between f_s^{max} and $\frac{f_s^{max}}{2}$, the clock phase abruptly shifts. The phase shift could be modeled as phase step:

$$\Delta\phi = 2\pi \cdot \left(\frac{1}{f_s^{max}} - \frac{1}{\frac{f_s^{max}}{2}} \right) = -\frac{2\pi}{f_s^{max}} \quad (7)$$

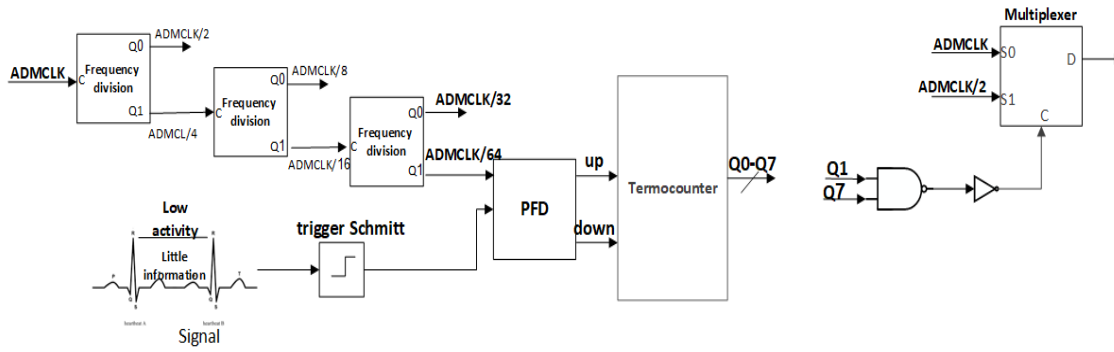


Figure 4. Switched input clock frequency.

Consequently, the step introduces timing jitter as:

$$\Delta t_j = \frac{\Delta \phi}{2\pi f_s} = \frac{1}{f_s^{\max}} - \frac{1}{\frac{f_s^{\max}}{2}} = -\frac{1}{f_s^{\max}} \quad (8)$$

To reduce jitter from frequency switching, Smooth Frequency Transitions would be used by replacing abrupt switches with linear frequency ramps as follows:

$$f_s(t) = f_s^{\text{old}} + \alpha \cdot t \quad (9)$$

where α is the ramp slope of changing frequency at the transition time.

3.2 Effect of Comparator Characteristics on Resolution

It is introduced the Mathematical Modeling of Comparator Noise and Offset Effects in Non-Uniform Sampling SAR ADCs is introduced as follow. The comparator in the SAR ADC introduces two key non-ideal characteristics: the Input-referred offset voltage (V_{OS}) which is a fixed DC voltage offset that shifts the decision threshold (Typically ranges from 0.5-5 mV) and thermal noise (V_n), random voltage fluctuations modeled as a Gaussian distribution:

$$V_n \sim \mathcal{N}(0, \sigma_n^2) \quad (10)$$

Where σ_n is the RMS noise voltage (typically 0.1-1 mV), so the Decision Equation of Modified Comparator is rearranged as follows: For each conversion step i ($1 \leq i \leq N$ bits), the effective input voltage becomes:

$$V_{comp}^{(i)} = V_{in}[k] - V_{DAC}^{(i)} + V_{OS} + V_n^{(i)} \quad (11)$$

where $V_{in}[k]$ is the sampled input voltage at time k , $V_{DAC}^{(i)}$ is the DAC output voltage at step i , and $V_n^{(i)}$ is the instantaneous noise value at step i . As a result, the bit decision is made by:

$$b_i = \begin{cases} 1 & \text{if } V_{comp}^{(i)} \geq 0 \\ 0 & \text{otherwise} \end{cases} \quad (12)$$

There are four components for total error at the output of

ADCs, introduced as:

$$\epsilon_{total} = V_{OS} + V_n + \epsilon_j + \frac{\Delta}{2} \quad (13)$$

V_{OS} : offset

V_n : noise

ϵ_j : Jitter

$\frac{\Delta}{2}$: Quantization

where, ϵ_j is sampling time jitter effect and Δ shows LSB voltage ($\frac{V_{ref}}{2^N}$). So the RMS error is calculated as:

$$\epsilon_{RMS} = \sqrt{V_{OS}^2 + \sigma_n^2 + \sigma_j^2 + \frac{\Delta^2}{12}} \quad (14)$$

For maintaining N-bit accuracy, the Noise and Offset must be limited as Eq (15) and Eq (16), respectively.

$$\sigma_n < \frac{\Delta}{4\sqrt{2\ln 2}} \approx \frac{V_{ref}}{2^{N+2}} \quad (15)$$

$$V_{OS}^{max} = \frac{\Delta}{2} = \frac{V_{ref}}{2^{N+1}} \quad (16)$$

4. The proposed SAR ADC circuits

As introduced earlier, the proposed non-uniform sampling technique adaptively reduces the sampling frequency during signal intervals lacking high-frequency content Fig. 3. The system operates as follows: (1) A Schmitt trigger performs edge detection on the input signal, (2) the phase-frequency detector (PFD) evaluates temporal variations, and (3) a thermo-encoded counter with logic control selects the optimal sampling frequency. This hierarchical approach minimizes power consumption while preserving signal integrity. The basic blocks used in this section are a frequency divider, a phase-frequency detector, a thermometer counter, and a logic control circuit.

4.1. Frequency Divider (FD)

Frequency dividers (FDs) are essential components in high-speed analog/RF and digital systems, especially for generating subharmonics from high-frequency references. For example, PLL-based frequency synthesizers, clock generators, and time-interleaved analog-to-digital converters can be mentioned [27-31]. There are three types of frequency dividers (FDs): regenerative FDs (RFDs), flip-flop-based FDs (FF-FDs), and injection-locked FDs (ILFDs) [32-35]. RFDs and ILFDs not only operate in a narrow frequency range, but they also take up a lot of space on the chip due to their excessive use of passive components [36].

Flip-flop based frequency dividers (FF-FDs) typically employ a master-slave closed-loop architecture. These circuits generate frequency division by toggling their output state (between logic 1 and 0) at each clock transition, effectively producing an output signal at half the input clock frequency ($\frac{F_{in}}{2}$). This fundamental divide-by-2 operation forms the basis for more complex frequency synthesis [37]. The frequency divider architecture, shown in Fig. 5, employs a D-flip-flop and a multiplexer to generate clock signals for various circuit blocks. This fundamental divide-by-2 cell can be cascaded to achieve higher division ratios, enabling flexible frequency synthesis across the system.

4.2. Phase-Frequency Detector (PFD)

As shown in Fig. 6, the phase-frequency detector (PFD) compares the reference clock (F_{ref}) with the feedback clock ($F_{feedback}$), generating UP and DOWN control signals based on their phase/frequency relationship. The PFD activates:

- UP when $F_{feedback}$ lags F_{ref} (requires frequency increase)
- DOWN when $F_{feedback}$ leads F_{ref} (requires frequency decrease) [38, 39]

This bang-bang control mechanism drives the system toward phase lock by correcting both frequency and phase mismatches. The frequency-difference detector employs two D flip-flops and a NAND gate, with the gate's output connected to the flip-flops' reset inputs (R) and its inputs fed from the Q outputs. This digital implementation suffers from a dead-zone limitation; when input phase differences approach zero, the parallel logic generates vanishingly narrow pulses. A common solution inserts a deliberate delay in the detector's reset path, ensuring minimum pulse width for reliable operation.

4.3. Thermometer-coded counter

Counters serve as fundamental building blocks in measurement systems, ADCs, frequency dividers, and PLL synthesizers. Modern applications require extended-range counters with size-independent counting

rates, yet face a fundamental trade-off: larger bit-widths introduce propagation delays during low-to-high-order bit transitions, limiting maximum speed. Synchronous binary counters address this issue by clocking all flip-flops simultaneously, ensuring stable outputs and predictable latency, though this leads to greater routing complexity [40]. A counter is made up of multiple cascaded flip-flops and can be categorized into two types: synchronous and asynchronous. Only the first stage flip-flop. The counter speed falls because of the extended propagation delay. However, because of the lower propagation delay with synchronous counters, the clock signal is applied to every flip-flop at once, which does not affect the counter speed [41]. Combinational logic and memory components make up synchronous counters. However, because of counting down (initial state less than temporary state), growing (initial state more than temporary state), or occasionally increasing/decreasing, the counters are separated into up-counter, down-counter, and up/down-counter types. Combining two counters, the up/down counter causes the clock output to occasionally rise and fall.

Flop in an asynchronous counter receives the clock, and its output is linked to the clock of the subsequent stage flip-flop.

This article discusses a counter with an up/down thermometer-coded mechanism. A thermometer is employed to toggle bits between one and zero, and due to the input frequency's potential to fluctuate, an increment/decrement counter is utilized. An 8-bit counter is chosen since counters exceeding 8 bits consume more power due to high clocking, while those below 8 bits lack sufficient reliability for frequency adjustments. The multiplexer employs a state machine with a straightforward algorithm to choose between $ADMCLK$ or $\frac{ADMCLK}{2}$. If both Q_1 and Q_2 are one, $\frac{ADMCLK}{2}$ is selected; otherwise, $ADMCLK$ is chosen for all other states. Fig. 7 illustrates the state machine for this algorithm. The state machine circuit ensures antialiasing is avoided during transitions between two sample frequencies as follows:

when the input frequency is below a quarter of the sample frequency, the state machine lowers the sample frequency and $ADMCLK$ after one cycle of F_S ($\frac{ADMCLK}{16}$). If the input frequency falls between $\frac{F_S}{2}$ and $\frac{F_S}{4}$, the sampling frequency and $ADMCLK$ are rapidly increased.

5. Result and discussion

To evaluate the performance of analog-to-digital converters comprehensively, it is essential to articulate the errors associated with the input signal's sampling and frequency. This section examines the key performance criteria for the proposed converter.

SNR is equal to the ratio of signal power to noise power at the output Eq (17):

$$SNR = \frac{P_{sig}}{P_{noise}}, SNR(dB) = 6.02N + 1.76 \quad (17)$$

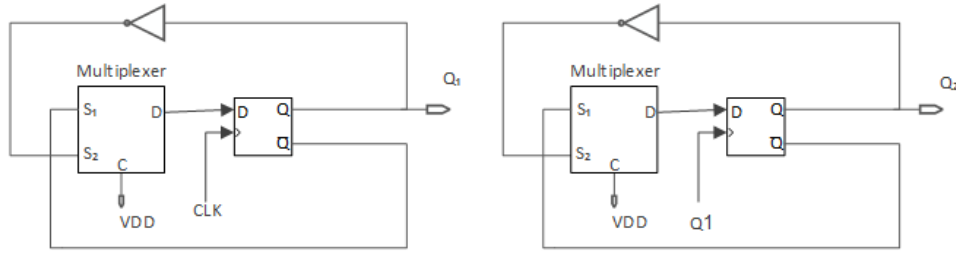


Figure 5. Frequency divider.

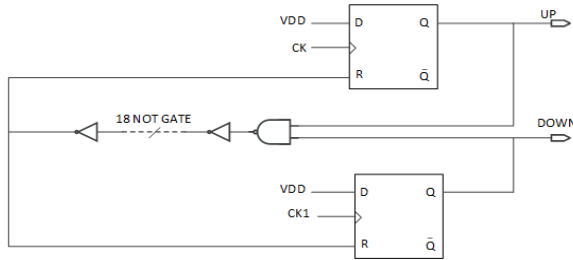


Figure 6. Phase-frequency detector.

Where N is the resolution of the converter.

SNDR is equal to the ratio of signal power to the sum of noise power and harmonic power Eq (18):

$$SNDR = \frac{P_{sig}}{P_{noise} + P_h} \quad (18)$$

SFDR is equal to the ratio of the signal power to the maximum harmonic power at the output of the converter Eq (19):

$$SFDR = \frac{P_{sig}}{P_{hmax}}, \quad SFDR_{bits} = \frac{SFDR(dBc)}{6.02} \quad (19)$$

ENOB indicates the number of effective bits of the converter Eq (20):

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (20)$$

Another key metric is the Figure of Merit (FOM), commonly used to compare the performance of various analog-to-digital converters. This parameter reflects the efficiency of a converter's power consumption under equivalent conditions. Equivalent conditions refer to eliminating the influence of the converter's accuracy and speed on its power consumption.

$$FOM = \frac{Total\ Power}{2^{ENOB} \times 2 \times BW} \quad (21)$$

Where the power is the conversion power and BW is the bandwidth of the signal.

The analog-to-digital converter (ADC) is a successive approximation register with switched frequency at the input clock, implemented in 0.13μm CMOS technology with a 1.2V supply voltage. Fig. 8 illustrates the ADC's frequency spectrum across the TT process corner for two-tone input signals at 11.2625 kHz and 11.239 kHz. Fig. 9

presents the DNL and INL for the proposed technique in the TT corner, showing variations of less than 0.81 LSB for DNL and 1.5 LSB for INL, measured with a full-scale single-tone Nyquist rate sine wave at the input. The results would be achieved without utilizing any calibration technique, such as reported in [42].

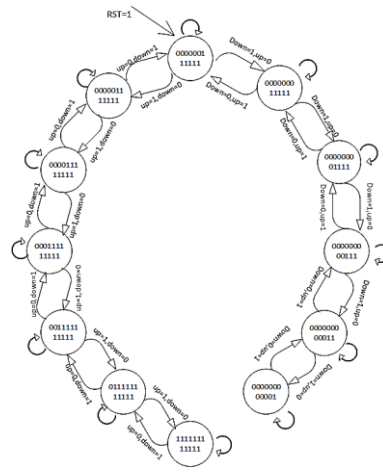


Figure 7. State transition diagram of a synchronous up/down-counter.

Table 1 compares the conventional SAR ADC with the proposed non-uniform sampling technique across three process corners. As shown, the SFDR and SNDR are slightly lower than the conventional SAR ADC, and further decrease in the SS corner due to reduced headroom voltage. In the SS corner, the increased transistor threshold voltage lowers transconductance and biasing current, which impairs the linearity of OPAMPs and comparators while reducing the ADC's power consumption. As indicated in Table 1, the elevated threshold voltage in the SS corner decreases the DNL and INL of the proposed non-uniform sampling technique. This degradation stems from slower comparators and MOS switches in the capacitive DAC, but it remains acceptable. The proposed approach lowers power consumption by approximately 25% compared to the conventional SAR ADC. Power measurements in all tables are based on a high-rate ECG signal (150 bpm) as the input to the proposed ADC, with further power savings expected at lower ECG signal rates. Table 2 compares the proposed SAR ADC with other works based on three criteria: technology, Figure of Merit (FOM), and power consumption. The proposed design demonstrates the lowest power consumption. For a fair comparison, the FOM defined earlier in the section is used, and the

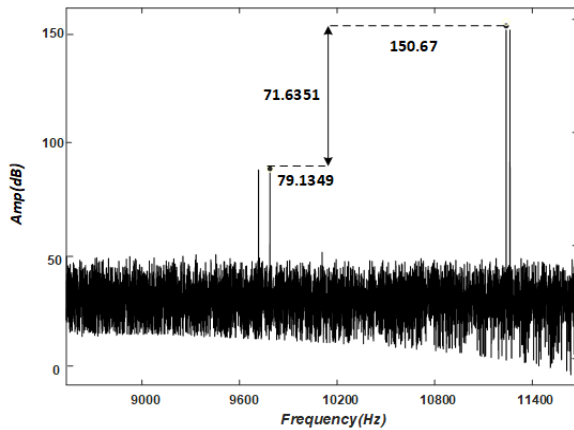


Figure 8. Output spectrum in two-tone Test at the TT corner of the process.

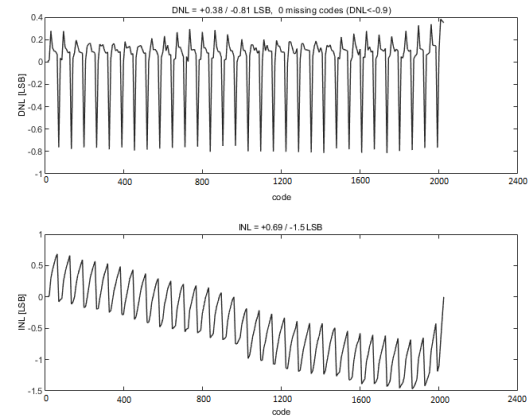


Figure 9. Simulated DNL and INL of the proposed SAR ADC.

proposed technique's FOM surpasses that of other works following reference [43].

All simulation results were obtained by applying a two-tone Nyquist rate sine wave to the ADC's input.

6. Conclusion

A 12-bit non-uniform sampling SAR ADC with switched input clock frequency, implemented in 0.13 μ m CMOS technology, is presented. This article introduces a novel non-uniform sampling technique to lower power consumption in a SAR ADC while preserving key

performance metrics, such as linearity and ENOB. The proposed method reduces power by decreasing the sampling frequency when the input signal exhibits slow variations, making power savings dependent on signal activity. For a high-rate ECG signal (150 bpm), power dissipation is reduced by approximately 25%. A key advantage of the design is the use of a single reference clock across circuit components, which, alongside the proposed technique, further minimizes system-wide power consumption. Additionally, a simple state machine algorithm reduces operating frequency, maintaining low circuit complexity.

Table 1. Comparison of our SAR ADC with conventional SAR.

	SNDR	SFDR	ENOB	Power consumption (μ Watt)	FOM fJ/conversion step	DNL (bits)	INL (bits)
Conventional SAR ADC	67.6892	72.456	10.95169	0.373	7.85	0.7	1
FF	67.1099	72.0589	10.85547	0.325	7.31	0.7	1.05
TT corner of the proposed architecture	66.3495	71.6351	10.72915	0.283	6.95	0.81	1.5
FS corner of the proposed architecture	65.8962	70.4358	10.65385	0.260	6.72	1.08	1.6
SF corner of the proposed architecture	65.3997	69.2476	10.57138	0.245	6.71	1.17	1.62
SS corner of the proposed architecture	64.9733	67.3721	10.50055	0.216	6.21	1.3	1.67

Table 2. Comparison with other works.

	Technology	Supply(v)	SNDR	Sampling frequency (Hz)	FOM fJ/conversion step	Resolution (bits)	Power consumption (Watt)
This Work*	130 nm	1.2	66.3495	24 K	6.95	12	0.283 μ
[44]	130 nm	1.2	79.2	28.6 K	59	14	130 μ
[15]	180 nm	1.8	75	40 M	17.7	16	34 m
[43]	40 nm	1	64.1	6.4 M	5.5	13	46 μ

*This work is about simulation, and it is compared with the post-construction results of other articles.

Authors Contribution

All the authors have participated sufficiently in the intellectual content, conception and design of this work or the analysis and interpretation of the data (when applicable), as well as the writing of the manuscript.

Availability of data and materials

The data that support the findings of this study are available from the corresponding author, upon reasonable request.

Conflict of interests

The author states that there is no conflict of interest.

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