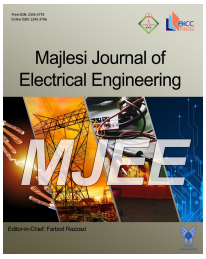

Volume 18, Issue 3, 182443 (1-10)

Majlese Journal of Electrical Engineering (MJEE)

https://dx.doi.org/10.57647/j.mjee.2024.180343

Three phase 7-level switched-capacitor inverter with minimum switching components

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Original Research

Received:
16 April 2024
Revised:
1 June 2024
Accepted:
11 June 2024
Published online:
3 September 2024

Abstract:

This research presents a new three-phase switched capacitor multilevel inverter (*SCMLI*) with a power enhancement capability. The structural design comprises six switches, two diodes and two capacitors to achieve a voltage gain of three times. Inherent self-balancing of capacitor voltage reduced active/passive part count, and the ability to generate bipolar output voltage without an H-bridge at the back end are the important aspects of the suggested topology. A concise description of the structural design, basic operation, determination of capacitance, and power loss analysis has been presented, along with comparisons with recent previous topologies. To regulate the switching process, a basic level-shift PWM modulation strategy has been designed. The simulation and hardware studies demonstrate the feasibility and efficacy of the proposed topology (PT).

Keywords: Component count per level; Gain; MLI; Self-balancing; TSV; MBV

1. Introduction

Nowadays, multilevel inverters (MLI) play an essential role in power conversion in low, medium, and high voltage applications such as acting as an interconnecting medium for electric vehicles (EVs), microgrids, distributed generation systems (DG), etc. Multilevel inverters are preferred over traditional inverters because of the following advantages; lower harmonic distortion, improved waveform, lower dv/dt, lower electromagnetic interference operating at a lower switching frequency, and many more [1].

Well-known and frequently used MLI topologies include the neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) topologies. These topologies have seen widespread use in numerous implementations across the energy storage and electrical conversion fields. Balanced charging of DC link capacitors is a relative issue that was mainly brought about by NPC and FC inverters. Multiple DC voltage sources are required by the CHB design to produce higher-level output. Furthermore, the number of semiconductor components needed for these conventional topologies grows linearly with the number of output levels. Because of these various circumstances, one of the most important priorities right now is to reduce the total number of semiconductor components and passive parts. This results in a reduction in the overall system's size and weight, as well as a reduction in the system's conduction and switching losses, and an increase in the system's overall efficiency [2, 3].

In contrast to the commercialization of NPC, FC, CHB, and MMC in medium- and high-voltage applications, SC-based MLIs (SCMLIs) have primarily found utility in low/high voltage applications due to their inherent advantages such as voltage-boosting capability and self-balanced capacitor voltages. Consequently, SC architecture has garnered increased attention from researchers in recent years for its potential to enhance input voltage, eliminate switching components, and reduce DC source requirements, making it a significant innovation. As a result, researchers have shifted their focus towards switched capacitor multilevel inverter (SC-MLI) topologies, which are classified as single-stage or two-stage configurations.

As a solution to the aforementioned problems associated with traditional inverters, the research community has presented several novel works to minimize part count to obtain the maximum voltage level. The article [4] gives an out-

standing idea to generate a multilevel waveform by using switched DC sources. The authors in [5] are concerned with lessening the number of components used in multilevel topologies. Three-phase MLI configuration in [6, 7] uses fewer component counts per level. This converter has two parts, one for positive polarity voltage other for negative polarity voltage. In [8], a SC MLI with a cross connection is presented that uses fewer switches to increase the output voltage. Hybrid modular topology [9] reduces the number of components count to achieve a higher level. Nonetheless, more DC voltage sources are needed for further voltage levels. This makes it more complex as well as expensive. In [10], a three-phase modular symmetrical multilevel inverter is described, which uses fewer power electronic components at higher voltages while subjecting all of the switches to the same voltage stress. A phase's symmetrical modular structure with reduced device count per level is proposed [11]. However, the drawbacks of getting multiple levels of voltage, by using several components, and voltage sources make these topologies complex and costly. Henceforth, the researcher concentrated on switched capacitor topology to minimize the isolated DC sources and components.

There are fewer switching components and power supplies required for an SC inverter to generate several voltage levels. The SC unit can be cascaded together to form a new switched capacitor topology which can produce increased voltage levels. Moreover, the improved waveform can be obtained by series-parallel combinations of switches with the input source and switched capacitors. Additionally, the switched capacitor inverter topology is more flexible, and it doesn't require any transformer or inductor to boost the output voltage. When transformers or inductors are used the inverter becomes bulky and heavy [12, 13]. The utilization of a bridge network within cascaded multilevel inverters serves the purpose of doubling the voltage level, making it adaptable for both symmetrical and unsymmetrical configurations [14]. Nonetheless, the literature review mentioned earlier highlights certain limitations in achieving multiple voltage levels through the use of numerous components and voltage sources, which ultimately render these topologies intricate and expensive. Therefore, the researcher has shifted their focus towards employing a switched capacitor topology as a means to reduce the reliance on isolated DC sources and components. The switched capacitor inverter has the capacity to generate multiple voltage levels with fewer switching components and power requirements. Interconnecting these SC units enables the creation of an innovative switched capacitor topology with the ability to generate an extended spectrum of voltage levels. By employing series-parallel combinations of switches with the input source and switched capacitors, superior waveform quality can be achieved. Furthermore, the capacitors within the switched capacitor topology are inherently self-balanced and prove to be more efficient in terms of Total Harmonic Distortion (THD) [15, 16]. In recent years, a three-phase design based on the SC method has gained popularity for medium-power applications since it retains most of the benefits of its parent topologies [17]. The benefits of a new seven-level inverter architecture for three-phase applications, including reduced conduction losses and excellent efficiency, are reported in [18]. In [19, 20], a new T-type ANPC with built-in voltage regulation and enhancement is introduced. In [21], an ANPC with 9 levels of unit gain is presented. As depicted in reference [22], a novel three-phase SCMLI architecture is currently under development for a renewable energy conversion system. This proposed MLI design is characterized by its modular construction, allowing for the connection of multiple source modules to produce a higher number of output pole voltage levels.

To increase the input voltage, the switch boost inverter makes use of the voltage source inverter's shoot-through state [23]. A novel topology for converters used to power conversion [24, 25]. However, these topologies uses more switches and has high TSV. A novel asymmetrical modular multilevel converter (A-MMC) configuration employing mixed-cell (SM) technology, featuring DC-side fault-blocking capability and a streamlined component count, has been introduced [26]. The mixed-cell submodule integrates both a full-bridge (FB-SM) and a half-bridge (HB-SM), leveraging asymmetric capacitor voltage determined by geometric propagation (GP) ratio. In [27], a direct power control (DPC) approach inspired by neuronal principles is implemented for a wind energy generation system employing a doubly fed induction generator (DFIG). In reference [28], a novel 3-phase SCMLI design, aimed at step-up operation, is presented. This topology boasts reduced switch count and minimized voltage stresses. In [29, 30], an economically viable three-phase triple-gain switched-capacitor (SC) inverter configuration is introduced. This innovative design features a structural layout with a single source and is capable of producing a seven-level line-to-line output voltage waveform while utilizing minimal switching components.

This study introduces a novel three-phase MLI design capable of amplifying the input voltage while minimizing switching components and reducing voltage stress, addressing the aforementioned concerns. Key distinguishing attributes of the proposed configuration include:

1. Incorporation of voltage-boosting capability within the topology.
2. Inherent self-balancing of capacitors.
3. Reduction in voltage stress across the switching components.
4. Utilization of a single DC source for generating seven-level (line-to-line) voltages.
5. Minimization of the number of switches required for any level of voltage generation.
6. Operational adaptability across a broad spectrum of power factors.
7. Introduction of a suggested topology leading to a lower TSV, thereby contributing to overall cost reduction.

A summary of the suggested article's structure may be found next to this paragraph. Structure, operation, and optimum capacitance values are discussed in section 2. In section 3, a modulation method for the switching operation has been discussed. The PT's power loss analysis has been discussed in section 4. Section 5 includes simulation and experimental verification of the novel topology. In section 6, a compara-

tive comparison between the PT and the existing topology has been performed. The last part of this article contains the summary of the novel's work, which serves as its conclusion.

2. Proposed three-phase SC topology

2.1 Description of structural design

The proposed three-phase SCMLI structural design is depicted in Fig. 1. It comprises six power semiconductor switches (transistor along with anti-parallel diode), Two auxiliary passive power diode, D_{X1}, D_{X2} two capacitors C_{X1}, C_{X2} per phase leg X ($X \in R$, Y, B).A single unit of DC supply (V_{DC}) is used for this PT which may be obtained from a fuel cell, battery, and PV (photovoltaic) cell. To prevent a possible short circuit with the power source, power switches S_{X1} and S_{X2} operating at complimentary mode. The PT synthesizes 7-level (0, $\pm 1V_{DC}$, $\pm 2V_{DC}$, $\pm 3V_{DC}$) line-to-line output voltage waveform at the load terminal. Switching states for each phase-leg R are shown in Table 1. Where "1" and "0" illustrate the ON and OFF states of the switches respectively. The $V_{RO}(t)$ indicates the pole voltage between the phase "R" and "O". Capacitor's charging and discharging effects are symbolically represented as ▲&▼ respectively. Depending on the mode of operation, a red or green dotted arrow line indicates the charging path for the capacitors and the load current respectively.

2.2 Operation principle

The operation principle for the phase leg Ris discussed below for a better understanding.

$$\text{Mode1}.V_{RO}(t) = 0$$

In this mode, the pole voltage $V_{RO}(t) = 0$ can be achieved when the switches S_{R1}, S_{R3}, and S_{R5} are turned off and S_{R2}, S_{R4}, and S_{R6} are turned on simultaneously. When the switches S_{R2} and S_{R4} are in the ON position, both the capacitors C_{R1} and C_{R2} are charged up to V_{DC}. Since both the capacitors are connected in parallel with the DC supply along with the series-connected auxiliary diode D_{R1} and D_{R2}. The circuit representation is shown in Fig. 2 (a).

$$\text{Mode2}.V_{RO}(t) = 1V_{DC}$$

In this mode, the pole voltage $V_{RO}(t) = 1V_{DC}$ can be achieved, when the power switches S_{R2}, S_{R4}, and S_{R5} are turned on, while the power switches S_{R1}, S_{R3}, and S_{R6} are turned off simultaneously. Due to the turn-on of the switches S_{R2}, and S_{R4} both capacitors are charged up to V_{DC}. The circuit representation is shown in Fig. 2 (b).

$$\text{Mode3}.V_{RO}(t) = 2V_{DC}$$

In this working mode, pole voltage $V_{RO}(t) = 2V_{DC}$ can be obtained when the switches S_{R2}, S_{R3}, and S_{R5} are turned on and S_{R1}, S_{R4} and S_{R6} are turned off simultaneously. The capacitors C_{R1} charge up to V_{DC}, and C_{R2} discharge its stored energy along with the supply voltage V_{DC} to give $2V_{DC}$ at its output. The circuit representation is shown in Fig. 2 (b).

$$Mode4.V_{RO}(t) = 3V_{DC}$$

During this mode of operation, the pole voltage $V_{RO}(t) = 3V_{DC}$ can be achieved when the switches S_{R1}, S_{R3}, and S_{R5} are turned on and other switches S_{R2}, S_{R4}, and S_{R6} are turned off simultaneously. The capacitors (C_{R1}, C_{R2}) discharge either stored energy along with the DC supply to achieve $3V_{DC}$. The circuit representation is shown in Fig. 2 (b).

2.3 Design guideline of capacitance

The capacitor plays a significant role in the DC/AC switched capacitor converter. Therefore, the values of capacitance C_X of the PT should be properly chosen so that the efficiency of the inverter will be high. Peak values of load current, longest discharging period, and phase angle between load voltage and current all have an impact on the maximum rate of capacitor discharge. A maximum permissible voltage ripple limit can be calculated by using the load current and the discharging period to determine the values of capacitance. This value of maximum voltage ripple should not be more than 10% of its maximum voltage rating. Under unity power condition the voltage ripple value is more which confirms in all other loading conditions i.e. either inductive or capacitive load this value of voltage ripple is small [17]. From Fig. 3 the values of t_1, t_2, t_3, t_4 can be calculated as follows [18];

$$t_1 = \frac{\sin^{-1}(\frac{1}{3})}{2\pi f_S} \tag{1}$$

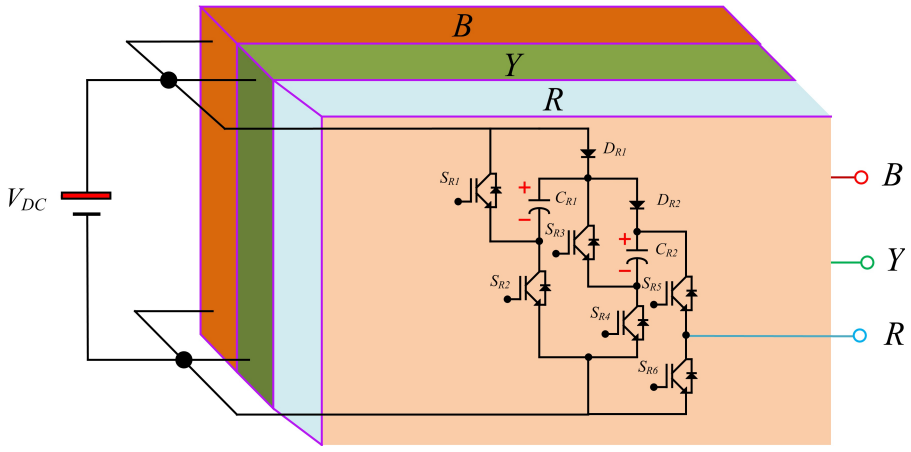

Figure 1. Circuit arrangement for Proposed 7-level SCMLI topology.

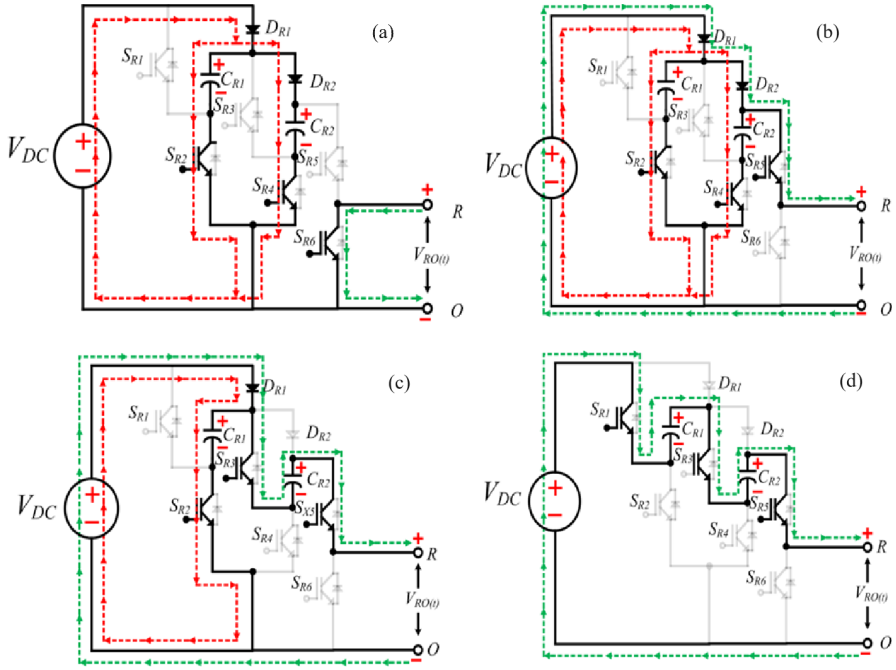

Figure 2. Equivalent circuit representation for (a) $V_{RO}(t) = 0$, (b) $V_{RO}(t) = 1V_{DC}$, (c) $V_{RO}(t) = 2V_{DC}$ (d) $V_{RO}(t) = 3V_{DC}$.

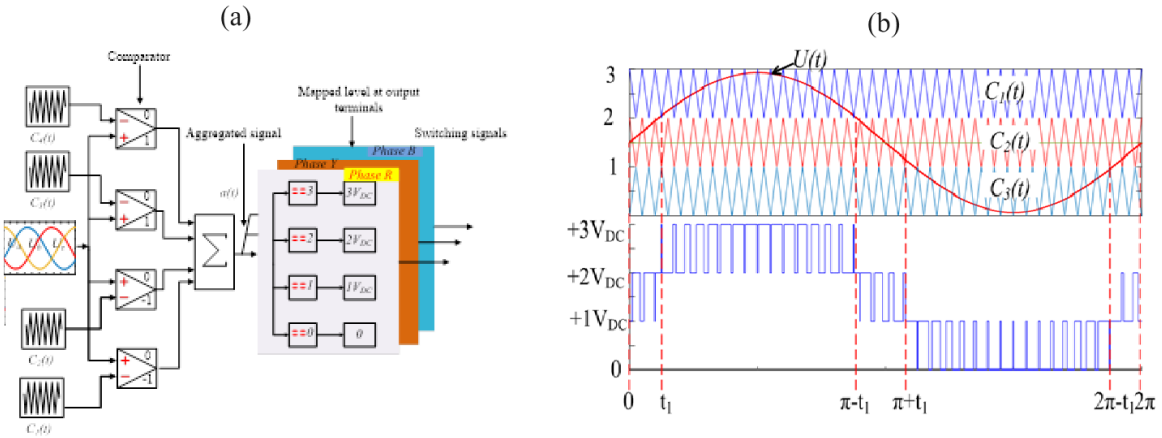

Figure 3. (a) Switching scheme of the PT (b) Carrier, Modulating and aggregate signal.

$$t_2 = \frac{\sin^{-1}\left(\frac{2}{3}\right)}{2\pi f_S} \tag{2}$$

$$t_3 = \frac{\pi - \sin^{-1}\left(\frac{2}{3}\right)}{2\pi f_S} \tag{3}$$

$$t_4 = \frac{\pi - \sin^{-1}\left(\frac{1}{3}\right)}{2\pi f_S} \tag{4}$$

where, f_S represents the fundamental wave frequency. Discharging amount of charge (ΔQ_C) of the capacitor is given asfollows.

$$\Delta Q_{C,i} = \int_{t_m}^{t_n} I_{peak} \sin(\omega t - \varphi) dt \tag{5}$$

where I_{peak} the peak value of load current is, φ is the phase angle between the load voltage and current, and $(t_m - t_n)$ is the lower and upper limits of the discharging period. Therefore, the capacitance $C_{X,i}(i = 1, 2)$ must satisfy the following condition

$$C_{X,i} \geq \frac{\Delta Q_{C_{X,i}}}{P * V_{DC}} \tag{6}$$

where, V_{DC} represents the supply voltage.

3. Modulation scheme

The proposed SCMLI utilizes a Level Shift Pulse Width Modulation technique, as illustrated in Figure 3 and described in reference [8]. In this approach, a reference signal at 50 Hz is consistently compared with three triangular carrier signals of identical amplitude and frequency (2 kHz) to generate the aggregated signal "a(t)". Utilizing Table 1 as a lookup table, the switching signals can then be derived from this combined signal.

Table 1. Switching states and the effect of capacitors.

S. No.	Pole voltage $V_{RO}(t)$	S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{R5}	S_{R6}	S_{R7}	S_{R8}
1	0	0	1	0	1	0	1	▲	▲
2	$+1V_{DC}$	0	1	0	1	1	0	▲	▲
3	$+2V_{DC}$	0	1	1	0	1	0	▲	▼
4	$+3V_{DC}$	1	0	1	0	1	0	▼	▼

4. Loss analysis

The suggested power converter experiences three different kinds of power losses, which can be divided into the following categories: (i) switching loss, (ii) conduction loss, and (iii) voltage ripple loss.

4.1 Switching loss

When a switch is activated or deactivated, some amount of energy is wasted is called switching losses. For a given switching cycle, the power dissipation due to the K^{th} switch can be written as [12, 13]:
Power loss due to turn-on:

$$p_{\text{sw, on, k}} = \frac{1}{6}(f_{\text{sw}} V_{\text{sw, k}} I_K t_{\text{on}}) \tag{7}$$

Power loss due to turn-off:

$$p_{\text{sw, off, k}} = \frac{1}{6}(f_{\text{sw}} V_{\text{sw, k}} I'_K t_{\text{off}}) \tag{8}$$

In the above equation, I_K and I'_K represent the current through the K^{th} power switch immediately after and immediately before it is turned on and off, respectively. The f_{sw} indicates the frequency of the transition. Blocking voltage is denoted by $V_{\text{sw, k}}$
Hence, total switching losses can be written as;

$$P_{\text{Switchingloss}} = \sum_{l=1}^{7}[\sum_{k=1}^{p_{\text{on}}} p_{\text{sw, on, k}} + \sum_{k=1}^{p_{\text{off}}} p_{\text{sw, off, k}}] \tag{9}$$

4.2 Conduction loss

Power consumed by the switches' internal resistance causes conduction losses. These conduction losses for the transistor and diode can be expressed as follows:

$$P_C(\text{transistor}) = \sum_{k=1}^{n} I^2_{\text{transistor(RMS)}} R_{\text{don}} \tag{10}$$

$$P_C(\text{diode}) = \sum_{k=1}^{n} I^2_{\text{diode(RMS)}} R_D \tag{11}$$

R_D and R_{don} the internal resistance of the switch and diode. As a result, the net conduction losses are expressed as;

$$P_C(\text{net}) = P_C(\text{transistor}) + P_C(\text{diode}) \tag{12}$$

4.3 Ripple loss

When capacitors are linked in parallel with the source, they get charged to V_{DC}. Voltage ripple loss [31] refers to the power dissipation that occurs when the supply voltage is different from the voltage across the capacitor. The formulae for calculating the ripple voltage of a capacitor are as follows:

$$\Delta V_{C_{X,i}} = \frac{1}{C_{X,i}} \int_{t_m}^{t_n} i_{c,i}(t) dt \tag{13}$$

where, $i_{c,i}(t)$ represents the current flowing through the capacitor at the time of discharge.
As a result, the ripple losses can be written as

$$P_{(\text{ripple})} = \frac{f_{ref}}{2} \sum_{i=1}^{2} C_{X,i} \Delta V^2_{C_{X,i}} \tag{14}$$

$i =$ no. of the switched capacitor units ($i = 1, 2$).

5. Results analysis

To determine the PT's efficiency, the simulation results are compared to the experimental data. Table 2 contains all the model and experiment parameters.

Fig. 4 presents the results obtained from executing the simulation. The pole voltage is depicted in Fig. 4 (a), which illustrates that the suggested architecture creates four different levels of pole voltage with a peak magnitude of $-3V_{DC}$. As can be seen in Fig. 4 (b), there are seven distinct line-to-line voltage levels produced by the design during the dynamic condition. A quick shift in the load depicted in Fig. 4 (c) does not affect the voltage level. Capacitor voltage, load voltage, and load current are displayed for phase leg R in Fig. 4 (d). As can be seen in Fig. 4 (d), the capacitors continue to have a self-balancing effect. FFT analysis of V_{RY} shows that the maximum fundamental voltage is 171.6 V with 31.08% of total harmonic distortion (THD), as shown in Fig. 4 (e) for an R-L load of 50 ohms and 80 mH. As can be seen in Fig. 4 (f), the FFT analysis of I_R reveals a fundamental current peak magnitude of 1.775 A with 1.45% THD. Switching losses

Table 2. Modelling and experimental study parameters.

Parameters	**Specification**
Input voltage (V_{DC})	100 V
Frequency (f)	50 Hz
Switching frequency (f_{sw})	2 kHz
Load	R = 50, L = 80 mH
Modulation index (M)	0.95
Capacitors ($C_{X1} = C_{X2}$)	2100 μF
Switches (MOSFET)	IRF640; Voltage rating = 600 V, Current rating = 18 A;
Diodes	MUR406
Driver	TLP152

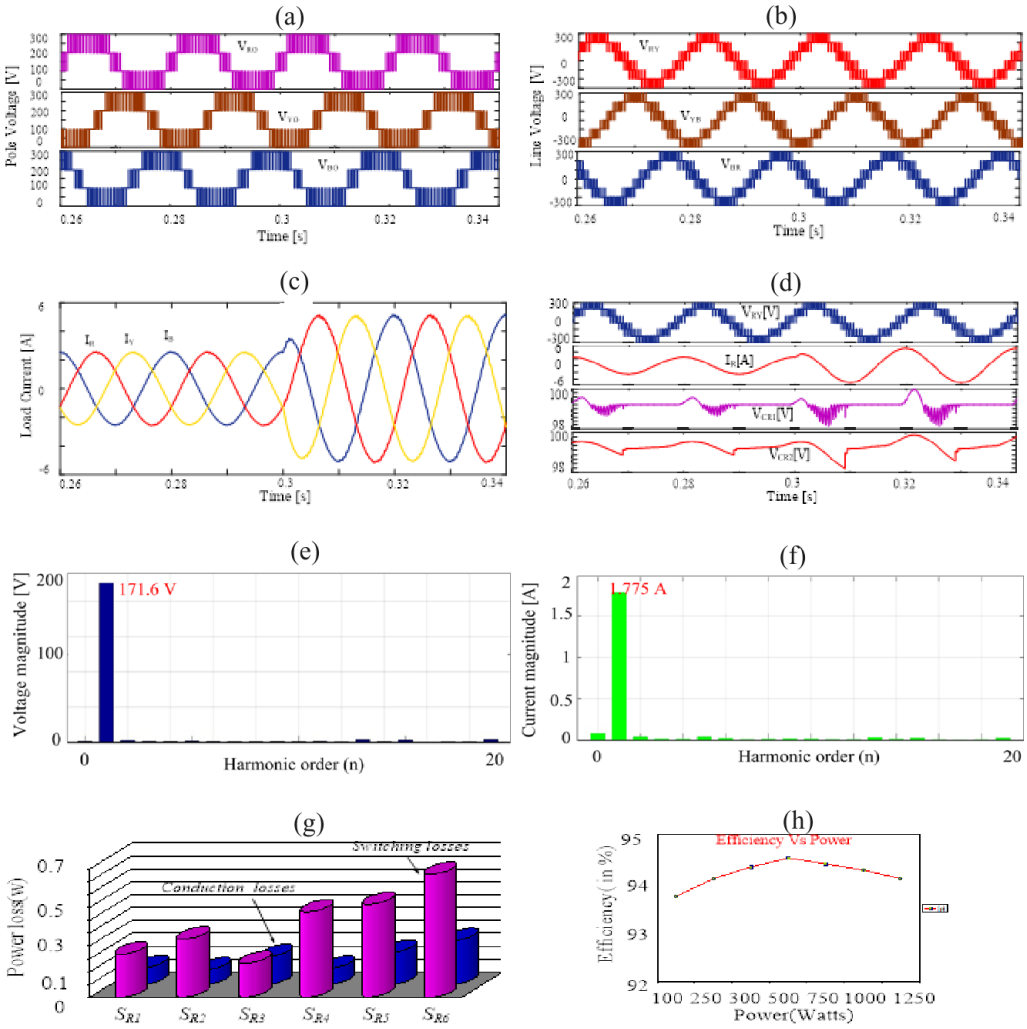

Figure 4. Simulation results of (a) V_{RO}, V_{YO}, V_{BO} (b) V_{RY}, V_{YB}, V_{BR} (c) I_R, I_Y, I_B (d) V_{RY}, I_R, V_{CR1}, V_{CR2} (e) FFT analysis of V_{RY} (f) FFT analysis of I_R (g) losses graph (h) power vs. efficiency.

To validate the proposed 7-Level novel work, experimental work has been carried out in the laboratory. Table 2 contains a list of the parameters that were utilized for the laboratory configuration. The snapshot of laboratory experimental setup has been shown in Fig. 5.

The experimental results are shown in Fig. 6. The PT generates a 4-level pole voltage (V_{RO}, V_{YO}, V_{BO}). Each level has an equal magnitude of V_{DC}. Fig. 6 (b-c) illustrates the PT line voltage (V_{RY}, V_{YB}, V_{BR}) as well as the line current (I_R, I_Y, I_B).It has been observed that during step change in load the novel work generates 7-level line-to-line voltage (V_{RY}, V_{YB}, V_{BR}) and each step of the line voltage has equal magnitude of V_{DC}. The voltage between the two separate capacitors is illustrated in Fig. 6 (d). Voltage and current

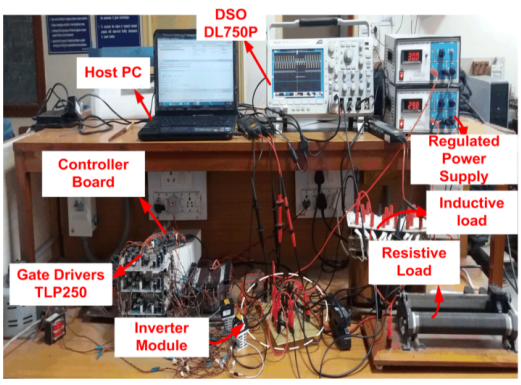

Figure 5. Experimental setup.

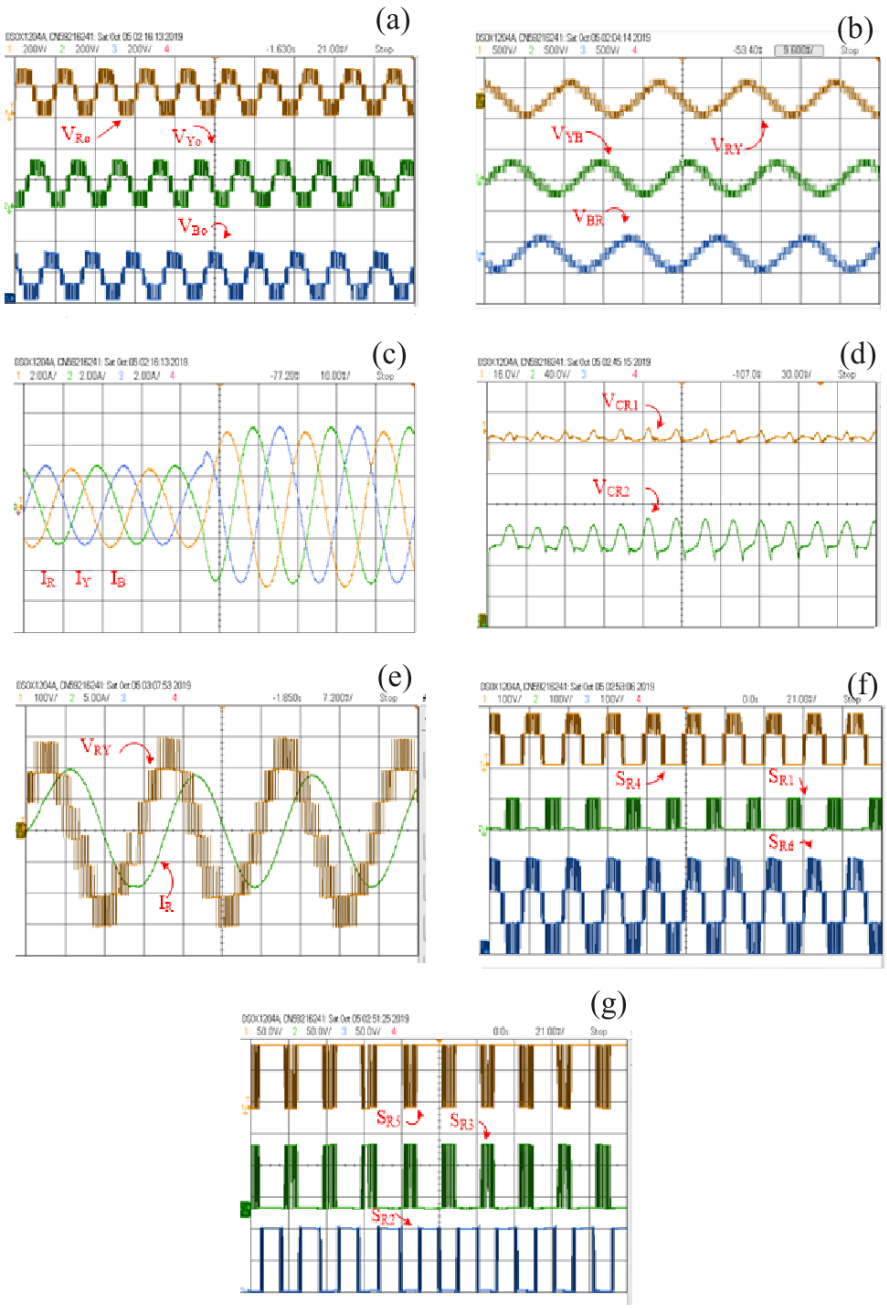

Figure 6. Experimental results of (a) pole voltage (b) line voltage (c) line current (d) per phase voltage and current (for R) (e) voltage stress on capacitors (f-g) switches stress.

along each phase of the line in steady state are shown in Figure 6 (e). Fig. 6 (f-g) shows the voltage stresses across the switching components

6. Comparative analysis

The proposed configuration minimizes the number of switching components and power supply required to achieve a maximum output voltage. The effectiveness of the PT has been evaluated by comparing it to other architectures regarding the number of power switches, diodes, capacitors, driver units, and power supplies and boosting ability. Total component counts can be calculated using the factor component count per level ($F_{c/l}$).

The following equation describes this variable:

$$F_{c/l} = \frac{N_{sw} + N_c + N_d + N_{dri} + N_s}{N_l} \tag{15}$$

N_s = number of sources, N_l = number of generated levels, N_c number of capacitors, N_d = number of auxiliary diodes, N_{dri} = the number of the gate driver circuits. Table 3 shows the results of a comparison between the PT and other three-phase topologies. In terms of the voltage source, the topologies [5–7], [9–11], [22] have multiple voltage sources and can't boost the voltage. These topologies are complex and costly as they come from multiple sources. The PT has a lower total number of components than topologies [17].

Table 3. Comparative analysis of the current three-phase topologies.

Topology	N_l	N_{sw}	N_s	N_d	N_c	N_{dri}	$F_{c/l}$	Gain
[5]	5	8	2	-	1	8	3.8	1
[6]	5	10	2	-	-	9	4.2	1
[7]	4	6	4	-	-	6	4	1
[9]	4	4	2	-	-	4	2.5	1
[10]	3	8	2	-	-	8	6	1
[11]	4	6	3	-	-	6	3.75	1
[17]	4	5	1	3	2	5	4	3
[18]	4	8	1	-	3	8	5	1.5
[19]	4	10	1	-	3	9	5.75	1.5
[20]	4	8	1	2	4	8	5.25	1
[21]	5	10	1	-	3	10	4.8	1
[22]	4	6	2	1	1	6	4	3
[P]	4	6	1	2	2	6	4.25	3

7. Conclusion

This paper presents a three-phase SC topology with reduced switching components. The PT's salient characteristics consist of its self-balancing voltage capacitor, its low number of parts counts, and its capacity to raise voltage levels by 3X times (i.e., three times the supply voltage). The suggested work's relevance is demonstrated through a brief comparison to existing topologies. The PT has been proven beneficial in both steady-state and transient studies, and it has been verified by both computational and experimental research. Moreover, FFT analysis of fundamental voltage is 171.6 V with 31.08% of total harmonic distortion (THD), and fundamental current peak magnitude of 1.775 A with 1.45% THD. The proposed topology achieves a peak efficiency of 95%.

Authors contributions
All authors have contributed equally to prepare the paper.

Availability of data and materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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