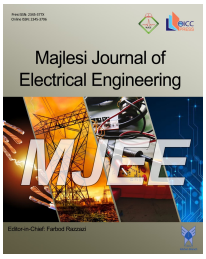


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# Two-switch step-down converter with low switch voltage stress

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**Original Research**

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**Abstract:**

The current research introduces an enhanced buck converter. The introduced converter improves the performance of similar converters thanks to causing lower switch voltage stress, higher efficiency and fewer number of elements. To make use of low voltage MOSFETs with a smaller ON resistance, using multiple switching strategies would reduce the voltage stress across the switch and thus allow them to be used. This study compares the performance of the proposed converter with the similar converters. The gate pulses are similar in the proposed converter, so the control is very simple. Input voltage is divided between the blocking capacitors at the input and as a result, the voltage stress on the switches is lower than the input voltage. So, the converter can be designed with MOSFETs with low drain-source resistance. Also, the voltage gain is reduced in comparison with the conventional buck converter. Furthermore, output power is shared between two switches which results in better heat dissipation. Also, it is possible to implement the proposed converter using a single magnetic element. Therefore, the total number of components in comparison with similar converters is reduced. The results show that the introduced converter technically performs with lower switching losses and increased overall efficiency discussion of operating modes, as well as converter design and test results shall be provided.

**Keywords:** Buck-boost converter; Buck converter; High efficiency; Low switch voltage stress; Pulse Width Modulation; Step-down DC to DC converter

## 1. Introduction

Step-down DC-DC converters have proved their applicability, especially in automotive and electronics industries where they are used as the main part of LED drivers, battery chargers, and voltage regulator modules (VRMs) integrated with microprocessors power supplies, etc. [1, 2]. Also, in cases where no electrically isolated systems are required, the converters without isolation including the conventional step-down buck converters are preferable as compared with isolated ones thanks to the need for smaller number of components, less complexity and reduced costs [3]. But the drawback here is their semiconductor devices undergo high voltage stress, relatively high conduction, and switching losses specifically affecting the output diode emanating from greater output current value. Additionally, owing to their working at narrower duty cycles with low voltage gain, the conventional buck converters operate with higher current stress of their semiconductor parts which in turn would lead to dramatic reduction of their efficiency [4]. The efficient strategies already in place are an interleaved approach, taking into consideration the series capacitors or switching capacitors, with a view to increasing efficiency. These methods are working with improving the voltage conversion ratio and reducing the switch voltage stress. Paper [5] has used switching capacitors and coupled inductors, with the disappointing use of seven number of switches. The study [6] has combined the interleaved method and series capacitors to enhance the voltage conversion ratio. However, it is equal in value to the input voltage pressure of the main switch. In another study [7], the addition of two switches improves

the voltage conversion ratio to one-sixth in comparison with conventional buck converter. Study [8] has used a switching capacitors cell together with the interleaved method to achieve a considerably high step-down conversion ratio accompanied by minimized voltage stress on the components. However, the disadvantage of the proposed system was that despite the many components used, the voltage conversion ratio has not improved considerably. Subsequently, the study [9] used a couple of inductors in the output section in order to decrease the converter volume. Despite these changes, the voltage stress and voltage conversion ratio of the elements did not encounter any decrease and the number of components used remained numerous. Another study [10] changed the interleaved buck converter structure and proposed a buck converter with improved lower voltage stress and voltage conversion ratio through input voltage splitting. Additionally, it enjoyed the current balance in all phases, although it used many inductors. The paper [11] introduced a high step-down converter by the combination of Cuk and buck converters that reduced the voltage stress of the semiconductor elements as the effect of input voltage splitting. The study [12] introduced a converter that can provide zero voltage switching. However, a voltage spike has also been generated by a leakage inductance spike during the turn-off instant.

Another alternative is a combined typology involving coupled-inductors or tapped inductors and buck converters. The soft switching interleaved converter proposed in [13] could eliminate as a result of the leakage inductance energy, the extra voltage spikes in the switches are absorbed. However, the topology required four switches and three magnetic cores while voltage spikes were observed in freewheeling diodes. Study [14] added coupled inductors to the converter introduced in [11], and proposed an ultra-high step-down converter that in spite of benefiting from reduced voltage stress across the semiconductor elements to below half of the input voltage, the system suffered from high number of components. A voltage stress greater than the input voltage of the converter itself was generated by the step-down converter introduced in [15]. The converter proposed in [16] by adjusting the ratio of coupled-inductor turns and their number of phases, improvements in voltage gain were achieved. Each individual phase consisted of numerus passive and active elements resulted in a greater volume and weight, and complex control. A further disadvantage is that there is a voltage stress factor of main switches which equals the input voltage. The converter proposed in the study [17] was a resonant converter with one switch. Although theoretically, the authors declared a voltage stress equivalent to the input voltage, practically the actual waveform however indicated a slight increase in the voltage stress.

The present paper introduces a step-down non-isolated DC-DC converter with improved voltage conversion ratio as compared to the conventional buck converter. Also, it offers a reduced semiconductor voltage stress to below of the input voltage. The proposed converter minimizes the number of components used in the structure, thus reducing size, cost, and circuit complexity. Furthermore, in view that switches being switched on and off at the same time, a simple control circuit is built into the converter. In addition, the proposed converter is characterized by a simplified control circuit as the switches are turned on and off at the same time.

The structure of this paper is based on eight sections. The operation of the proposed converter shall be provided for in the second part of this article, while design considerations shall be taken into account in the third part. The results of the experiments are also made available in the fourth section. Loss calculations are being examined under the 5th section. A comparison is made between similar converters and the proposed converters in the sixth section. The improved converter with a single magnetic element is proposed in the seventh section.

## 2. Operation of proposed converter

The introduced converter, as can be seen from Fig. 1, is composed of two input capacitors ($C_1$, $C_2$), a pair of switches ($S_1$, $S_2$), two inductors ($L_1$, $L_2$), one output filter capacitor ($C_o$), and two diodes ($D_1$, $D_2$). The converter has been proposed with the decline of voltage stress as the ultimate goal and the switches will have identical duty cycles to counterbalance the voltage among the input capacitors.

In order to evaluate the probable performance of converters under that study, the assumptions set out below have been considered. All the switches have been considered ideal, and the input capacitors are identical with different voltages which are calculated in the next section ($C_1 = C_2$). The converter operates in CCM mode. In general, the introduced converter can operate in two modes in a switching cycle. Fig. 2 represents the key operational waveforms of the converter proposed in this study.

**Mode 1 [$t_0 - t_1$]:** In this mode, the switches $S_1$ and $S_2$ are turned on, while the diodes $D_1$ and $D_2$ turn off. In the meantime, the inductors $L_1$ and $L_2$ are charged by voltage sources $V_{C1}$ and $V_{C2}$. In Fig. 3 (a) the equivalent circuit of the converter is shown. The currents of inductors are calculated as follows:

$$V_{L1} = V_{C1} - V_O \tag{1}$$

$$I_{L1}(t) = \frac{V_{C1} - V_O}{L_1}(t - t_1) + I_{L1}(t_0) \tag{2}$$

**Mode 2 [$t_1 - t_2$]:** In this mode, the switches $S_1$ and $S_2$ are turned off, and diodes $D_1$ and $D_2$ turn on, as illustrated in

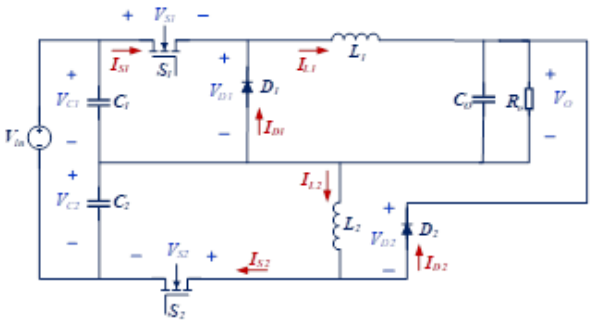

**Figure 1.** The proposed converter.

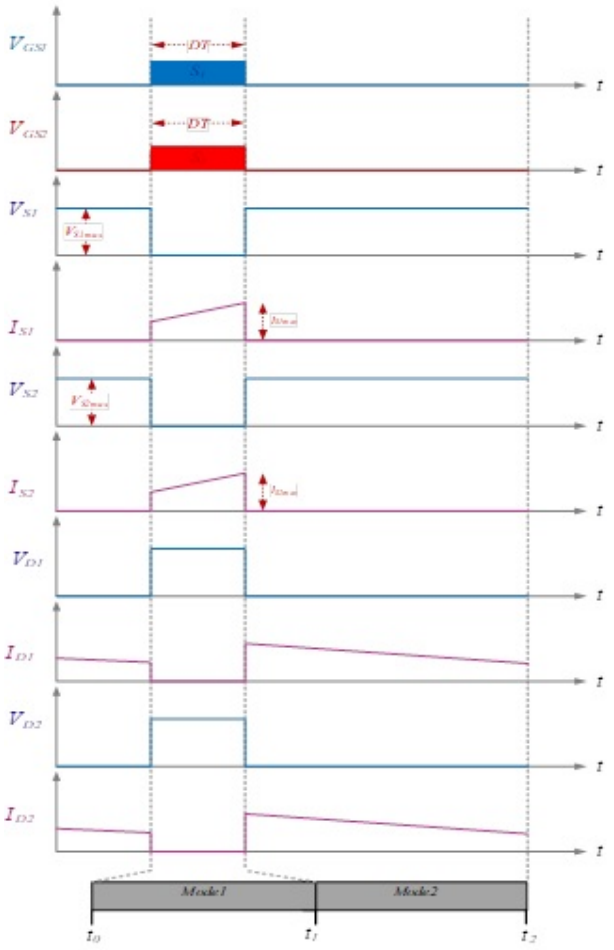


**Figure 2.** Switching waveforms of the proposed converter.

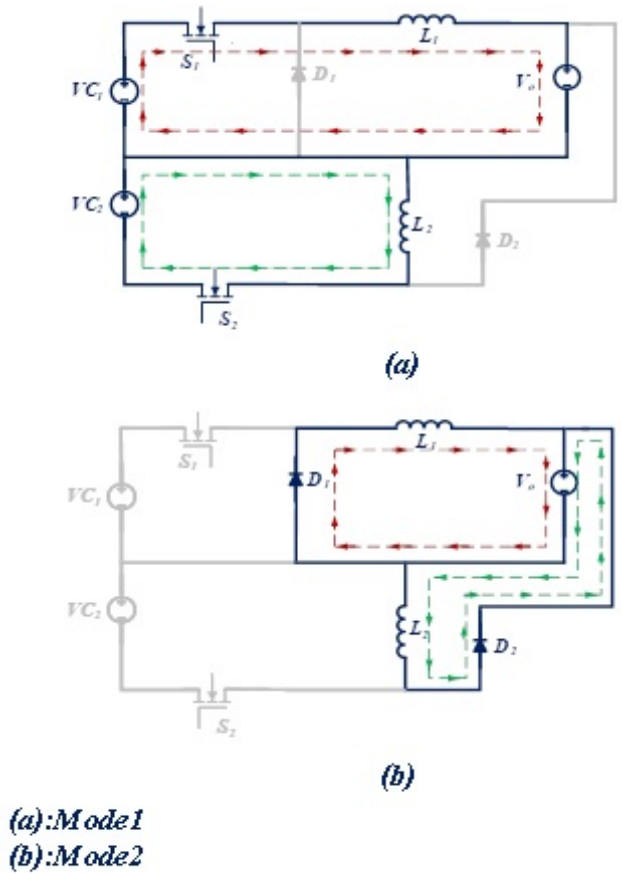


**Figure 3.** An equivalent circuit for each of the stages of operation.

Fig. 3 (b). In the meantime, the $L_1$ and $L_2$ inductors are discharged by $V_O$. The currents of inductors are calculated as follows:

$$V_{L1} = V_{L2} = -V_O \tag{3}$$

$$I_{L1}(t) = \frac{-V_O}{L_1}(t - t_2) + I_{L1}(t_1) \tag{4}$$

The block diagram of the control system is shown in Fig. 4, based on the operation of the proposed converter shown in Fig. 3. Regular PWM controllers such as SG3525 or UC38xx series can be used to control the converter. Only the output pulse should be applied to two gate drive circuits.

## 3. Converter anslysis and design consideration

The following relationships are obtained on the basis of the volt-second balance of $L_1$ and $L_2$:

$$(V_{C1} - V_O)DT = V_O(1-D)T \tag{5}$$

$$V_{C2}DT = V_O(1-D)T \tag{6}$$

$$V_{C1} = \frac{V_O}{D} \tag{7}$$

$$V_{C2} = \frac{V_O(1-D)}{D} \tag{8}$$

Considering the input KVL, the input voltage is written as the following:

$$V_{in} = V_{C1} + V_{C2} \tag{9}$$

The voltage conversion ratio may be determined by means of Equations (7), (8) and (9) as follows:

$$G = \frac{V_O}{V_{in}} = \frac{D}{2-D} \tag{10}$$

The voltage gain versus various values of Duty cycle is shown in Fig. 5 and it has been compared with some articles from the references.

### 3.1 Current and voltage stress of switches

A determination of the current stress on $S_1$ and $S_2$ switches is made as follows:

$$I_{S1max} = I_{S2max} = \frac{I_O}{2-D} + \frac{1}{2}\Delta_{iL} \tag{11}$$


**Figure 4.** Controller block diagram of the proposed converter.

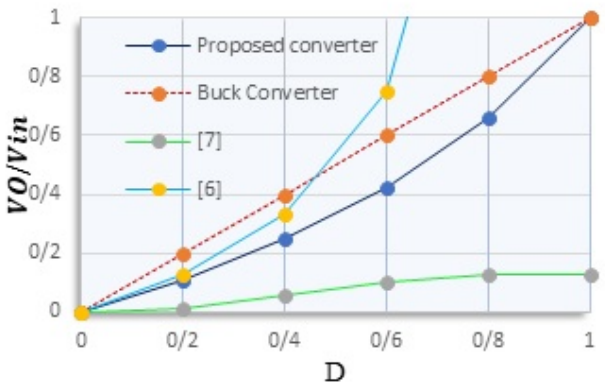


**Figure 5.** Voltage gain vs. Duty Cycle.

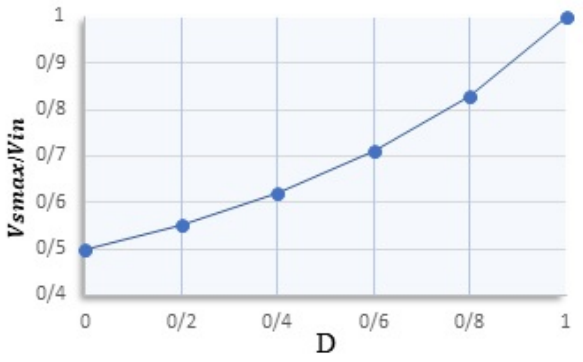


**Figure 6.** Normalized switch voltage stress vs. Duty Cycle.

Note that $\Delta_{iL}$ represents the inductor current peak-to-peak ripple, which can be designed as 10% $I_O$.
The voltage stress on each switch could be determined by means of the Equations (7) and (10):

$$V_{S1max} = V_{S2max} = \frac{V_{in}}{2-D} \tag{12}$$

In Fig. 6, the voltage stress for switches is shown to be normalized with input voltage, taking into account different duty cycle values.

### 3.2 The inductor designs

First, the operating duty cycle in CCM mode is estimated based on the converter voltage gain equation. The inductance of the $L_1$ and $L_2$ converter is similar to that of a conventional buck-boost and buck converter, as follows:

$$L_1 = L_2 = \frac{V_O(1-D)}{\Delta_{iL} f_{sw}} \tag{13}$$

### 3.3 Capacitor design

Based on the converter voltage gain and its input and output voltages, the converter operating duty cycle is calculated. The output current discharges an output capacitor when the switches are turned on. the calculation of the output capacitor is made through the following relationship:

$$C_o = \frac{I_O D(1-D)}{\Delta V_{Co} f_{sw}(2-D)} \tag{14}$$

where, $\Delta V_{Co}$ is usually considered less than $\%1 V_o$.

## 4. Experimental results

The converter prototype, designed for a 100 W output power, 160 V input voltage, 20 V output voltage, and 50 kHz operating frequency, was assembled and commissioned, the results of which have been provided as indicated in Fig. 7.
• At first, the switching frequency has been chosen to be 50 kHz.
• Duty cycle has been calculated from the Equation (10) and it is equal to:

$$G = \frac{20}{160} = \frac{D}{2-D} \Rightarrow D = 0.22 \tag{15}$$

• The inductors and output capacitor are designed as follows, according to the design equations described in previous section:
$\Delta_{iL}$ has been considered as 10% of the maximum output current, which is 0.5 A.
According to Equation (13), the values of inductors have been calculated as:

$$L_1 = L_2 = \frac{20 \times 0.78}{0.5 \times 50000} = 624 \ \mu\text{H} \tag{16}$$

So, the values of inductors have been considered equal to 600 $\mu$H.
• For calculating the output capacitor:
$\Delta V_{Co}$ has been considered less than $\%1 V_O$, which is 0.5 v.
According to Equation (14), the value of the output capacitor has been calculated as:

$$C_o = \frac{20 \times 0.22 \times 0.78}{0.5 \times 50000 \times 1.78} = 77 \ \mu\text{F} \tag{17}$$

So, the value of the output capacitor has been considered to be larger and equal to 100 $\mu$F.
• The current stress and voltage stress of switches have been calculated on each switch from the Equation (11) and (12),

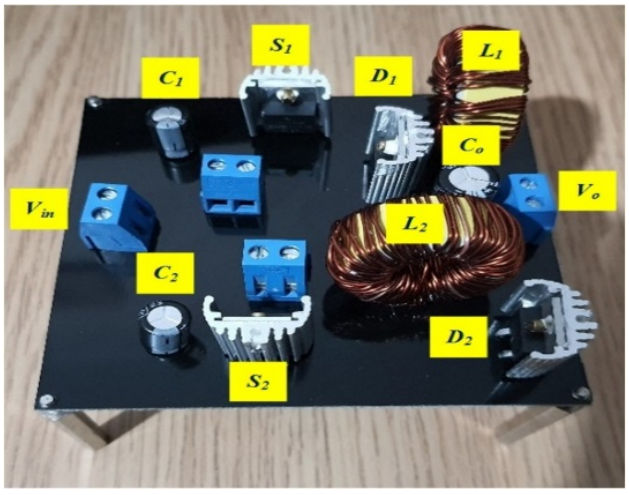


**Figure 7.** The photo of prototype converter.

**Table 1.** Characteristics of the elements in the prototype converter.

| Components | Specifications |
|---|---|
| Input voltage | 160 V |
| Output voltage | 20 V |
| Switching frequency $f_s$ | 50 kHz |
| Output power | 100 W |
| Inductors $L_1$ & $L_2$ | 600 $\mu$H |
| Input capacitors $C_1$ & $C_2$ | 10 $\mu$F |
| Output capacitor $C_o$ | 100 $\mu$F |
| Main switches $S_1$ & $S_2$ | IRF3710 |
| Diode $D_1$ & $D_2$ | MBR10100 |

and the values are equal to:

$$V_{S1max} = V_{S2max} = \frac{160}{2-0.22} = 89.8 \text{ V} \qquad (18)$$

$$I_{S1max} = I_{S2max} = \frac{5}{2-0.22} + \frac{1}{2}0.5 = 3.05 \text{ A} \qquad (19)$$

Due to the fact that the voltage stress on each switch and each diode are less than 100 volts, IRF3710 and MBR10100 are selected for the converter switches and diodes respectively.

The prototype specifications are shown in Table 1. Experimental data indicate equal voltage stress across the $S_1$ and $S_2$ switches. Also, Fig. 8 illustrates the gate pulses of switches. Figs. 9 and 10 show the corresponding voltage and current results for $S_1$ and $S_2$. Figs. 11 and 12 show the corresponding voltage and current results for $S_1$ and $S_2$ in PSPICE software. As a result, the corresponding voltage stress across switches $S_1$ and $S_2$ was equal to 90 V in the proposed converter prototype.

Additionally, Fig. 13 compares the introduced converter efficiency with the conventional buck converter at different loads.

## 5. Loss calculation

A comprehensive loss analysis of the introduced converter owing to switches, diodes, and inductors is given in the present section. Table 2 presents the loss data as shown below:

Table 2, containing $R_{ds}$, $V_f$, $t_f$, $t_r$, and $C_{oss}$ individually appears the ON-state resistance of the switches, diode forward bias voltage, the fall time of the switches, and the output capacitance of the switches, given by the MOSFET's and

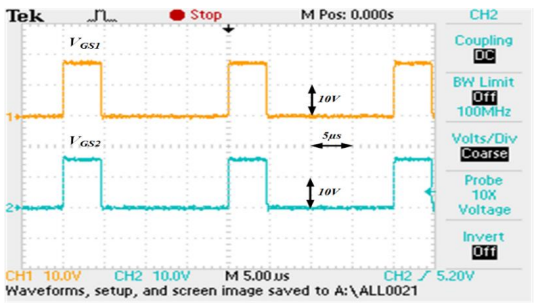


**Figure 8.** The Switches gate pulses.

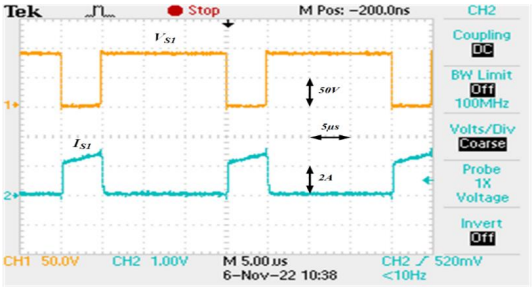


**Figure 9.** The prototype converter is the voltage and current of the switch $S_1$.

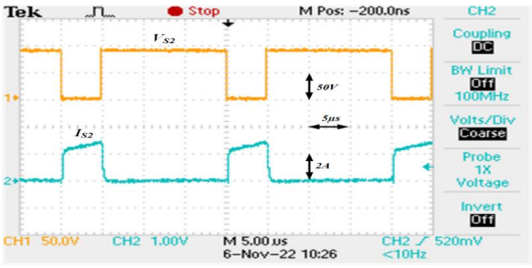


**Figure 10.** The prototype converter is the voltage and current of the switch $S_2$.

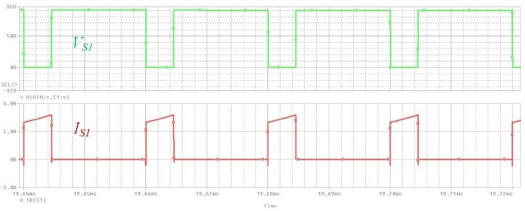

**Figure 11.** The prototype converter is the voltage and current of the switch $S_1$ in PSPICE software.

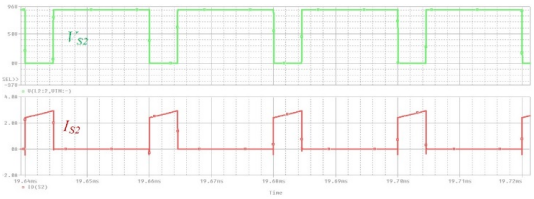

**Figure 12.** The prototype converter is the voltage and current of the switch $S_2$ in PSPICE software.

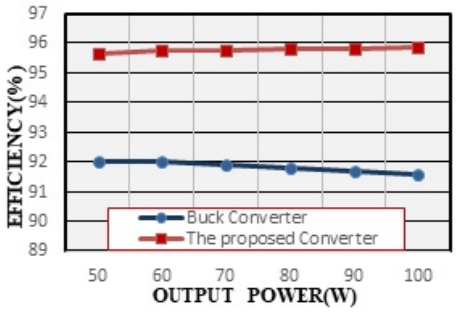


**Figure 13.** Efficiency versus output power in the prototype converter and buck converter.

**Table 2.** The prototype converter losses

| **Type of losses** | **Expressions** | **Value (Watt)** |
|---|---|---|
| Conduction loss of each switch | $P_{cond,\,S_1} = R_{ds}D(\frac{I_O}{2-D})^2$ | 0.04 |
| Turn-on switching loss of each switch | $P_{\mathrm{On},\,S_1} = \frac{1}{2}t_r\frac{P_O}{D(2-D)}f_{sw}$ | 0.37 |
| Turn-off switching loss of each switch | $P_{\mathrm{Off},\,S_1} = \frac{1}{2}t_f\frac{P_O}{D(2-D)}f_{sw}$ | 0.30 |
| Capacitive turn on loss each switch | $P_{coss,\,S_1} = \frac{1}{2}C_{oss}(\frac{V_{in}}{2-D})^2 f_{sw}$ | 0.12 |
| loss of each diode | $P_{DIODE,\,D_1} = V_F\frac{(1-D)^2}{2-D}I_O$ | 1.11 |
| Conduction loss of each inductor | $P_{cu,\,L_1} = R_L(\frac{I_O}{2-D})^2$ | 0.07 |
| Other loss | $P_{oth}$ | 0.30 |
| Total power losses | | 4.32 |

**Table 3.** A Comparisons between converters on voltage stress and the number of elements.

| Characteristics | Switch count | Capacitor count | Diode count | Total number of components | Voltage stress of switches | Voltage gain | Efficiency ($P_{out}$ = 100 W) |
|---|---|---|---|---|---|---|---|
| [6] | 5 | 2 | 0 | 10 | $V_{in}, \frac{V_{in}}{3}$ | $\frac{D}{(1+n)(1-D)}$ | 90.5% |
| [7] | 6 | 7 | 2 | 17 | $\frac{V_{in}}{3}$ & $\frac{V_{in}}{6}$ | $\frac{D}{6}$ | 89% |
| [9] | 3 | 3 | 4 | 11 | $\frac{V_{in}}{2-D}$ | $\frac{D}{2-D}$ | 87.8% |
| [10] | 2 | 5 | 6 | 17 | $\frac{V_{in}[(1+D)[1+N(1-D)]+ND^2]}{2[1+N(1-D)]-D^2}$ | $\frac{D^2}{2[1+N(1-D)]-D^2}$ | 94.3% |
| [13] | 6 | 4 | 2 | 15 | $\frac{V_{in}}{2}$ | $\frac{D(1-D)}{2(1+n)}$ | 91% |
| [14] | 3 | 5 | 2 | 13 | $\frac{V_{in}(n-D+1)}{n(D+1)+D(D-1)+1}$ & $\frac{V_{in}(n+D)}{n(D+1)+D(D-1)+1}$ | $\frac{D(1-D)}{n(1+D)+D(D-1)+1}$ | 93.8% |
| Proposed converter | 2 | 3 | 2 | 9 | $\frac{V_{in}}{2-D}$ | $\frac{D}{2-D}$ | 95.8% |

the Diode datasheets.
As a result, the total power loss is to be read as follows:

$$P_{LOSS} = P_{cond,\,S_1} + P_{cond,\,S_2} + P_{\mathrm{On},\,S_1} + P_{\mathrm{Off},\,S_1} + P_{coss,\,S_1} + P_{\mathrm{On},\,S_2} + P_{\mathrm{Off},\,S_2} + P_{coss,\,S_2} + P_{DIODE,\,D_1} + P_{DIODE,\,D_2} + P_{cu,\,L_1} + P_{cu,\,L_2} + P_{oth} \tag{20}$$

$P_{out}$ denotes the output power. Thus, the theoretical efficiency, as shown by $\eta$ can be determined according to the following equation:

$$\eta = \frac{P_{out}}{P_{out} + P_{LOSS}} \tag{21}$$

Using the parameter values obtained from the previous designs, the theoretical nominal efficiency was calculated to be as equal to 95.8%.

## 6. Comparison with other converters

Table 3 shows the comparison of the introduced converter from this paper with a number of converters that have been suggested by literature. According to Table 3, the introduced converter produces lower voltage stress on the switches and uses smaller number of elements. The efficiency of 100 watts of power was also compared.

## 7. Proposed converter with single magnetic element

In this part, it is shown that instead of two inductors of the converter, one coupled inductor can be used. In Fig. 1 the inductors are coupled to each other and PSPICE software is used for simulation of converters. The simulation results confirm the balance of input capacitors and thus power balance between the two phases. The inductors are coupled without any change in the circuit operation.

## 8. Conclusion

The DC-DC converter that has been introduced in this study is an improvement over the other similar step-down converters, by reducing voltage stress on switches and providing greater efficiency. In terms of efficiency between 50 W and 100 W, the prototype converter has been compared with a conventional buck converter. Compared to a conventional buck converter, the prototype has an efficiency of 95.8% at 100 W output power and is improving slightly by about 4%. The studied prototype, produced a voltage stress of about 90 V under 160 V input voltage while producing 100 W-output power. The proposed structure provides step-down conversion, low voltage stress of switches and current sharing among them. It follows from this that the prototype produced a voltage stress lower than the input voltage of the switches, which would in turn lead to reduced equipment costs.

**Authors contributions**
All authors have contributed equally to prepare the paper.

**Availability of data and materials**
The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Conflict of interests**
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.



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