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Original Research

A Novel Switched Capacitor Multilevel Inverter for Renewable Energy Application

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Abstract:

This paper introduces a novel single-phase five-level switched-capacitor multilevel inverter (5L-SCMLI) topology distinguished by self-voltage balancing and intrinsic voltage enhancement capabilities. Without an extra DC-DC boost converter or transformer, the proposed topology (PT) provides a voltage gain factor of two. The PT produces a five-level output voltage utilizing only eight switches and two capacitors, hence offering a more compact, cost-effective, and efficient design. The proposed design implements the PWM technique for the smooth operation of the PT. A comprehensive comparison with the current SCMLI design highlights the PT benefits. To assess the usefulness of the proposed methodology, extensive simulations and experimental investigations have been executed to confirm the effectiveness of PT. The PT stands out as the most cost-effective design at only 73.44 USD.

Keywords: Cost function; Multilevel inverter; Switched capacitors; PD-PWM; Switch count; Total voltage stress

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1. Introduction

Renewable energy has emerged as the most promising alternative source in response to the depletion of fossil fuels. Nonetheless, although the majority of renewable sources are DC, alternating current (AC) is necessary for domestic and industrial applications. Power electrical devices, such as inverters, are utilized to facilitate efficient DC-to-AC conversion, thereby bridging this gap. Conventional two-level inverters are widely used but face significant drawbacks, including high switching losses and inferior harmonic performance. Multilevel inverters (MLIs) have attained considerable prominence in the power electronics domain owing to their benefits over traditional inverters, such as reduced dv/dt, enhanced power quality, and reduced total harmonic distortion (THD), and minimize voltage stress on power devices [1]. Owing to these benefits, MLIs are extensively employed in various applications, such as FACTS, active power filters, and renewable energy generation (REG). However, incorporating an inductor in a boost converter increases the system's size and complicates its control architecture. The SCMLI has become a promising topology for medium- and high-power applications because it can boost voltage, lower the number of devices needed, and balance capacitor voltage naturally without needing extra sensors or controllers [2]. Several five-level inverter configurations employing switched-capacitor (SC) technology have been presented in the literature, each offering distinct advantages and limitations. A five-level cascaded inverter that uses a half bridge and an inductor to charge capacitors slowly and boost voltage twice. It addresses impulse charging currents and non-uniform operation common in switched-capacitor inverters [3].

Five-level common ground inverter with double voltage boosting, utilizing only eight switches and two capacitors for efficient operation. It minimizes leakage current, balances capacitor voltages, and achieves high efficiency ($\sim 96.5\%$) [4]. A common ground type inverter that uses *SC* to boost voltage while cutting down the energy those capacitors need to store. Unlike older designs where capacitors had to handle peak output voltage, this one uses capacitors rated just for half that voltage. It balances voltage on its own, keeps voltage change rates low, and doesn't need sensors to operate [5]. It introduces an H-9 topology with nine switches for output voltage control. Uses virtual grounding to cut down leakage current and keeps the capacitor ripple balanced [6]. A new five-level inverter design focuses on a common ground design to minimise leakage current. The inverter uses just two *SC*, each rated for half the output voltage, which cuts down the size, cost, and complexity [7]. An enhanced 5-L ANPC inverter, in contrast to the traditional model that uses only half of the dc-link voltage, attains double dc voltage utilization by utilizing an *SC* charged to half of the input voltage [8]. A single-phase five-level *SC* boost inverter is proposed to achieve higher voltage gain compared to conventional impedance-source inverters. The *SC* configuration effectively doubles the boosting capability while ensuring self-balancing of capacitor voltages [9]. A novel dual-mode, transformer less five-level inverter with a common-ground architecture for PV grid-connected systems provides efficient voltage boosting, self-balancing, significantly reduces leakage current, and ensures stable power injection with simple control strategies [10]. A five-level T-type inverter that addresses the problem of current spikes by employing a soft-charging technique using a dedicated inductor–switch circuit and also it enhances voltage gain and achieves improved utilization of the dc-link voltage compared to conventional designs [11]. Single-phase five-level converters design using SCs includes the key points that it boosts voltage without needing the usual H-bridge for reversing polarity, which cuts down on switching losses and voltage stress on parts [12, 13]. A new single-phase five-level *SC* boost inverter with improved voltage gain over traditional impedance-source inverters. It uses an *SC* structure that doubles the boost factor while keeping capacitor voltages balanced [14]. Common ground 5-level topologies recommended in [15, 16] are utilized for PV applications with zero leakage current. A five-level inverter integrating a flying-capacitor clamp with a bridge *SC* configuration, as presented in [17]. It reduces the quantity of components, minimizes switching losses, and enhances efficiency. An improved phase-disposition PWM ensures the self-balancing of capacitors and enhances output quality. The 7L inverter design presented in [18] provides a number of advantages, such as fewer parts, automatic voltage balancing, higher power quality with reduced harmonic distortion, and efficient maximum power point tracking using the modified Regula Falsi method. It is a fantastic choice for reliable, high-quality solar PV applications that perform better since it is compact and can improve voltage. An A7-level switched capacitor inverter for solar PV systems that uses fuzzy logic to find the best switching angles and an APSO algorithm to find the best maximum power point. The design lowers harmonic distortion and the number of devices, which makes it more efficient and cost-effective [19]. A novel seven-level inverter that utilizes the SCs approach and is powered by a single DC source, as proposed in [20]. It naturally balances the capacitors voltage, a closed-loop voltage balancing circuit is not required.

The following are the key benefits of the PT:

- Increasing ability, which is $2X$
- Natural balancing of the capacitor voltage
- Less TSV
- Lower cost
- 50% switches can work with any voltage level
- Low losses

The remaining details of the section are as follows: section 2 specifies the design's concept and operation. In section 3, discuss the PT control techniques. The idea of power loss of the proposed 5-level topology is explained in detail in section 4. Section 5 covered a comparison study to establish the effectiveness of the suggested topology and superiority. Section 6 focuses on further investigating the outcomes analysis that confirms the efficacy. The last section 7, provides a summary of the work.

2. Proposed 5L-SC-MLI topology

(a) Description of 5L-SC-MLI Topology:

Figure 1 depicts a 5-LSCMLI structure that uses a single input source and features eight switches, two capacitors, and two diodes. The PT generates five different voltage levels as an output: 2 V_{DC}, 1 V_{DC}, 0, -1 V_{DC}, and -2 V_{DC} with a gain of twice the input voltage. It doesn't use an H-bridge here to make both types of voltage. The PT doesn't need a sensor or any other circuit to keep the capacitor voltage balanced. The capacitors maintain their own balance due to their series and parallel connections to the input source. Table 1 shows the order in which the proposed topology switches.

(b) Operation of the *SC* five-level topology:

State-β_1/β_2:$V_0 = 0$

$V_0 = 0$, when S_2, S_6, and S_8 are closed, the network connects C_1 to a charging path from the DC supply through the on-switch S_6, so C_1 is charging towards V_{DC} shown in Fig. 2 (a). In state β_2, $V_0 = 0$, when S_1, S_3, and S_7 are closed, the network links C_2 to a charging path from the DC source (via the on-switches S_3), therefore C_2 is charged towards V_{DC} shown in Fig. 2 (b).

State-β_3:$V_0 = 1$ V_{DC}

When switches S_2, S_6, and S_7 are turned ON, the output voltage in this state is $V_0 = 1$ V_{DC}. As shown in Fig. 2 (c), S_6 also charges capacitor C_1 to V_{DC} at the

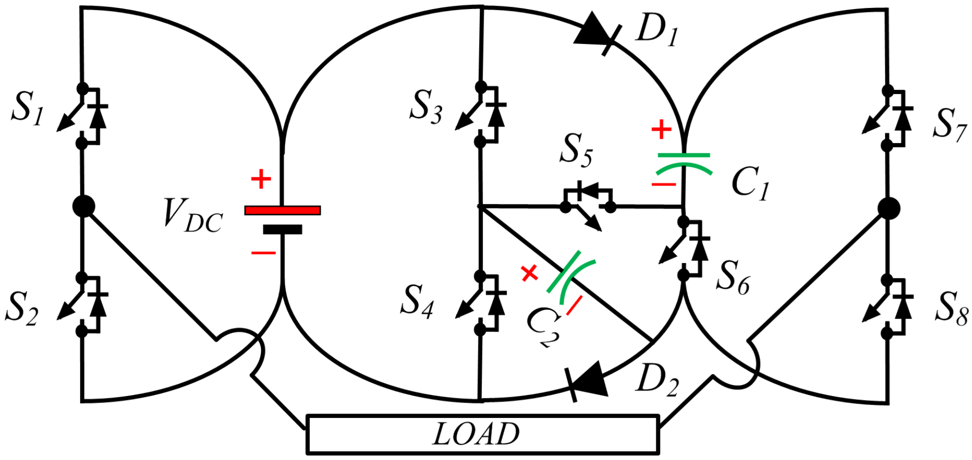

Figure 1. Proposed 5-LSCMLI.

Table 1. Switching pattern of 5L-SC-MLI.

X	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	C_1	C_2	V_O
β_1	-	1	-	-	-	1	-	1	Δ	-	0
β_2	1	-	1	-	-	-	1	-	-	Δ	0
β_3	-	1	-	-	-	1	1	-	Δ	-	1 V_{DC}
β_4	-	1	1	-	1	-	1	-	∇	-	2 V_{DC}
β_5	1	-	1	-	-	-	-	1	-	Δ	-1 V_{DC}
β_6	1	-	-	1	-	-	-	1	-	∇	-2 V_{DC}

X: state, "1": on-state, "-": off-state, Δ: charging, ∇: discharging, V_o: output

same time.
State-β_4:$V_0 = 2\ V_{DC}$

The output voltage in this state is $V_0 = 2\ V_{DC}$ when switches S_2, S_3, S_5, and S_7 are turned-on. To achieve this, as illustrated in Fig. 2 (d), the capacitor C_1 is discharged.
State-β_5:$V_0 = -1\ V_{DC}$

At this state, the output voltage is $V_0 = -1\ V_{DC}$ when switches S_1, S_3, and S_8 are turned ON. Simultaneously, as seen in Fig. 2 (e), capacitor C_2 is charged to V_{DC} through the conduction of S_6.
State-β_6:$V_0 = -2\ V_{DC}$

The output voltage in this state is $V_0 = -2\ V_{DC}$ when switches S_1, S_4, and S_8 are turned-on. To achieve this, as illustrated in Fig. 2 (f), the capacitor C_2 is discharged.

3. Modulation technique

The suggested inverter has been designed to produce 5-Level output waveforms using a popular phase opposition disposition level-shifted pulse width modulation (POD-LSPWM) to generate gate pulses. This scheme compares four carrier signals (C_1, C_2, C_{11}, C_{22}) at the desired switching frequency with a modulating signal. The control technique is shown in Figs. 3(a-d), with Figs. 3(a-b) corresponding to the positive half cycle and Figs. 3(c-d) to the negative half cycle.

Selection of capacitance

Typical values for the capacitors are a critical challenge for designing the *SC* topologies, which ensure capacitor voltage ripple remains below a defined threshold value. For the calculation of capacitance, the longest discharging time (LDT) of the capacitor plays a crucial role. Therefore, discharging instant. t_1, t_2, t_3, t_4 can be calculated from Fig. 4 as [5]:

$$t_1 = \frac{\arcsin \frac{1}{2}}{2\pi f} \tag{1}$$

$$t_2 = \pi - \frac{\arcsin \frac{1}{2}}{2\pi f} \tag{2}$$

The value of t_3, t_4 can be similarly calculated like equations (1) and (2).

The following is the formula for figuring out the highest discharge values of each capacitor when conditions are at their worst, like when there is only a resistive load:

$$\Delta Q_{C,i} = \int_{t_1}^{t_2} i_0(t)dt \tag{3}$$

$\Delta Q_{C,i}$: maximum discharge during LDT
i_0: Max. load current
For a pure resistive load, the load current becomes $i_0(t) = \frac{2V_{DC}}{R}$

$$\Delta Q_{C,1} = \int_{t_1}^{t_2} \frac{2\ V_{DC}}{R} dt \tag{4}$$

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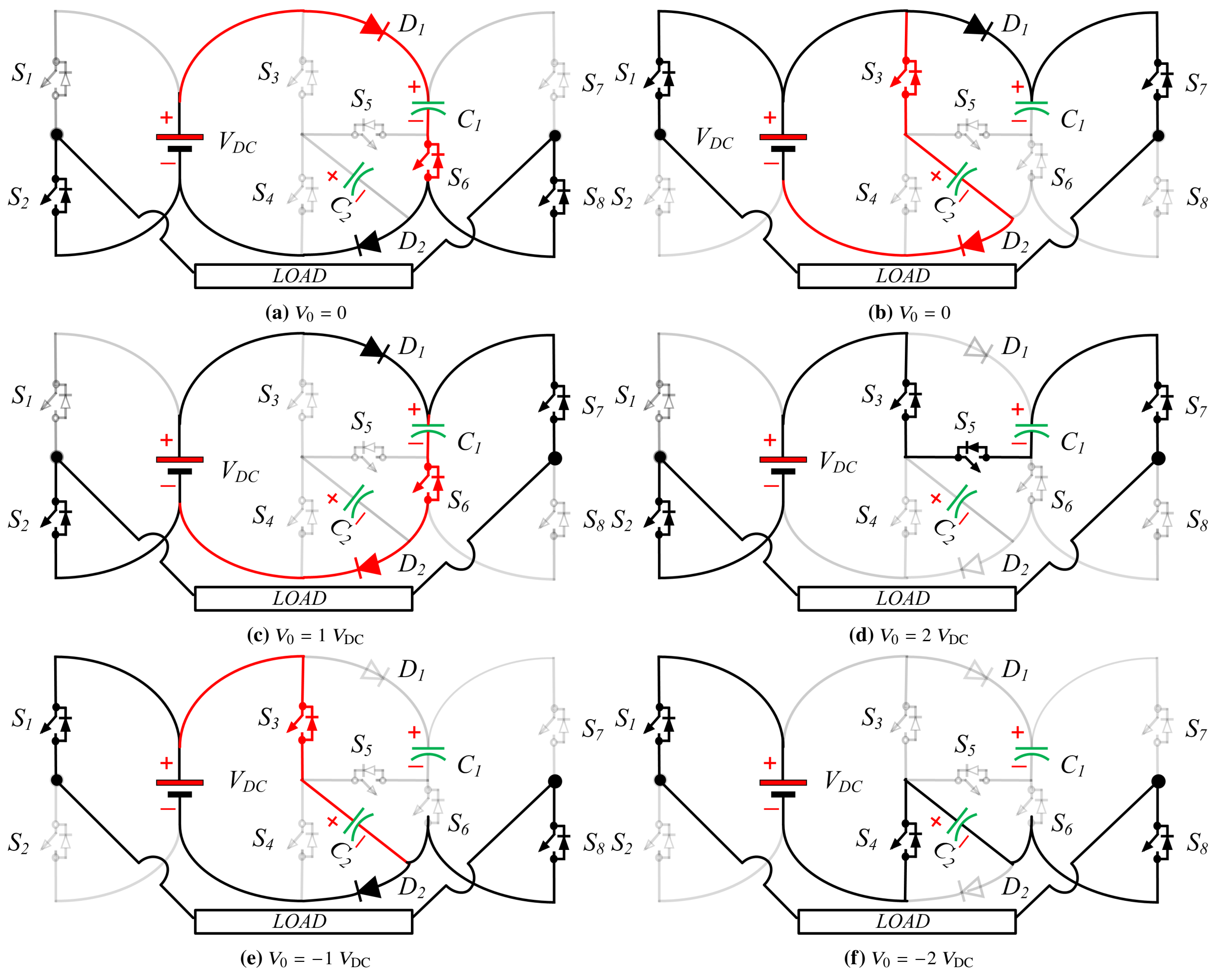

Figure 2. Operation of the SC five-level topology.

Hence, the perfect capacitance may be calculated by considering the allowable voltage ripple, which is 5−10% of the input voltage:

$$C_i \geq \frac{\Delta Q_{C,i}}{\delta V \times V_{\mathrm{DC}}} \tag{5}$$

$$C_1 \geq \frac{2.1}{\pi \times \delta V \times R} \tag{6}$$

Similarly, capacitor C_2 can be calculated.

4. Losses analysis of the proposed SCMLI

There are three forms of total losses in an SCMLI: conduction losses (P_C), switching losses (P_S), and ripple losses (P_r). The diodes and power switches cause the conduction and switching losses, while the capacitors cause the ripple losses.

Conduction losses (P_C):

These losses occur when semiconductor devices are in their on-state. This loss relationship is given as [12]:

$$\begin{aligned} P_C =& (V_{o,sw} I_{a,sw} + I_{rms,sw}^2 R_{o,sw}) + \\ & (V_{o,d} I_{a,d} + I_{d,rms}^2 R_{o,d}) \end{aligned} \tag{7}$$

Switching losses (P_S):

These losses arise during the switching transitions of semiconductor devices, i.e., when they shift from the ON state to the OFF state and vice versa. The corresponding loss can be expressed as [12, 15]

$$P_S = \frac{1}{6} V_{\text{off}} f_{sw}(t) [t_{\text{on}} + t_{\text{off}}] \tag{8}$$

V_{off}: off-state voltage, t_{on} and t_{off} are the turn-on and turn-off durations of the switch.

Ripple losses (P_{rip}):

The variation in capacitor voltage during the discharging process leads to ripple losses.

$$\delta V = \frac{1}{C_i} \int_{t_x}^{t_y} i_{C,i} dt \tag{9}$$

$$P_{rip} = \frac{f}{2} C_i \delta V^2 \tag{10}$$

δV: ripple voltage, (t_x,t_y): discharging time span, $i_{C,i}$: current flowing through the capacitor.

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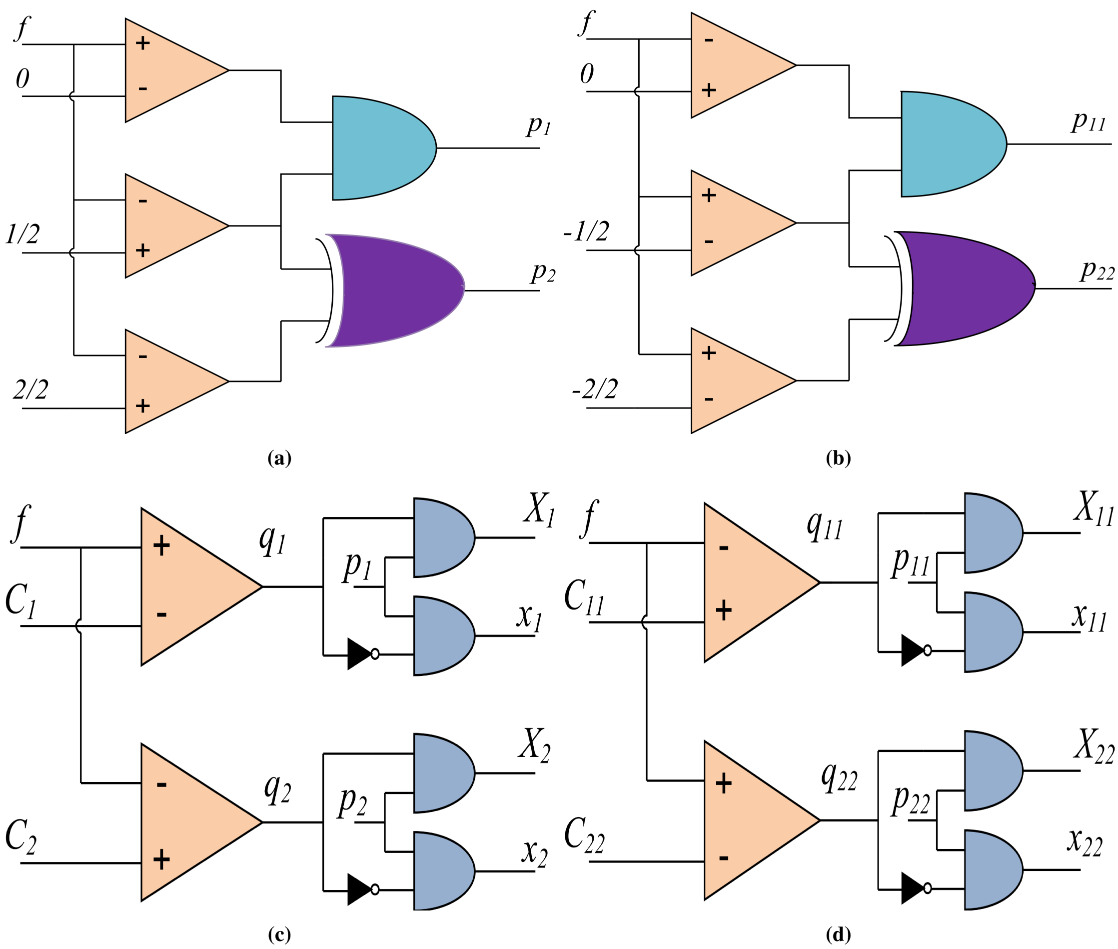

Figure 3. Modulation scheme for (a-b) positive half cycle (c-d) negative half cycle.

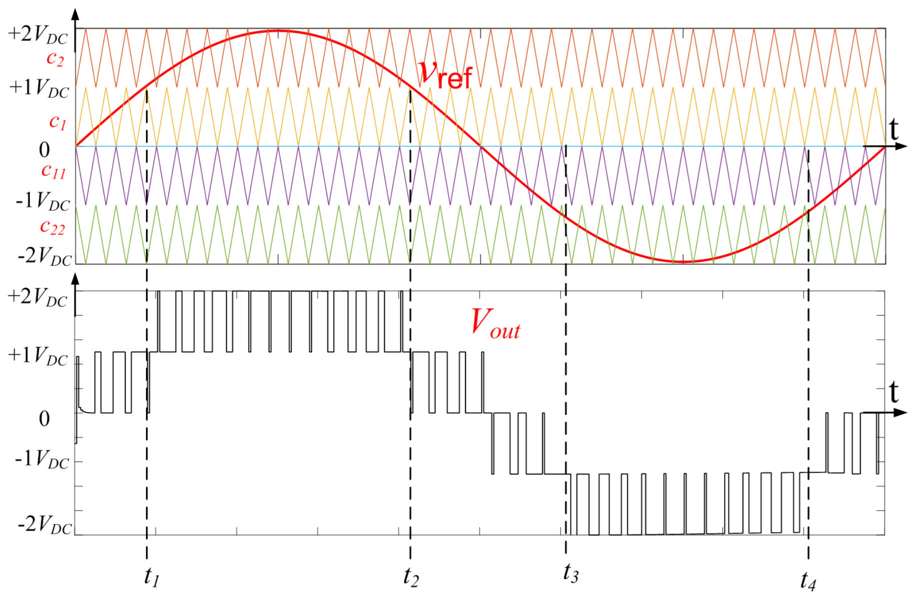

Figure 4. longest discharging instant of the capacitor.

5. Comparative analysis with existing 5-level SCMLI topologies

The comparative cost analysis of various SCMLI topologies underscores the economic feasibility of the proposed design. Table 2 shows how much switches, diodes, capacitors, and driver circuits cost in different topologies. The number and kind of switches have a big effect on both the cost and the complexity of the circuit. For example, the designs in [10] and [11] use a lot more IXTP36N30T switches (six and twelve, respectively),

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which makes them much more expensive. The proposed inverter [PT], on the other hand, uses six IXTP36N30T and two IRFP460PBF devices, which makes it work reliably at a lower cost. When it comes to diodes, topologies like [13] use up to four devices, which raises the cost. The PT, on the other hand, only needs two SBR40U300CTB diodes, which keeps efficiency high with little extra hardware. Capacitors are one of the most expensive parts, so they also affect the total cost. Most topologies, like [9, 10, 11, 13], and [PT], use two 300 V capacitors. However, design [16] uses one 500 V capacitor, which costs a lot more and makes the total cost go up a lot. The PT cuts the number of drivers needed from twelve to eight, making the setup easier and cheaper. When looking at the total costs, [PT] stands out as the most cost-effective design at only 73.44 USD. So, the suggested inverter successfully cuts down on the number of devices and drivers needed, which saves a lot of money while keeping high performance, reliability, and usefulness for practical medium-power uses. Table 3 shows a comparison between the current topologies and the proposed SCMLI in relation to several parameters such as total standing voltage (TSV), voltage gain, capacitors, diodes, and switches. In contrast to inverters [10, 11], and [17], which require 9-12 switches, the suggested inverter [PT] uses just eight, cutting down on switching losses and the number of gate drivers needed. Unlike [13], which needs four diodes, this one utilizes just two, and it matches most topologies with two capacitors, thus it naturally balances itself. [P] achieves a voltage gain of 2, which is higher than [11], which delivers just 1.5, and is on par with several other designs. Notably, the suggested design reduces device stress and expense by achieving a lower TSV of 12, as opposed to 16 in [13] and 20 in [17]. Hence, the PT offers an optimal balance of lower TSV and reliable performance.

6. Results analysis

(a) Results of the simulation:

A comprehensive time-domain simulation has been conducted for the PT supplying an RL load to evaluate the transient behaviour. Table 4 shows the model parameters. The output voltage waveform maintained five distinct levels without distortion when the load varied, as depicted in Fig. 5 (a). The increased discharge current causes the capacitor voltage ripple to temporarily increase, yet it still verifies the natural self-balancing even when the load changes. A change in frequency (like 100 Hz - 2 kHz) shows that the SCMLI keeps the waveform intact and the capacitors balanced over a wide range, depicted in Fig. 5 (b). The inverter automatically changes the number of active levels (5-, 5-, and then 3-level operation) when MI transitions (for example, from 0.95 to 0.5 or from 0.5 to 0.3) shown in Fig. 5 (c). The output voltage follows the command without going too high and the load current rises and falls according to the R-L dynamics. Capacitor voltages stay close to their target, with limited ripple and no need for extra sensors or controllers. The semiconductor losses are illustrated graphically as depicted in Fig. 5 (d).

(b) Results of the experiment:

Table 2. Cost analysis of the proposed inverter.

	Device/Range/Description	Cost ($)	[9]	[10]	[11]	[13]	[15]	[16]	[17]	[PT]
Switch	IXTP36N30T(TO220), 300 V,36 A	2.65	3	6	12	3	5	1	10	6
	IRFP460PBF(TO247), 500 V, 20 A	4.11	4	3	-	4	4	7	2	2
Diode	SBR40U300CTB, 300 V, 40 A	2.11	3	1	2	4	-	1	-	2
	RURU5050(TO-218), 500 V, 50 V	3.1	-	1	-	-	-	-	-	
Capacitor	871-B43415C3218A000, 2100 µF, 300 V	13.83	2	2	2	2	2	1	2	2
	ALF70G222KP500, 2200 µF, 500 V	26.17	-	1	-	-	-	2	-	
Drive	TLP250, 25 kHz	2.18	7	9	12	7	9	8	12	8
Total cost ($)			75.7	128	89.8	75.7	77.9	177	88.5	73.44

*www.mouser.in

Table 3. Comparative analysis with the existing topologies.

Parameter	[3]	[4]	[10]	[6]	[13]	[17]	[11]	[14]	[15]	[16]	[17]	[PT]
a	10	6	9	9	7	8	12	7	9	8	12	8
b	1	3	2	1	4	1	2	3	-	1	-	2
c	1	2	3	2	2	2	2	2	2	2	2	2
d	2	2	2	2	2	2	1.5	2	2	2	2	2
e	14	13	15	14	16	15	11	14	9	14	20	12
f	2	2	2	2	2	2	2	2	2	2	2	2

a. No of switches, b. No. of diodes/inductor, c. No. of capacitors, d. MBV, e. TSV, f. Gain

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Table 4. Parameters for validation of simulation and experimentation.

Item	Specification
V_{DC}	50 V
C_1, C_2	2100 µF
f_{sw}	2000 Hz
f	50 Hz
Diode	SBR40U300CTB, 300 V, 40 A
MOSFETs	IXTP36N30T(TO220), 300 V, 36 A
Driver	TLP250, 25 kHz
load	R = 50, L = 80 mH

*www.mouser.in

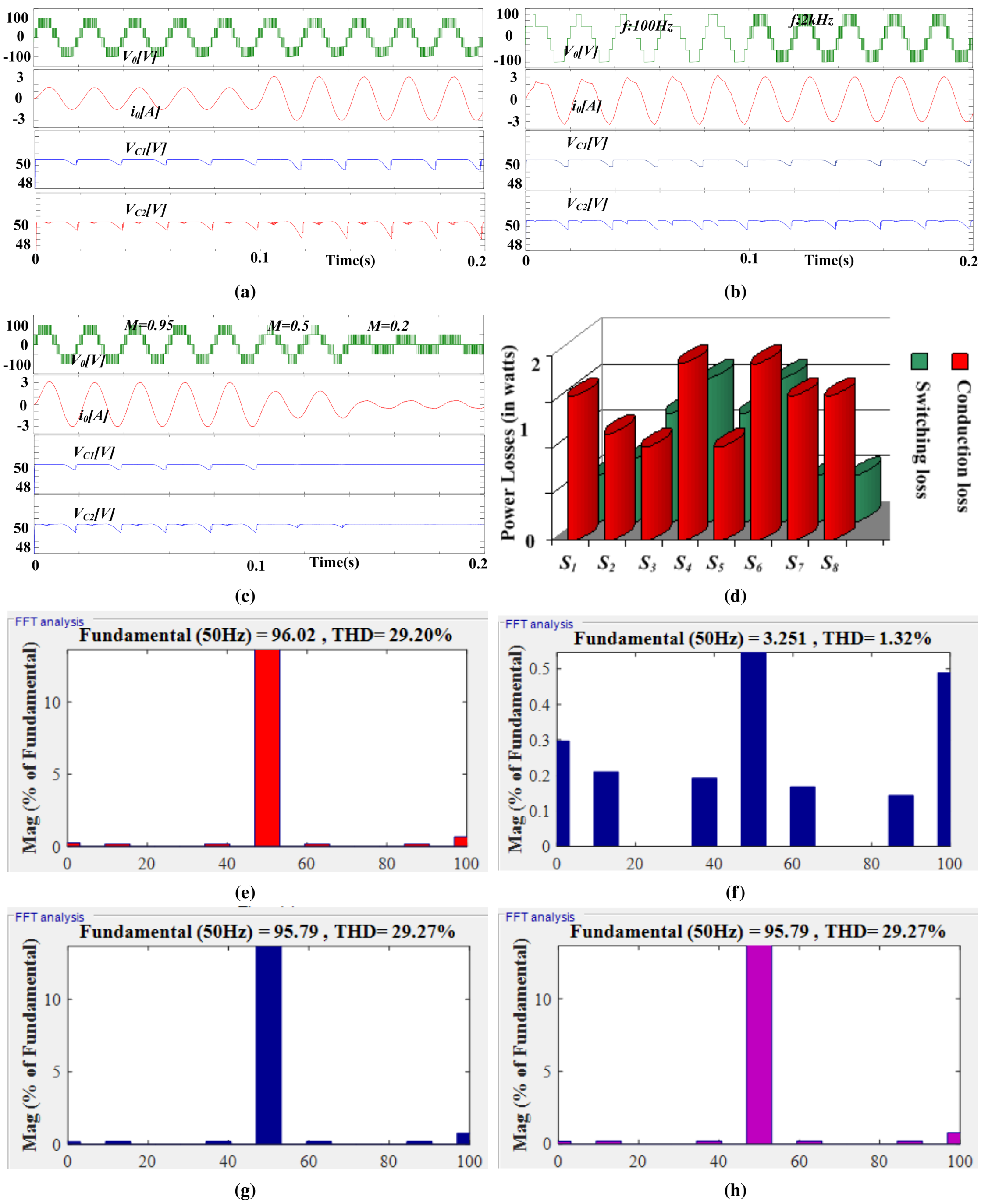

Figure 5. Displays simulation results under transient conditions: (a) load, (b) switching frequency, (c) modulation index, and (d) losses graph; (e) voltage and current THD for RL-load, (g-h) voltage and current THD for R-load.

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Table 4 and Fig. 6 (a) give a summary of the prototype and specification modules. It has been noted that the PT exhibits exceptional dynamic performance, rapidly stabilizes during transients, and inherently equalizes capacitor voltages across an extensive output ranges and the laboratory prototype. To confirm the PT's efficacy, a prototype was created and evaluated under both steady-state and dynamic operational conditions. Figure 6 (b) shows the steady-state performance, which proves that the PT has a self-balancing feature from no load to full

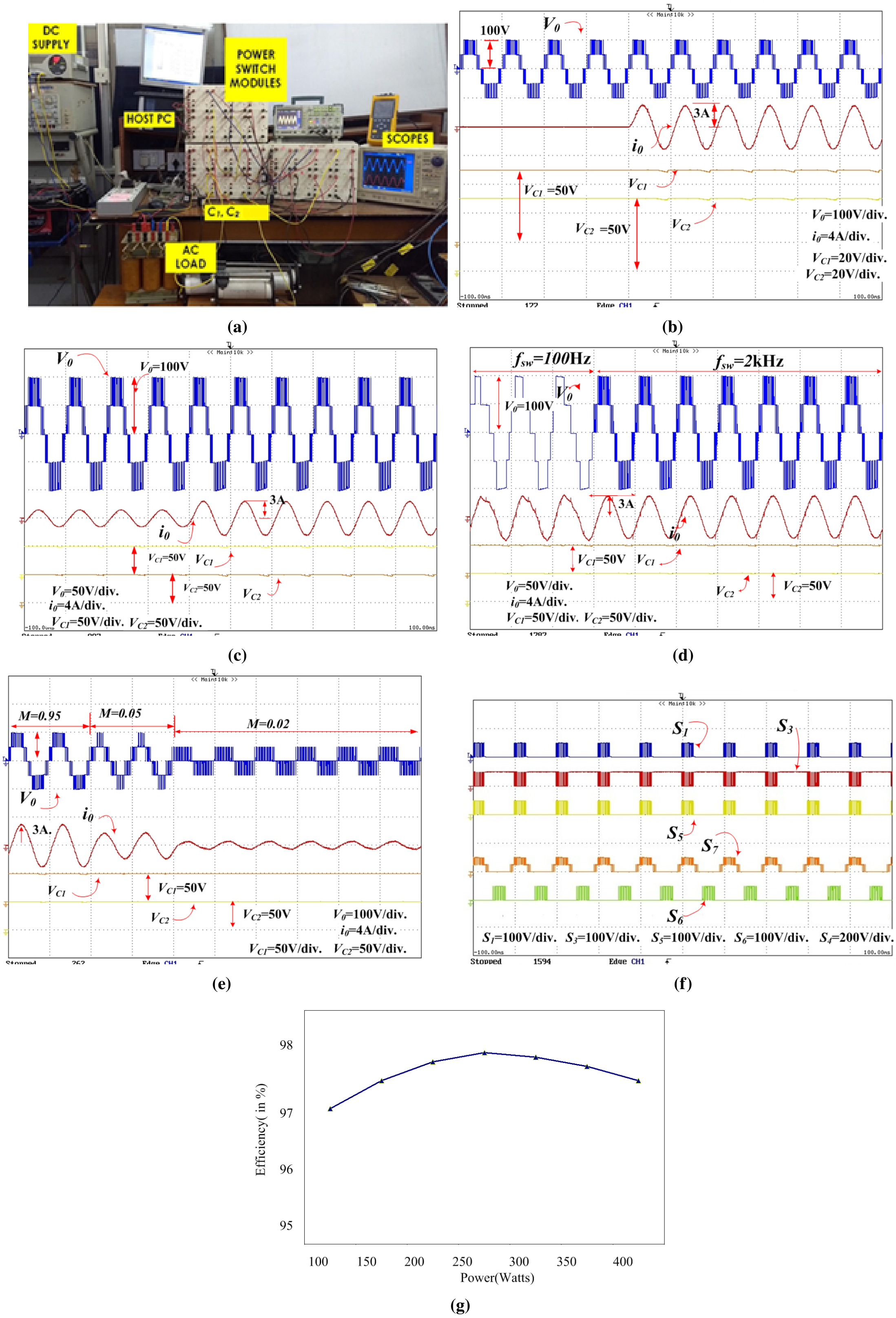

Figure 6. Experimental results: (a) prototype module, (b) No load to load, (c) change in RL-load, (d) switching frequency, (e) modulation index, (f) voltage stresses, (g) efficiency curve.

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load and produces a 5-level output with a peak voltage of 100 V. C_1 and C_2 both have a voltage of 50 V, which keeps the capacitors naturally balanced. No extra devices or sensors are needed. Figure 6 (c-e) shows how the PT responds to variations in load, switching frequency, and modulation index (MI). The results of an experiment with a quick change in load are shown in Fig. 6 (c). Due to the change in load, the output voltage remains intact at 100 V, and capacitor voltages are naturally balanced at a voltage of 50 V. The shift in load shows the PT operates smoothly during the dynamic conditions. The system may also adjust to a 100 Hz to 2 kHz switching frequency change, as shown in Fig. 6 (d). The inverter swiftly adapts to both frequency levels, maintaining consistent transient performance, as seen in the waveforms. Figure 6 (e) displays the effects of MI fluctuation. Three, five levels are produced by the output waveform for MI values of 0.2, 0.5, and 0.95, respectively. The voltage stress across the switches is depicted in Fig. 6 (f). It has been noted that the PT exhibits exceptional dynamic performance, rapidly stabilises during transients, and inherently equalizes capacitor voltages across an extensive output range. Figure 6 (g) shows the effectiveness of the PT under various loads.

7. Conclusion

A single-phase voltage boosting five-level SCMLI is presented in the article. Additionally, the suggested inverter exhibits capacitor self-balancing by naturally removing away with the requirement for voltage sensors or a circuit. It attains a voltage gain of two and a noteworthy TSV_{pu} of 6, and a cost of \$73.44. A thorough comparison analysis demonstrates this topology superiority over current designs. A laboratory prototype is used for experimental validation under different load circumstances, verifying reliable performance in both steady-state and dynamic conditions of the structure.

Authors contributions
All authors contributed equally to the conception, design, execution, and writing of this work. All authors read and approved the final manuscript.

Availability of data and materials
The authors declare that the data supporting the findings of this study are available within the paper.

Conflict of interests
The authors assert that they do not have any identifiable conflicting financial interests or personal relationships that might be perceived to influence the work presented in this paper.

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