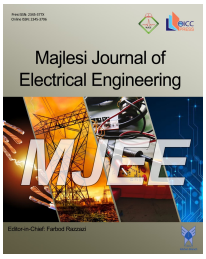

Majlesi J. Electr. Eng. 2026; 20(1) : 113-125

Majlesi Journal of Electrical Engineering (MJEE)

https://dx.doi.org/10.57647/mjee.2026.2001.08

Original Research

A Novel Quadratic High Step-Up Converter Featuring Low Ripple Input Current and Lossless Snubber

Fatemeh Omrani, Majid Delshad*, Bahador Fani

Department of Electrical Engineering, Isf.C, Islamic Azad University, Isfahan, Iran

*Corresponding author: majid.delshad@iau.ac.ir

Article History

Received:
16 October 2025

Revised:
12 December 2025

Accepted:
31 December 2025

Published in Issue:
31 March 2026

Abstract:

This paper introduces a high step-up DC–DC converter that combines a quadratic boost architecture with a flyback stage and incorporates a novel lossless snubber network to enhance efficiency and voltage stress performance. The converter achieves a substantial step-up ratio increase with diminished switch over-voltage, while maintaining soft-switching operation for all semiconductor devices. Consequently, transition-related losses are suppressed and diode reverse-recovery is mitigated. The leakage inductance energy is efficiently captured by the snubber and redirected to the output, contributing to overall performance enhancement. The circuit design is simplified due to the ground-referenced single power switch, which facilitates easier control and gate driving. Moreover, the low input-current ripple renders the converter configuration highly suitable for photovoltaic energy systems. A comprehensive theoretical analysis is conducted, and a 140 W prototype has been built. The experimental results validate the proposed analysis and indicate a 4% efficiency improvement over conventional hard-switched equivalents.

Keywords: Step-up; Quadratic; Lossless snubber; ZVS; ZCS

Cite this article: Omrani F, Delshad M, Fani B. A Novel Quadratic High Step-Up Converter Featuring Low Ripple Input Current and Lossless Snubber. Majlesi J. Electr. Eng. 2026;20(1): 113-125. https://doi.org/10.57647/mjee.2026.2001.08

1. Introduction

In recent years, increasing global concern over environmental pollution and climate change driven by fossil fuel consumption has accelerated research into renewable energy technologies such as photovoltaic systems and fuel cells [1]. A key element within these systems is the High conversion-ratio DC–DC converter, which is essential for elevating the low output voltage of renewable sources to usable levels. However, typical boost design is inadequate for achieving the high voltage gain required, as they necessitate extremely high duty cycles that result in substantial conduction losses and complex control dynamics. Moreover, traditional designs subject semiconductor components to elevated voltage stress and contribute to diode reverse recovery losses. Consequently, advanced converter topologies are being developed to offer Improved voltage boosting capability with reduced device stress, improved efficiency, and minimized reverse recovery effects in diodes [1].

Numerous topologies of non-isolated converters providing large voltage gain have been developed using a variety of techniques. Examples include Z-source converters [2, 3], quasi-Z-source networks [4, 5], switched inductor configurations [6, 7, 8, 9], coupled inductor-based designs [10, 11, 12, 13, 14], voltage multiplier or booster cells [15, 16, 17], switched capacitor approaches [18, 19], and quadratic boost converter structures [20, 21, 22].

Z-source converters are notable for providing substantial voltage boost at relatively low duty cycles [2, 3]. However, Z-source converters present several limitations, including elevated stress imposed on switching elements, discontinuous input current profiles, and Isolation of ground references at the input and output sides. Furthermore, the limited operating range of the converters' duty cycle reduces their usefulness in practical designs for renewable energy DC-DC converters. To address these challenges, interleaved converter structures are utilized to minimize input current ripple and improve overall conversion efficiency [23]. In [4], the Quasi Z-Source

converter achieves soft-switching operation for the power switches through the integration of an auxiliary circuit incorporating coupled inductors. This converter design is the perfect candidate for applications requiring a significant voltage boost. Its topology ensures a stable, uninterrupted input current, effectively minimizes the voltage strain on internal capacitors, and provides the system with a vital common ground connection. Despite these advantages, impedance-source-based networks still suffer from drawbacks such as raised voltage level across the primary switch and a restricted operational duty cycle range, as noted in [24]. Additionally, Y-Source converters, which incorporate three-winding coupled inductors, offer the advantage of high voltage gain. Nevertheless, a significant disadvantage of this particular design is the considerable electrical strain placed upon the power-switching components, which consequently leads to an increase in power dissipated as heat, or greater conduction losses [25, 26].

In [20], a quadratic converter topology is presented that enhances the step-up conversion performance and reduces voltage stress on the switch by employing coupled inductors (CIs) along with a voltage doubler cell. Quadratic boost converters offer several benefits, including common grounding of input and output alongside high voltage amplification at relatively low duty cycles, and a reduced count of circuit elements. However, these converters typically experience a significant voltage strain on the power components, and their implementation cost is elevated due to the use of separate switches for each boost stage. To address these issues, a single-switch quadratic boost converter is suggested in [21], offering decreased voltage stress and an exceptionally high voltage gain. Nevertheless, its main drawback is the hard-switching behavior of the devices, which leads to higher levels of electromagnetic interference (EMI) and switching losses. In the converter proposed in [22], the integration of a quadratic structure with switched capacitor (SC) cells results in an improved voltage gain. However, this topology presents certain limitations, including lack of a shared ground between the input and output, as well as significant input current ripple.

In active clamping techniques, an auxiliary switch is employed to recover leakage energy and mitigate the excessive main switch voltage burden [27]. This approach can facilitate Zero Voltage Switching (ZVS), reduce the required duty cycle, and typically involves employing a magnetically coupled inductor in conjunction with a high turns ratio to enhance performance [28, 29]. To enhance converter performance, [30] employ voltage boosting techniques in combination with coupled inductors (CIs) or built-in transformers (BITs). Furthermore, a soft-switching cell consisting of an auxiliary MOSFET, a diode, and a coupled inductor is incorporated to enable ZVS, thereby minimizing capacitive turn-on losses and switching losses [31]. The converters proposed in [32, 33, 34] employ three-winding coupled inductors (TWCI) to achieve low input current, high voltage gain, and single-switch operation. These designs utilize leakage inductance to mitigate reverse recovery issues in diodes. However, they encounter challenges in efficiently recycling the energy stored in the leakage inductance, necessitating the inclusion of additional components to optimize performance. The researchers in [35] employed a hybrid approach to improve voltage amplification, merging a Passive Switched Capacitor network with an Active Switched Inductor circuit (ASL). However, the converter suffers from drawbacks such as a complex control circuit and voltage oscillations across the switches.

A novel quadratic converter is introduced that is capable of delivering an elevated voltage gain and reduced switch voltage without using an additional soft-switching device, which simplifies control implementation. The incorporated lossless snubber circuit not only avoids increasing switch voltage stress but also efficiently recycles its energy to the output. Omitting coupled inductors in the auxiliary circuit allows for a more compact and cost-effective design. Moreover, the converter's smooth input current profile and shared input–output ground make it an excellent candidate to interface with power sources such as PV arrays and fuel cells.

A comprehensive analysis of the converter's configuration and its method of operation is presented within the confines of section 2 of this paper. Section 3 provides an analytical study supported by the necessary component design equations. Section 4 details the empirical results that confirm the theories developed earlier, and section 5 concludes with a comprehensive evaluation of the converter's power dissipation.

2. Technical work preparation

The topological structure for the presented high step-up converter can be observed in Fig. 1. This topology integrates the quadratic boost and flyback converter principles to achieve an enhanced voltage gain. The converter incorporates an input inductor L_{in}, a switch S, a coupled inductor N_1-N_2, an auxiliary inductor L_a, diodes (D_1, D_2, D_3, D_4, D_5, D_6) and five capacitors (C_1, C_2, C_3, C_{O1}, C_{O2}). The converter utilizes a single switching device activated by a PWM control input, which simplifies the overall control circuitry. The snubber network (comprising an auxiliary inductor, capacitors C_2 and C_3, and diodes D_4 and D_5), is designed to enable ZCS during turn-on the switch. Additionally, due to the presence of the snubber capacitors, the switch is turned off under ZVS conditions, thereby reducing switching losses and improving efficiency.

2.1 Functional description of the converter

Figure 2 illustrates the switching waveforms of the presented high step-up converter over a complete switching cycle. The converter operates through eight distinct modes within each cycle. A detailed explanation of the converter's functionality in each mode is provided.

For the sake of simplifying the analytical process, the subsequent assumptions are adopted:

- All components are ideal.

https://dx.doi.org/10.57647/mjee.2026.2001.08

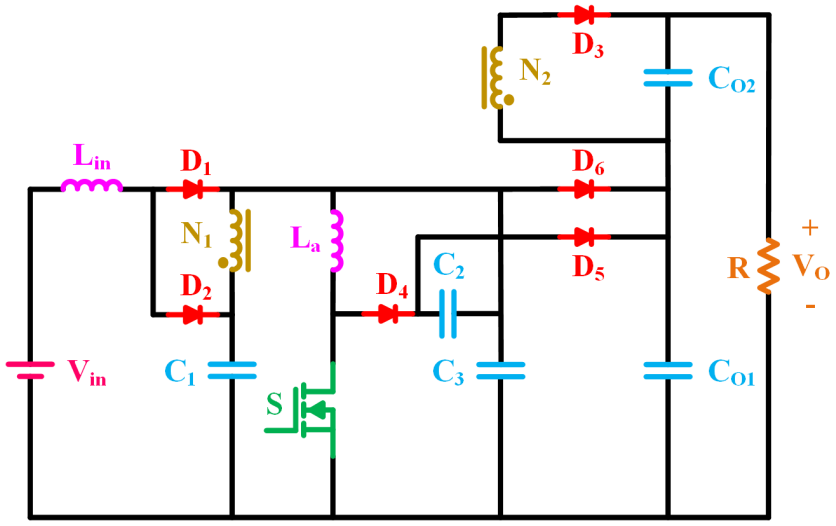

Figure 1. Circuit arrangement of the converter.

- C_1, C_{O1}, and C_{O2} have large capacitances, keeping their voltages constant during switching.

Refer to figure 3 to see the simplified circuit representation of the converter as it shifts through its different operational modes.

Before Mode 1: In the switch's OFF state, the simultaneous conduction of D_2, D_3, and D_6 occurs. The circuit dynamics are set such that V_{C3} equals V_{Co1} and V_{c2} drops to zero. A key action in this mode is the delivery of the coupled inductor's stored energy to the final output.

Mode 1 (t_0-t_1): The operational mode commences the moment switch S is activated. As this occurs, the current passing through S begins to rise at a rate that is precisely controlled by the value of the series inductor L_a, allowing S to turn on under ZCS conditions. Consequently, the current through L_a increases linearly, while the current through D_6 decreases linearly. The voltage V_{CO1} is applied across L_a. During this interval, diode D_3 turns off under ZCS conditions. The mode concludes when the current through switch S reaches I_{in}.

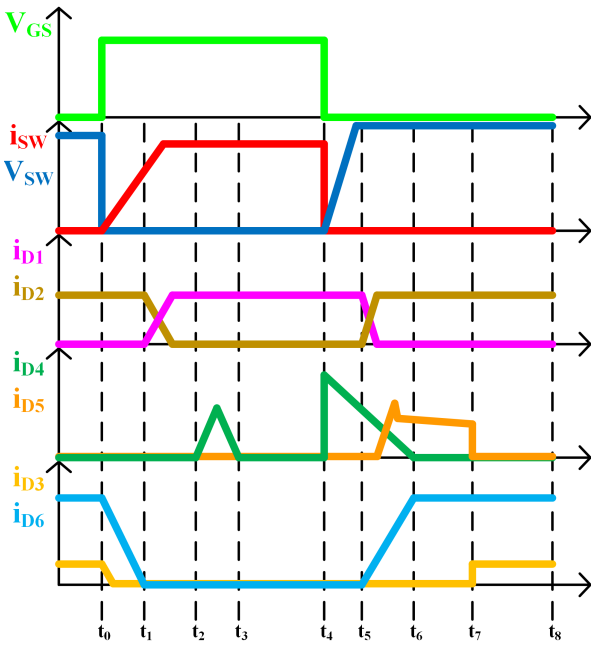

Figure 2. Graphical display of the converter's key operating waveforms.

Mode 2 (t_1-t_2): At time t_1, the current through D_6 becomes zero, causing it to turn off under ZVS conditions due to the presence of capacitor C_3. When the current through S reaches I_{in}, the current through D_2 starts to decrease, while the current through D_1 increases, transferring the input current from D_2 to D_1. As a result, D_2 turns off and D_1 turns on under ZCS conditions. At this stage, a resonant interaction occurs between L_a and C_3, leading to an increase in the current through L_a and a sinusoidal decrease in the voltage across C_3. The current through L_a consists of the sum of I_{in} and I_{C3}. The initial conditions for this state are $V_{C3}(t_1) = V_{CO1}$ and $I_{La}(t_1) = I_{in}$. The mode ends when V_{C3} falls to zero.

Mode 3 (t_2-t_3): To initiate this state, when the voltage across C_3 becomes zero, D_4 starts conducting under ZVZCS (Zero Voltage Zero Current Switching) conditions. The resonance between C_3 and L_a continues, discharging the voltage across C_3. Additionally, a new resonance occurs between C_2 and L_a, which increases the voltage across C_2. In this operating state, the voltage across capacitor C_3 becomes negative and reaches its peak magnitude at time t_3. The combined voltage of C_3 and output capacitor V_{CO1} represents the maximum reverse voltage stress applied to diode D_6. During this interval, resonant behavior is observed through two distinct paths: L_a-D_4-C_2 and L_a-S-C_3. The state concludes when the turn-off of diode D_4 occurs under ZCS conditions.

Mode 4 (t_3-t_4): This state is triggered by the turn-off of diode D_4, leading to the clamping of capacitor C_3 at zero voltage. Throughout this interval, the main switch S conducts a constant input current I_{in}, and the output capacitors C_{O1} and C_{O2} supply the load current. Upon the deactivation of the main switch, diode D_4 resumes conduction, marking the end of this mode.

https://dx.doi.org/10.57647/mjee.2026.2001.08

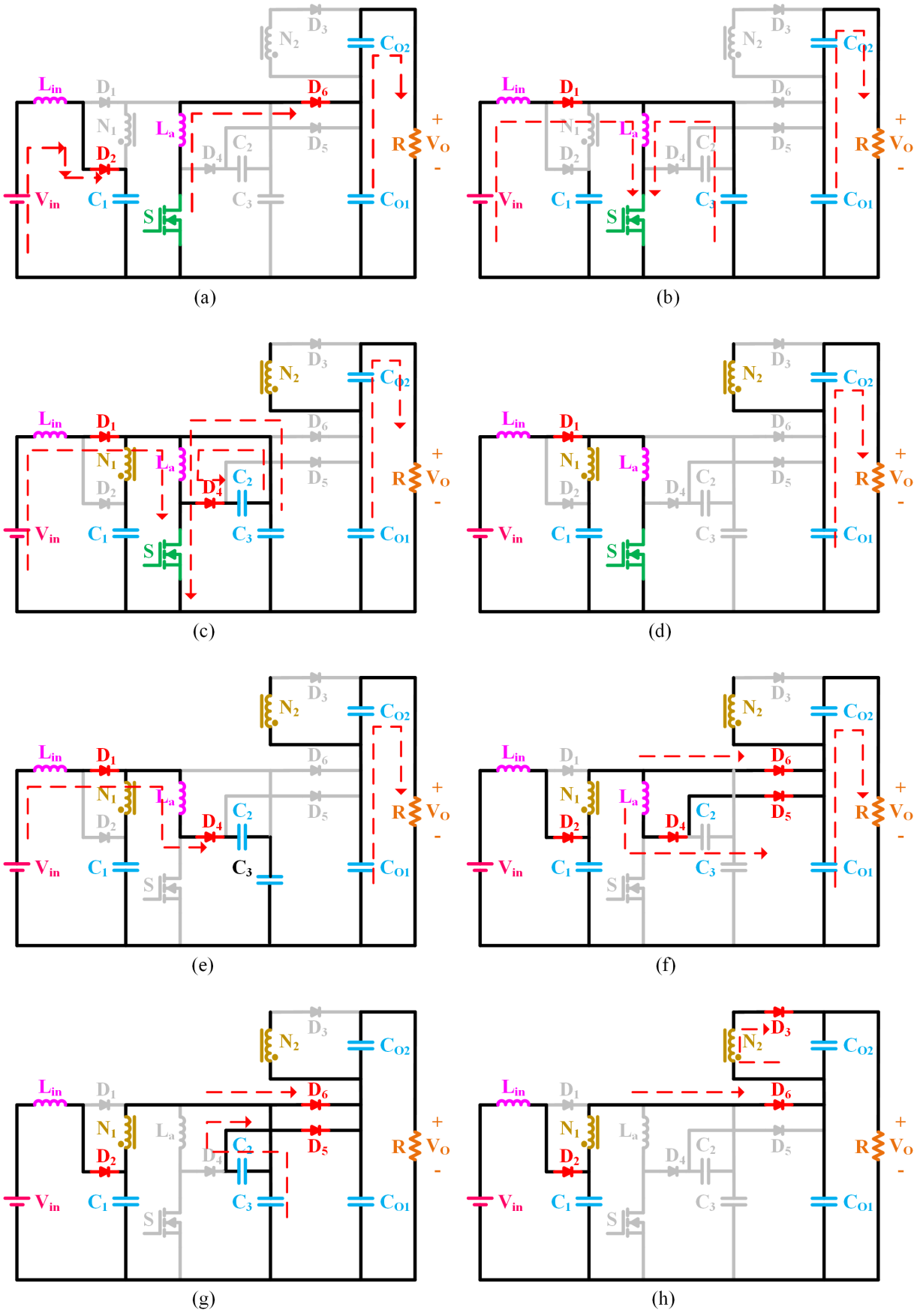

Figure 3. Illustrates the sequence of all eight distinct operational modes (Mode 1(a) through Mode 8(h)).

https://dx.doi.org/10.57647/mjee.2026.2001.08

Mode 5 (t_4-t_5): Switch S is deactivated in this stage of operation and the input current linearly charges capacitor C_3, causing switch S to turn off under ZVS conditions. Diode D_4 starts conducting, and a resonance occurs between C_2 and L_a, causing capacitor C_2 to charge resonantly. In this state, Diode D_6 becomes forward-biased under ZVS conditions when V_{C3} rises to V_{CO1}. This state concludes when the current conducted by D_1 commences its reduction, and the current through D_2 begins to increase.

Mode 6 (t_5-t_6): In this state, the current through D_1 starts to decrease, while the current through D_2 starts to increase, and capacitor C_1 begins to charge linearly. Meanwhile, diode D_5 conducts, and the voltages across capacitors C_2 and C_3 are clamped at V_{CO1}. This state ends when D_4 turns off under ZCS conditions.

Mode 7 (t_6-t_7): This mode commences with the turn-off of diode D_4. During this interval, capacitors C_2 and C_3 discharge their stored energy into the output capacitor. This state concludes with the turn-off of diode D_5 under ZVS operation, and diode D_3 turns on.

Mode 8 (t_7-t_8): During this interval, diode D_5 is turned off under ZVS conditions, while diode D_3 starts to conduct. The coupled inductor's reservoir of energy is supplied to the load using D_3. The mode concludes when S is switched on.

3. Converter analytical evaluation

In this section, a detailed analytical evaluation of the converter is carried out. The voltage conversion ratio is derived for both CCM and DCM to fully characterize the converter's steady-state performance. Furthermore, this section evaluates the voltage burden imposed on the converter's semiconductor elements, and detailed guidelines for the design of passive components are provided.

3.1 Converter gain

The voltage gain relationship for the converter under CCM is mathematically derived using the fundamental principle of volt-second balance, considering the input and magnetizing inductor L_m. The resulting expression is provided in equation (7). To illustrate the behavior of the converter, figure 4 displays the ideal voltage gain for a perfect coupling condition (k = 1), while figure 5 compares the gain characteristics under different coupling coefficients, highlighting the impact of magnetic coupling on the overall performance.

$$V_{in}DT_S + (V_{in} - V_{C1})(1 - D)T_S = 0 \tag{1}$$

$$V_{C1} = \frac{1}{(1 - D)}V_{in} \tag{2}$$

$$V_{Lm}^1 = \frac{L_m}{L_k + L_m}V_{C1} = KV_{C1} \tag{3}$$

$$V_{CO2} = nV_{Lm}^1 \tag{4}$$

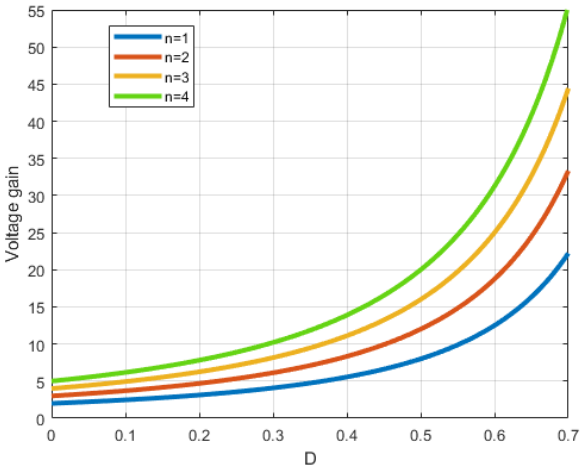

Figure 4. The dependence of the voltage gain on the turn ratio and the duty cycle.

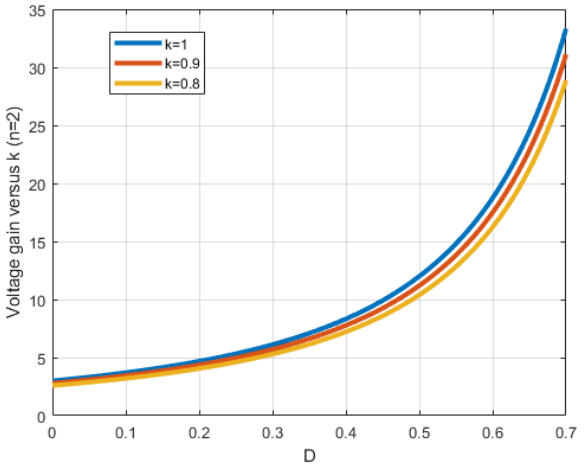

Figure 5. Influence of the coupling coefficient on voltage gain.

$$V_{CO1} = \frac{1}{(1 - D)^2}V_{in} = \frac{V_O}{1 + nK} \tag{5}$$

$$V_{CO2} = \frac{nk}{(1 - D)^2}DV_{in} = \frac{nKD}{1 + nK}V_O \tag{6}$$

$$M = \frac{V_O}{V_{in}} = \frac{1 + nK}{(1 - D)^2} \tag{7}$$

In discontinuous conduction mode (DCM), the proposed converter exhibits a third operating interval in which both the main switch and all diodes are off, causing the magnetizing and input inductors to fully discharge while the output capacitor momentarily supplies the load. Under ideal coupling (K = 1), the magnetizing inductor experiences the input voltage during the switch-on interval, resulting in a linear current rise and enabling the peak current to be expressed in terms of the duty cycle, switching frequency, and inductance value. Using this peak value, the average input current and corresponding input power are obtained from the triangular waveform of L_m. Assuming lossless operation, this input power equals the output power delivered through the coupled-inductor, whose intrinsic gain contributes a factor of

(1 + n). Equating the derived input and output power expressions yields the closed-form DCM voltage gain and provides the basis for identifying the boundary between CCM and DCM, which depends on the duty ratio, load resistance, magnetizing inductance, and switching frequency. Figure 6 shows the CCM-DCM boundary of the converter versus magnetizing inductance.

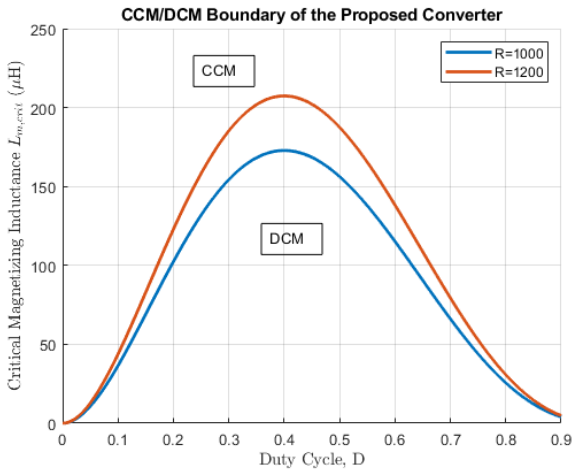

Figure 6. The CCM-DCM boundary of the converter versus magnetizing inductance.

$$i_{Lm}(0) = 0, \quad i_{Lm}(T_s) = 0 \tag{8}$$

$$I_{pk} = \frac{V_{in}D}{L_m f_s} \tag{9}$$

$$I_{in,avg} = \frac{1}{2} I_{pk} D \tag{10}$$

$$P_{in} = V_{in} I_{in,avg} = \frac{V_{in}^2 D^2}{2 L_m f_s} \tag{11}$$

$$P_{out} = \frac{V_o^2}{R} \tag{12}$$

$$P_{in} = P_{out} \tag{13}$$

$$M_{DCM} = (1+n)\frac{D}{\sqrt{2(1-D)}}\sqrt{\frac{R}{L_m f_s}} \tag{14}$$

3.2 Voltage stress of switch and diodes

In order to determine the voltage stress on the converter's components operating in CCM, it is enough to analyze the voltage across each device during its off-state using appropriate Kirchhoff's Voltage Law (KVL) equations. The following equations represent the resulting voltage stresses on the semiconductor elements.

$$V_S(\max) = \frac{V_O}{(1+n)} \tag{15}$$

$$V_{D1}(\max) = \frac{(1-D)V_O}{(1+n)} \tag{16}$$

$$V_{D2}(\max) = \frac{DV_O}{(1+n)} \tag{17}$$

$$V_{D3}(\max) = \frac{nV_O}{(1+n)} \tag{18}$$

$$V_{D6}(\max) = \frac{V_O}{(1+n)} \tag{19}$$

The normalized voltage stress profiles for the converter's semiconductor devices are presented in figure 7.

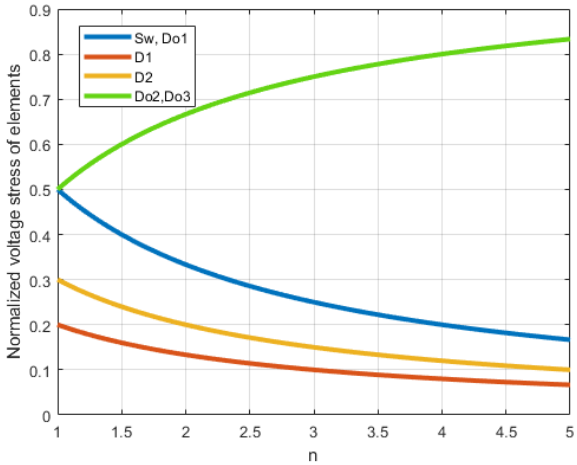

Figure 7. The voltage stress ratio of elements.

3.3 Design considerations for converter passive elements

This section provides the analytical expressions for the passive elements of the converter. The input inductor is determined using equation (20), considering the permissible current ripple. Additionally, the calculation of the coupled inductors' magnetizing inductance relies on the principle of the switching frequency, peak current, and the converter's output power, as shown in equation (21).

$$L_{in} = \frac{V_{in} \cdot D}{\Delta i_L \cdot f} \tag{20}$$

$$L_m = \frac{2P_o}{I_{peak}^2 \cdot f} \tag{21}$$

Capacitor C_1 undergoes charging from the input current during the switch-off interval, which leads to the establishment of the following expression.

$$C_1 = \frac{(1-D)I_{in})}{\Delta V_{C1} f)} \tag{22}$$

Capacitor C_2 functions as a snubber element, facilitating ZVS during the turn-off transition of the switch. Its value can be readily calculated using the conventional snubber capacitor design formula provided below

$$C_2 = \frac{I_{sw} t_f}{2V_{sw}} \tag{23}$$

https://dx.doi.org/10.57647/mjee.2026.2001.08

$$L_a = \frac{V_{sw} t_r}{I_{sw}} \tag{24}$$

$$C_3 < \frac{I_{sw}^2 L_a - V_{C2}^2 C_2}{V_{C3}^2} \tag{25}$$

The sizing of the buffer capacitor C_3 is derived using the energy conservation principle. With known values of L_a and C_2, the required capacitance for C_3 can be directly obtained. Likewise, C_{o1} and C_{o2} are calculated based on fundamental capacitor design equations, as outlined below

$$C_{o1} = \frac{V_{Co1} D}{Rf \Delta V_{Co1}} \tag{26}$$

$$C_{o2} = \frac{V_{Co2} D}{Rf \Delta V_{Co2}} \tag{27}$$

4. Experimental verification of the proposed converter

The converter was physically constructed and underwent lab-based experimental testing. The resulting data successfully confirmed that the built circuit operates correctly. The specifications and component values of the developed converter are summarized in Table 1 and the implemented converter is shown in Fig. 8. Figure 9 presents the experimentally recorded voltage and current characteristics for switch S, the currents of diodes D_1-D_6, and I_{in}, demonstrating its operational behavior under practical conditions. Figure 9 (a) provides a view

Table 1. Design specifications and element values of the proposed converter.

Parameter/element	Part no./ value
Diodes	BYV29-500 V_F = 0.9 V
Switch	STU7NF25 $R_{DS(on)}$ = 0.29 Ω C_{oss} = 90 pF
C_1-C_{O1}-C_{O2}	10 µF
C_2	47 nF
C_3	10 nF
L_{in}-N1	200 µH
N_2	800 µH
L_a	10 µH
PO	140 W
Input voltage	48 V
Output voltage	280 V
Switching frequency	100 kHz

of the voltage and current waveforms associated with the converter's single switching device. The presence of a current slope during the turn-on interval confirms that ZCS is effectively achieved. Notably, the switch voltage remains free of overshoot, distinguishing it from conventional snubber-based circuits. The current characteristics for each of the converter's diodes are illustrated across Figs. 9 (b) to 9 (e). Thanks to the leakage inductance introduced by the coupled inductors, each diode turns off under ZCS operation, effectively minimizing reverse-recovery losses. Figure 9 (f) illustrates the converter's input current waveform, which exhibits a ripple of only 0.2 A, emphasizing the minimal input current ripple inherent in the new converter design.

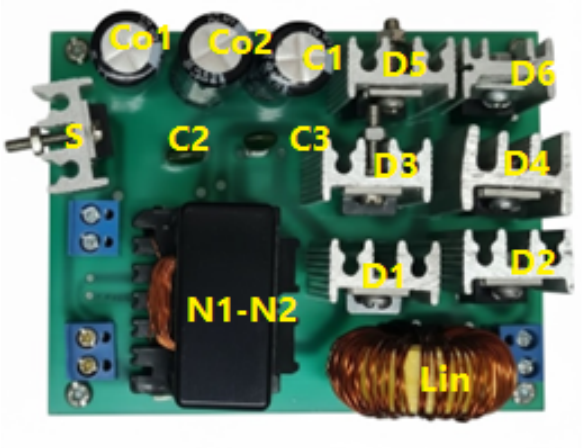

Figure 8. Laboratory prototype of the converter design.

5. Loss analysis

This section presents an analysis of the power losses in the proposed converter. Due to the implementation of soft-switching techniques, the switching losses are minimal and can be reasonably neglected. Accordingly, the loss evaluation focuses on the conduction losses and the capacitive turn-on losses of the switches. These losses are quantified using the available parameters, yielding the following results.

$$R_{DS}(on) \times I_{RMS,Si}^2 nrm_{60^\circ C}^* = 0.29 \times 1.72^2 \times 1.3 = 1.11 \text{ W} \tag{28}$$

$$\frac{1}{2} C_{oss} \times V_{Si}^2 \times f = 0.5 \times 90 \times 10^{-12} \times 95^2 \times 10^5 = 0.04 \text{ W} \tag{29}$$

The total power dissipation in the diodes is largely influenced by the forward voltage characteristics and the average conduction current of each diode, as formulated in equation (20).

$$V_{F,D} \times (I_{av,D_1} + I_{av,D_2} + I_{av,D_3} + I_{av,D_1} + I_{av,D_2} + I_{av,D_3}) = 0.9 \times (1.72 + 1.21 + 0.31 + .56 + .56 + 0.21) = 4.11 \text{ W} \tag{30}$$

Inductor power dissipation arises primarily from the resistive losses in the windings, which scale with the square of the RMS current. The corresponding losses are determined using the following expression.

$$R_{DC,L_{in}} \times I_{RMS,L_{in}}^2 + R_{DC,L_{N1}} \times I_{RMS,L_{N1}}^2 + R_{DC,L_{N2}} \times I_{RMS,L_{N2}}^2 = 0.03 \times 3.13 + 0.11 \times 3.24 + 0.24 \times 1.16 = 0.73 \text{ W} \tag{31}$$

https://dx.doi.org/10.57647/mjee.2026.2001.08

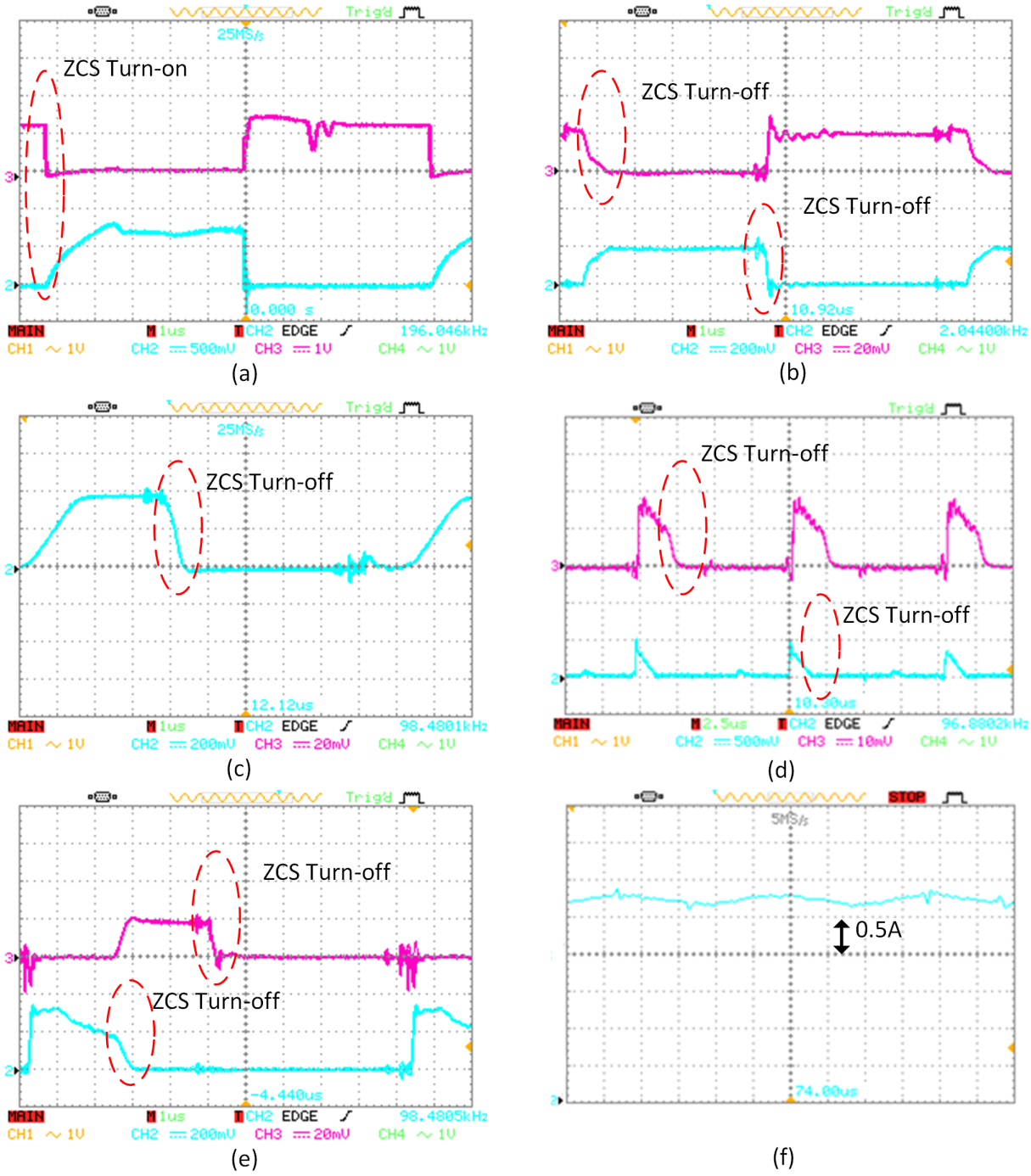

Figure 9. The practical waveforms (a) voltage (up) and current (bottom) of switch S (b) current of diode D_2 (up) and diode D_1 (bottom), (c) current of diode D_3 (d) current of diode D_5 (up) and diode D_4 (bottom) (e) current of diode D_6 (up) and diode D_5 (bottom), (f) waveform of the input current (I_{in}).

The resistive losses in the converter's electrolytic capacitors, due to their equivalent series resistance, are quantified below. Meanwhile, the snubber capacitor losses are disregarded in this study because of their negligible magnitude, stemming from their small capacitance and polyester dielectric properties.

$$ESR_{C1} \times I^2_{RMS,C1} + ESR_{Co1} \times I_{RMS,Co1} + ESR_{Co2} \times I^2_{RMS,Co2} = 0.05 \times (3.67 + 1.02 + 2.01) = 0.34 \text{ W} \quad (32)$$

As indicated by the loss analysis at full-load operation, the converter maintains a high efficiency of 95.7%, owing to its relatively low total power dissipation. Figure 10 illustrates the share of individual components in the total loss through a pie chart.

The operational efficiency of the presented converter is compared to the performance of a traditional design utilizing hard-switching techniques, as depicted in figure 11 which indicating an efficiency improvement of approximately 4% under full-load conditions. Nonetheless, a reduction in output power leads to a noticeable efficiency decline, which can be attributed to the rel-

https://dx.doi.org/10.57647/mjee.2026.2001.08

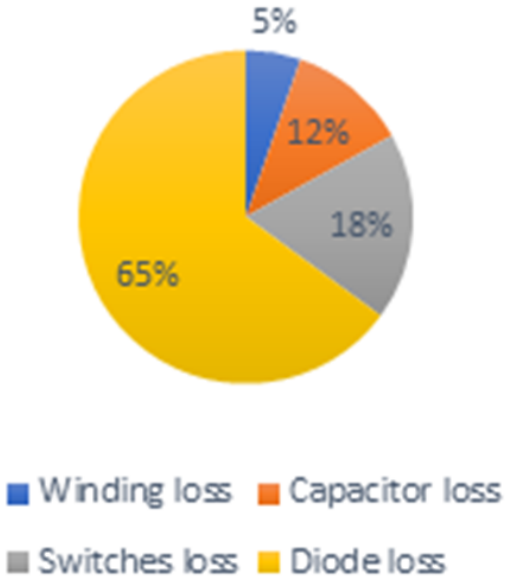

Figure 10. The converter power loss breakdown.

atively constant current drawn by the auxiliary circuit during light-load operation.

6. Comparative performance analysis

As summarized in Table 2, converters [22], [19], and [25] operate under hard-switching conditions, which results in increased switching losses and, consequently, lower overall efficiency. In addition, converters [19], [20], and [25] require a greater number of components, increasing circuit complexity. Moreover, converters [20], [18], and [25] suffer from high voltage stress across their diodes, whereas the new topology features significantly reduced maximum diode voltage stress. From the voltage gain perspective, as illustrated in Fig. 4. The presented design demonstrates a superior gain compared with the other counterparts. Overall, converters [14] and [22] demonstrate inferior performance when compared with the proposed design.

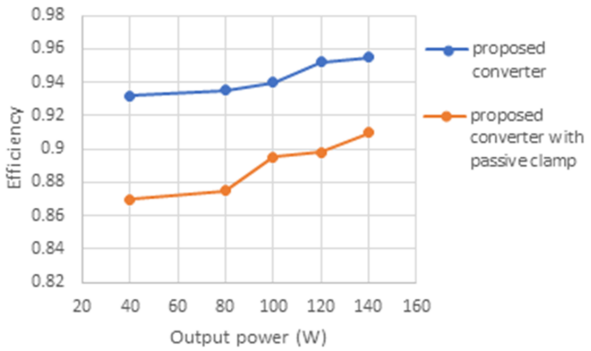

Figure 11. The measured efficiency of the proposed converter is compared with that of its hard-switched counterpart.

A comparative evaluation of the snubber structures shows that the proposed topology offers a more favorable performance profile compared to existing designs. It achieves a lower overall component count while maintaining comparable switching-stress levels. A key advantage of the proposed snubber is the elimination of the coupled inductor, which simplifies implementation, reduces magnetic complexity, and improves practical feasibility. The radar comparison clearly illustrates that the proposed structure provides a more balanced and efficient design, making it a strong candidate for high-performance converter applications. To evaluate the performance of the proposed converter, the variations of voltage gain and normalized voltage stresses of the switch and diodes versus duty cycle are illustrated in Fig. 12. Also, to provide a structural and performance comparison among different high-gain converter topologies, a radar chart illustrating the key design and stress-related features is presented in Fig. 13.

7. Conclusion

A new quadratic converter is presented, featuring both a high step-up ratio and single active switch soft-switching operation. The topology effectively combines a quadratic boost structure with a flyback component, which results

Table 2. Comparative performance table.

Converter	Voltage gain	Maximum voltage stress across switch	Maximum voltage stress across diode	No. of elements					Switching condition	Common Ground
				S	D	C	M.C*	T		
[14]	$\frac{n+2}{1-D}$	$\frac{V_o}{n+2}$	$\frac{(2n+3)}{n+2}V_o$	1	3	3	2	9	ZCS	Yes
[22]	$\frac{2D}{(1-D)^2}$	$\frac{(3D-1)V_o}{2D}$	$\frac{V_o}{2}$	2	6	4	4	14	Hard	Yes
[18]	$\frac{3+D}{1-D}$	$\frac{2V_o}{3+D}$	V_o	2	7	3	4	16	Hard	Yes
[20]	$\frac{n+2}{1-D}$	$\frac{V_o}{n+2}$	V_o	1	3	3	1	10	ZCS-ZVS	Yes
[19]	$\frac{D^2}{(1-D)^2}$	$\frac{V_o}{D^2}$	$\frac{V_o}{D}$	2	2	3	3	10	Hard	Yes
[21]	$\frac{1-2D^2+2D}{(1-D)^2}$	$\frac{V_o}{1-2D^2+2D}$	$\frac{V_o}{1-2D^2+2D}$	1	5	4	6	16	Hard	No
[25]	$\frac{2}{(1-D)^2}$	V_o	V_o	1	5	3	3	12	Hard	Yes
Proposed Converter	$\frac{1+n}{(1-D)^2}$	$\frac{V_o}{1+n}$	$\frac{nV_o}{1+n}$	1	6	5	3	15	ZCS-ZVS	Yes

https://dx.doi.org/10.57647/mjee.2026.2001.08

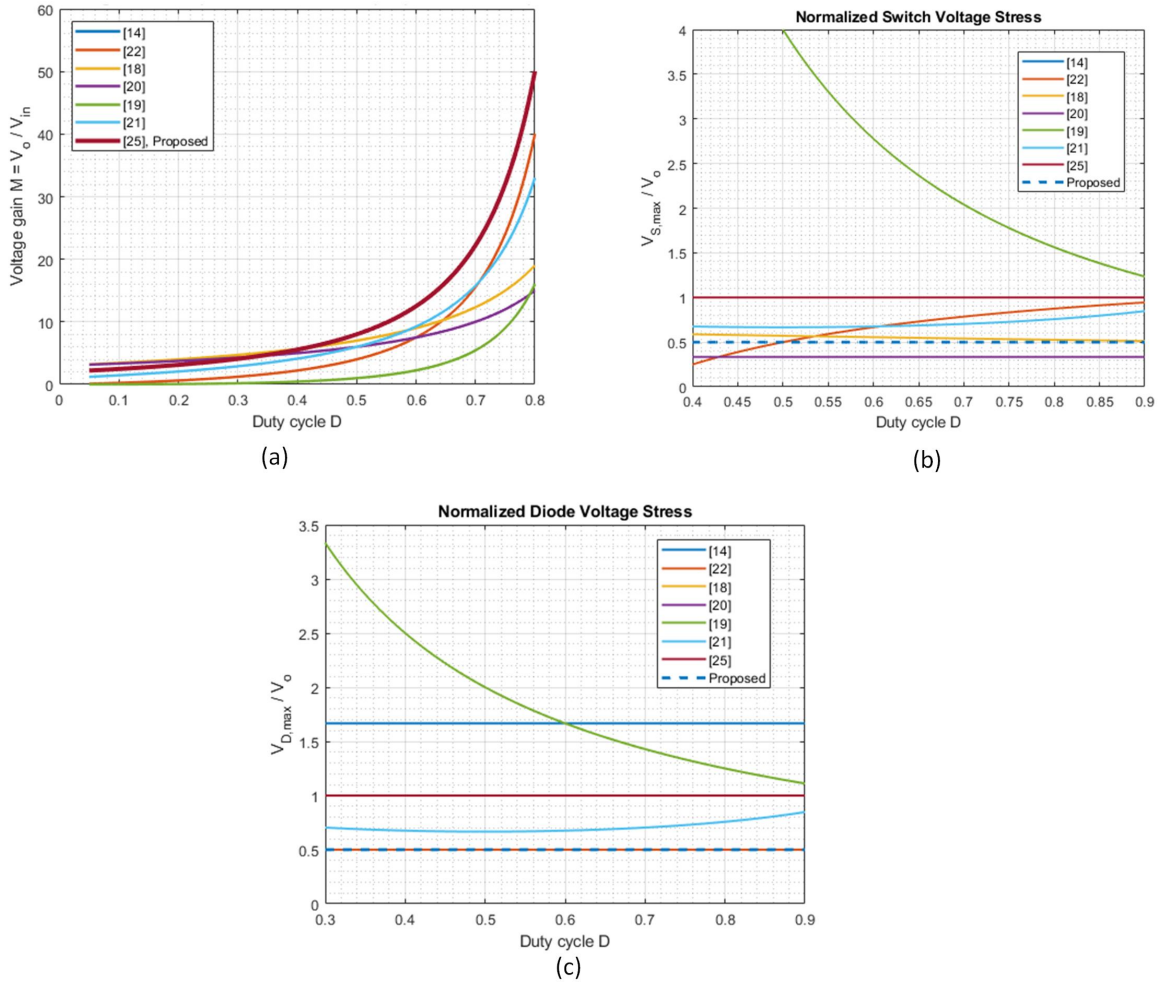

Figure 12. Comparison of the proposed converter with several existing topologies: (a) voltage gain versus duty cycle, (b) normalized switch voltage stress, and (c) normalized diode voltage stress.

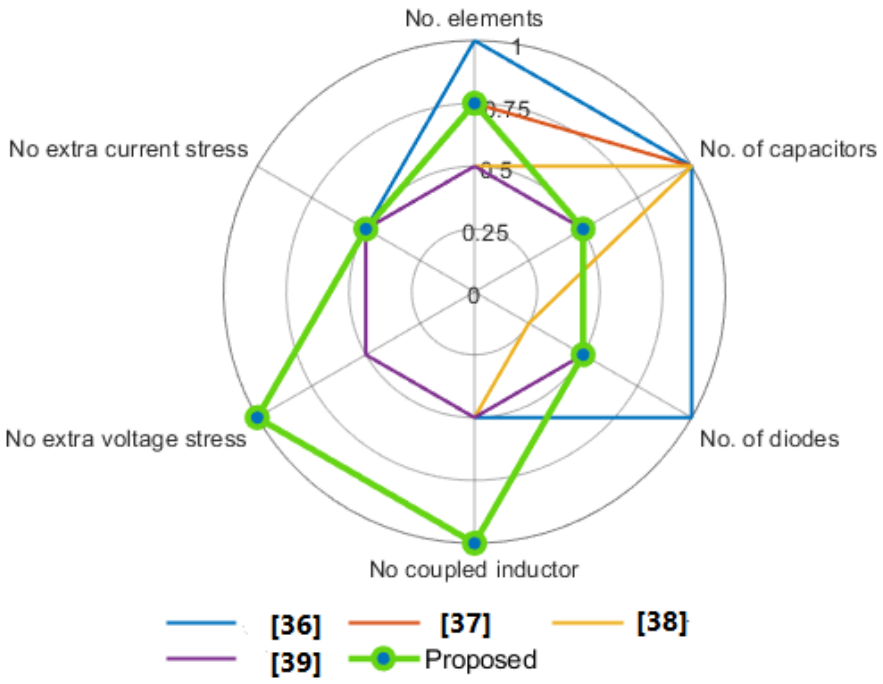

Figure 13. Radar chart comparison of the proposed converter with existing topologies in terms of circuit complexity and stress characteristics. The blue, red, orange, and purple traces correspond to converters reported in [36, 37, 38, 39], respectively, while the proposed converter is highlighted in green.

https://dx.doi.org/10.57647/mjee.2026.2001.08

in both increased voltage gain and lower voltage strain on the primary switch. The single switch achieving ZCS turn-on and ZVS turn-off operation, while the snubber circuit facilitates lossless energy recovery to the output. Moreover, the presence of leakage inductance ensures all diodes achieve ZCS turn-off, thereby mitigating reverse recovery losses. Owing to its single-switch structure, the converter maintains a simplified control strategy, and unlike many snubber-based topologies, it exhibits no voltage overshoot across the switch.

Authors contributions
All authors contributed equally to the conception, design, execution, and writing of this work. All authors read and approved the final manuscript.

Availability of data and materials
The authors declare that the data supporting the findings of this study are available within the paper.

Conflict of interests
The authors assert that they do not have any identifiable conflicting financial interests or personal relationships that might be perceived to influence the work presented in this paper.

References

1. Zaghmari MK, Delshad M, Abbasian M, and Yazdani MR. "**A new ZVS multi-input converter with modular auxiliary circuit and low voltage stress for renewable energy applications.**" Majlesi Journal of Electrical Engineering 2025. DOI: 10.57647/j.mjee.2025.17076
2. Bashirazami S, Amini MR, Adib E, and Delshad M. "**Two-switch step-down converter with low switch voltage stress**". Majlesi Journal of Electrical Engineering 2024; 18:1–8. DOI: 10.57647/j.mjee.2024.180345
3. Akhlaghi B and Farzanehfard H. "**Soft Switching Interleaved High Step-Up Converter With Multifunction Coupled Inductors**". IEEE J. Emerg. Sel. Topics Ind. Electron. 2021; 2:13–20. DOI: 10.1109/JESTIE.2020.3033542
4. Samadian A, Hosseini SH, and Sabahi M. "**A New Three-Winding Coupled Inductor Nonisolated Quasi-Z-Source High Step-Up DC–DC Converter.**" IEEE Trans. Power Electron. 2021; 36:11523–11531. DOI: 10.1109/TPEL.2021.3071847
5. Delshad M. "**A new zero-voltage-switching buck–boost-type DC–DC converter.**" Majlesi Journal of Electrical Engineering 2010; 4:25–318. DOI: 10.1234/mjee.v4i1.149
6. Faridpak B, Bayat M, Nasiri M, Samanbakhsh R, and Farrokhifar M. "**Improved Hybrid Switched Inductor/Switched Capacitor DC–DC Converters.** " IEEE Trans. Power Electron. 2021; 36:3053–3062. DOI: 10.1109/TPEL.2020.3014278
7. Luo P, Liang TJ, Chen KH, and Chen SM. "**Design and Implementation of a High Step-Up DC-DC Converter With Active Switched Inductor and Coupled Inductor.**" IEEE Trans. Ind. Appl. 2018; 59:3470–3480. DOI: 10.1109/TIA.2023.3238701
8. Li H and Chen D. "**A Novel High Step-Up Nonisolated Quasi-Z-Source DC–DC Converter With Active Switched Inductor and Switched Capacitor.**" IEEE J. Emerg. Sel. Topics Power Electron. 2023; 11:5062–5077. DOI: 10.1109/JESTPE.2023.3295408
9. Krishna B and Karthikeyan V. "**Active Switched-Inductor Network Step-Up DC–DC Converter With Wide Range of Voltage Gain at the Lower Range of Duty Cycles.**" IEEE J. Emerg. Sel. Topics Ind. Electron. 2021; 2:431–441. DOI: 10.1109/JESTIE.2021.3097943
10. Hasanpour S. "**New Structure of Single-Switch Ultra-High-Gain DC/DC Converter for Renewable Energy Applications.** " IEEE Trans. Power Electron. 2022; 37:12715–12728. DOI: 10.1109/TPEL.2022.3172311
11. Ding X, Zhou M, Cao Y, Li B, Sun Y, and Hu X. "**A High Step-Up Coupled-Inductor-Integrated DC–DC Multilevel Boost Converter with Continuous Input Current.**" IEEE Journal of Emerging and Selected Topics in Power Electronics 2022; 10:7346–7360. DOI: 10.1109/JESTPE.2022.3184699
12. Rezaie M and Abbasi V. "**Ultrahigh Step-Up DC–DC Converter Composed of Two Stages Boost Converter, Coupled Inductor, and Multiplier Cell.**" IEEE Trans. Ind. Electron. 2022; 69:5867–5878. DOI: 10.1109/TIE.2021.3091916
13. Rao BT and De D. "**A Coupled Inductor-Based High-Gain ZVS DC–DC Converter With Reduced Voltage Stresses.**" IEEE Trans. Power Electron. 2023; 38:15956–15967. DOI: 10.1109/TPEL.2023.3310577
14. Jin T, Lin J, Li H, Yan X, Weng Y, and Mao X. "**A Novel Three-Winding Coupled Inductor-Based High Step-Up DC-DC Converter for Renewable Energy Application.**" IEEE J. Emerg. Sel. Topics Power Electron. 2023; 11:4477–4490. DOI: 10.1109/JESTPE.2023.3260899
15. Niazi Y, Hosseini SH, and Maalandish M. "**A Switched-Capacitor Multi-Level Inverter With Variable Voltage Gain Based on Current-Fed Dickson Voltage Multiplier.**" IEEE Access 2023; 11:119352–119361. DOI: 10.1109/ACCESS.2023.3327309
16. Sarvghadi P, Varjani AY, and Shahparasti M. "**A High Step-Up Transformerless DC–DC Converter With New Voltage Multiplier Cell Topology and Coupled Inductor.**" IEEE Trans. Ind. Electron. 2022; 69:10162–10171. DOI: 10.1109/TIE.2021.3135625

17. Azizkandi ME, Hosseini SH, Maalandish M, and Babaei E. "**A High Voltage Gain DC–DC Converter Based on Three Winding Coupled Inductor and Voltage Multiplier Cell.**" IEEE Trans. Power Electron. 2020; 35:4558–4567. DOI: 10.1109/TPEL.2019.2944518
18. Mohammadi F, Hosseini SH, Maalandish M, and Babaei E. "**Non-Isolated Step-Up DC–DC Converter Based on Switched Capacitor Cells.**" CSEE J. Power Energy Syst. 2023; 9:1161–1172. DOI: 10.17775/CSEEJPES.2021.07370
19. Sadeghpour D and Bauman J. "**High-Efficiency Coupled-Inductor Switched-Capacitor Boost Converter With Improved Input Current Ripple.**" IEEE Trans. Ind. Electron. 2022; 69:7940–7951. DOI: 10.1109/TIE.2021.3109505
20. Subhani N, Bhaskar MS, Padmanaban S, and Blaabjerg F. "**An Improved Non-Isolated Quadratic DC–DC Boost Converter With Ultra High Gain Ability.**" IEEE Access 2023; 11:11350–11363. DOI: 10.1109/ACCESS.2023.3241863.
21. Li G, Tang Y, He Y, and He X. "**The Methodology of Constructing the Quadratic Converters.** " IEEE J. Emerg. Sel. Topics Power Electron. 2022; 10:6586–6606. DOI: 10.1109/JESTPE.2022.3157002
22. Hu R, Tang Y, and He X. "**An Ultrahigh Step-Up Quadratic Boost Converter Based on Coupled-Inductor.**" IEEE Trans. Power Electron. 2020; 35:13200–13209. DOI: 10.1109/TPEL.2020.2995911
23. Nouri T, Hosseini SH, Maalandish M, and Babaei E. "**An Interleaved ZVS High Step-Up Converter for Renewable Energy Systems Applications.**" IEEE Trans. Ind. Electron. 2022; 69:4786–4800. DOI: 10.1109/TIE.2021.3080211
24. Hasanpour S, Hosseini SH, Maalandish M, and Babaei E. "**High Step-Up SEPIC-Based Trans-Inverse DC–DC Converter with Quasi-Resonance Operation for Renewable Energy Applications.** " IEEE Trans. Ind. Electron. 2023; 70:485–497. DOI: 10.1109/TIE.2022.3150103
25. Yuan J, Tang Y, and He X. "**A Modified Y-Source DC–DC Converter With High Voltage-Gains and Low Switch Stresses.**" IEEE Trans. Power Electron. 2020; 35:7716–7720. DOI: 10.1109/TPEL.2020.2964153
26. Zhou M, Tang Y, and He X. "**High Step-Up Soft-Switching DC–DC Converter Integrated With Y-Source Network.**" IEEE J. Emerg. Sel. Topics Power Electron. 2023; 11:3348–3358. DOI: 10.1109/JESTPE.2023.3264984
27. Tarzamni H, Hosseini SH, Maalandish M, and Babaei E. "**Nonisolated High Step-Up DC–DC Converters: Comparative Review and Metrics Applicability.**" IEEE Trans. Power Electron. 2024; 39:582–625. DOI: 10.1109/TPEL.2023.3264172
28. Kalahasthi RB, Mishra SK, and Joshi A. "**A ZVS-Based Non-Isolated High Step-Up DC–DC Converter With Low Voltage Stress for Renewable Applications.**" IEEE J. Emerg. Sel. Topics Power Electron. 2023; 11:2793–2804. DOI: 10.1109/JESTPE.2023.3237076
29. Mohseni P, Hosseini SH, Maalandish M, and Babaei E. "**An Optimal Structure for High Step-Up Nonisolated DC–DC Converters With Soft-Switching Capability and Zero Input Current Ripple.**" IEEE Trans. Ind. Electron. 2022; 69:4676–4686. DOI: 10.1109/TIE.2021.3080202
30. Nouri T, Hosseini SH, Maalandish M, and Babaei E. "**A Novel Interleaved High Step-Up Converter With Built-In Transformer Voltage Multiplier Cell.** " IEEE Trans. Ind. Electron.
31. Alavi P, Hosseini SH, Maalandish M, and Babaei E. "**An Ultra-High Step-Up DC–DC Converter With Extendable Voltage Gain and Soft-Switching Capability.**" IEEE Trans. Ind. Electron. 2020; 67:9238–9250. DOI: 10.1109/TIE.2019.2952821
32. Farsijani M, Hosseini SH, Maalandish M, and Babaei E. "**A High Step-Up Cost Effective DC-to-DC Topology Based on Three-Winding Coupled-Inductor.**" IEEE J. Emerg. Sel. Topics Ind. Electron. 2023; 4:50–59. DOI: 10.1109/JESTIE.2022.3217017
33. Hasanpour S, Hosseini SH, Maalandish M, and Babaei E. "**A Novel Full Soft-Switching High-Gain DC/DC Converter Based on Three-Winding Coupled-Inductor.**" IEEE Trans. Power Electron. 2021; 36:12656–12669. DOI: 10.1109/TPEL.2021.3075724
34. Liang TJ, Luo P, and Chen KH. "**A High Step-Up DC–DC Converter With Three-Winding Coupled Inductor for Sustainable Energy Systems.**" IEEE Trans. Ind. Electron. 2022; 69:10249–10258. DOI: 10.1109/TIE.2021.3123683
35. Marzang V, Sabahi M, and Guerrero JM. "**A High Step-Up DC–DC Converter Based on ASL and VMC for Renewable Energy Applications.**" Energy Rep. 2022; 8:12699–12711. DOI: 10.1016/j.egyr.2022.09.080
36. Amini MR and Farzanehfard H. "**Novel family of PWM soft-single-switched DC–DC converters with coupled inductors.** " IEEE Trans. Ind. Electron. 2009; 56:2108–2114. DOI: 10.1109/TIE.2009.2016509
37. Esteki M, Mohammadi M, Yazdani MR, Adib E, and Farzanehfard H. "**Family of soft-switching pulse-width modulation converters using coupled passive snubber.**" IET Power Electron. 2017; 10:792–800. DOI: 10.1049/iet-pel.2016.0362

38. Mohammadi M, Adib E, and Yazdani MR. "**Family of soft-switching single-switch PWM converters with lossless passive snubber.**" IEEE Trans. Ind. Electron. 2015; 62:3473–3481. DOI: 10.1109/TIE.2014.2371436

39. Zhan T, Zhang Y, Nie J, Zhang Y, and Zhao Z. "**A novel soft-switching boost converter with magnetically coupled resonant snubber.**" IEEE Trans. Power Electron. 2014; 29:5680–5687. DOI: 10.1109/TPEL.2013.2295887