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Original Research

Direct-Written AgNP Electrodes in All-Solution-Processed Low-Voltage Organic Thin Film Transistors Employing High-k PVP Dielectric

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Abstract

Researchers have explored various fabrication methods for organic devices to meet the growing demand for printed electronics and wearables. Inkjet printing has been widely used for deposition of solution-processable materials at low temperatures, making it ideal for flexible electronics. However, nozzle clogging and strict ink and substrate requirements limit its commercialization for OTFTs. Besides, the practical applications of OTFT devices are limited by their high operating voltages. To address these limitations, this study proposes a simple, solution-based fabrication method for developing low-voltage OTFTs on Silicon substrates. A novel direct-write printing technique was utilized to deposit the source/drain electrodes at temperatures below 150 °C in ambient conditions without experiencing nozzle clogging issues, while a spin-coating method was

employed for the deposition of TIPS-pentacene semiconducting and high-k PVP dielectric layers. Remarkably, the fabricated OTFT achieved a channel length of 120 µm with saturation mobility of 4.49×10^{-1} cm^2/Vs, a threshold voltage of –1.5 V, an On/Off current ratio of 10^8, and a subthreshold swing of 66.8 mV/decade, operating below –5 V. The integration of direct-write printing with a high-k dielectric layer offers a new approach for fabricating OTFTs and other organic devices at lower temperatures, making it suitable for flexible electronics.

Keywords: Organic Thin Film Transistor; OTFT; Direct-write printing technique; TIPS-pentacene; PVP; PET; Low-voltage; Flexible; Semiconductor devices.

1. Introduction

Recently, organic electronics have gained significant attention from researchers, driven by the expansion of the printed electronics industry over the past few decades. Organic electronics represent a promising solution for the development of flexible, low-cost, and large-area electronic applications, including Organic Thin Film Transistors (OTFTs). The OTFT typically comprises three main functional layers, including the organic semiconductor (OSC), the dielectric, and the electrodes (i.e., source, drain, and gate terminals) deposited on either a rigid or flexible substrate. The selection of materials and their compatibility with fabrication processes and conditions determined the performance of the device, as highlighted by Yusof et al. in [1]. Therefore, careful consideration of material selection is essential during the device fabrication process.

In OTFT devices, the OSC layer plays an essential role as it serves as a channel for charge transport. Pentacene-based OTFTs have drawn substantial attention from researchers due to their high charge mobility [2], [3]. To promote effective charge injection and transport within the device, it is essential that the contacts are compatible with the OSC layer. Theoretically, an Ohmic contact is ideal for the proper operation of OTFTs. Nonetheless, a mismatch between the energy level of the semiconductor and the work function of the electrodes is inevitable, resulting in contact resistance at the metal/semiconductor interface, which is unfavorable for charge transport [4]. Thus, an appropriate electrode material selection is pivotal to optimize the overall OTFT performance.

Continuous efforts have been made to improve the performance of OTFT devices. However, the high operating voltages reaching up to –60 V, particularly in Silicon Dioxide (SiO_2) based OTFTs, remain a primary concern among researchers. The application of high voltages can exert stress on materials, particularly in flexible substrates, potentially leading to degradation and reducing the lifespan of the device. A low operating voltage in OTFT can be achieved by increasing the gate capacitance. The gate capacitance refers to the capacitance with the gate terminal of the OTFT and can be expressed as Equation 1 [5].

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d} \quad (1)$$

Where C is the gate capacitance, ε_0 is the vacuum permittivity (8.86 $\times$ 10^{-12} C^2 N^{-1} m^{-2}), ε_r is dielectric permittivity (also known as dielectric constant, k), A is the plate overlap area, and d is the distance between the two plates (also referred to as the dielectric thickness). From Equation 1, the gate capacitance C can be increased using materials with a high dielectric constant or reducing the dielectric thickness d [6], [7]. Scaling down the dielectric thickness is not a feasible approach, as it increases leakage currents. Therefore, employing dielectric with a high dielectric constant is a more viable strategy for enhancing the device's gate capacitance in order to reduce its operating voltage.

OTFTs can be developed using various fabrication techniques, contact methods (e.g. screen printing and lithography) or non-contact methods (e.g. inkjet printing). Among these, non-contact inkjet printing has emerged as the most promising technology due to its benefits, including the elimination of the need for a vacuum environment during fabrication, minimized material waste through drop-on-demand technology, and its scalability for large-area manufacturing, as mentioned in [8], [9]. Moreover, its contactless and direct patterning of functional layers prevents morphological damage to the other layers, which is commonly induced by developing and etching processes [10].

Despite its advantages, inkjet printing technology presents several challenges that impede the commercialization of OTFTs, including persistent nozzle clogging issues and stringent requirements for conductive inks (i.e. low viscosity typically between 1 – 25 mPa.s) and substrate properties (i.e. low surface tension between 20 – 50 $mN.m^{-1}$)[9], [11]. To address these challenges, a novel fabrication technique employing a direct ink writing (DIW) method has been proposed to develop OTFTs [12]. Unlike inkjet printing, this method allows the deposition of a wide range of materials, which are not limited to the low-viscosity materials as required in inkjet printing technology. This technique enables layer-by-layer patterning directly from computer-aided design (CAD) files and presents a novel bottom-up manufacturing approach for fabricating electronic devices.

In this work, we successfully reported all-solution-processed low-voltage OTFTs utilizing Silver Nanoparticle (AgNP) conductive ink, Polyvinylpyrrolidone (PVP), and 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) as the source/drain electrodes, gate dielectric, and OSC layers, respectively, on a Silicon wafer. Notably, the electrodes were deposited using the proposed DIW printing technique with a channel length of 120 µm. The employment of a high-k dielectric material allows the device to operate at a lower operating voltage of less than –5 V.

The rest of this paper is organized as follows: Section 2 outlines the materials utilized and the experimental details involved in the fabrication of the proposed device. This section also

presents the electrical and morphological characterizations of the fabricated OTFTs. Subsequently, Section 3 analyzes the performance of the devices. These results have been discussed comprehensively and compared with relevant prior work. Finally, Section 4 concludes the paper.

2. Materials and experimental details

2.1 Materials

In this study, commercially available Silver Nanoparticle (AgNP) conductive ink from Voltera Inc. was utilized to deposit the conductive electrodes, i.e. source and drain, while 99+ % hydrolyzed Polyvinylpyrrolidone (PVP) (molecular weight = 40,000) purchased from Sigma-Aldrich was employed as the dielectric layer. For the organic semiconducting (OSC) layer, high purity (>99.9 %) 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) and its solvent, 99.5 % AR-grade Toluene, were obtained from Ossila Ltd. and Chemiz (M) Sdn. Bhd., respectively. All materials were used as received without further purification. A single-side polished <100> Silicon substrate, with a thickness of 625 ± 25 µm and a resistivity of 1 to 3 mΩ.cm, obtained from Fuleda Technology, was utilized as the substrate for OTFT fabrication.

2.2 Experimental details

This work is organized into two primary sections: device fabrication using the proposed DIW technique, followed by the electrical and morphological characterization of the fabricated device. Both fabrication and measurements were performed in ambient air at room temperature. Notably, all materials used in this study were solution-processable and applied to the fabrication of Bottom-Gate Bottom-Contact (BGBC) OTFTs.

2.2.1 Fabrication of all-solution-processed low-voltage OTFT

Initially, the Silicon (Si) substrate was cut into a 20 mm × 15 mm piece and cleaned using a standard solvent cleaning procedure. The process involved sequential ultrasonic cleaning in Acetone, Isopropyl Alcohol (IPA), and Deionized (D/I) water for three minutes each. The cleaned substrate was subsequently dried using a dryer before being exposed to ultraviolet (UV) light in the UV/ozone cleaner to remove any residual organic contaminations on its surface. Afterwards, 100 µl of high-k PVP dielectric solution was spin-coated on the cleaned substrate and subjected to heat treatment at 80 °C to 100 °C for one hour.

This research utilized a direct-write printing technique for the deposition of source and drain electrodes in OTFT devices. The printer parameters were optimized as described in [12], [13]. To fabricate a bottom-contact device, the source and drain electrodes were DIW printed onto the PVA dielectric layer and subsequently cured at temperatures between 100 °C to 150 °C for one hour. Following this, to complete the OTFT structure, 60 µl of OSC solution was spin-coated onto the source and drain electrodes and annealed at temperatures ranging from 80 °C to 100 °C for 10 minutes to remove any residual solvent. In this work, the OSC solution was prepared by dissolving TIPS-pentacene in Toluene. Finally, any excess OSC material on the surface of the sample was removed using a cotton swab wetted with Toluene. Fig. 1 illustrates the layout of the fabricated device using PVP dielectric on the Si substrate.

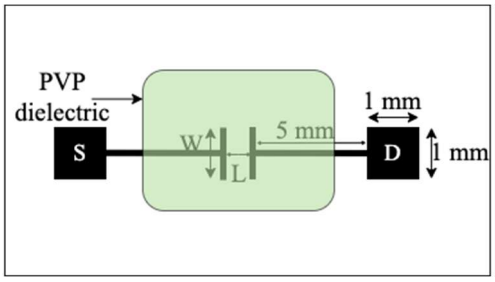

Figure 1. Layout of the proposed OTFT device using PVP dielectric on the Si

2.2.1 Characterization of the fabricated OTFT devices

The fabricated OTFT devices were characterized and analyzed using a Keithley 4200A SCS semiconductor parameter analyzer (SPA) and a quick test system consisting of a custom probe station and optical microscope. The output characteristics were measured by sweeping V_D from 0 to – 5 V, across a range of V_G from 0 to –5 V. From the output and its corresponding square-root I_D curves, the saturation mobility (μ_{sat}), threshold voltage (V_{th}), and On/Off current ratio (I_{ON}/I_{OFF}) were extracted. Furthermore, the subthreshold swing (S) can be calculated from the inverse of the subthreshold slope of the square-root I_D curve. The morphological characteristics of the deposited TIPS-pentacene film on the PVP/Si substrate were analyzed using scanning electron microscopy

(SEM) and atomic force microscopy (AFM), while the surface energy of the PVP dielectric was characterized through contact angle measurements.

3. Results and discussion

3.1 Morphological characterization of the proposed OTFT

Fig. 2(a) presents a schematic diagram of the proposed OTFT device, illustrating the materials used in each layer, while Fig. 2(b) displays the camera photograph of the DIW-printed OTFT device. The OTFT was fabricated on a Si substrate, utilizing AgNP conductive ink for the source and drain electrodes, TIPS-pentacene solution for the OSC layer, and PVP solution for the dielectric layer. This work selected TIPS-pentacene as the OSC layer due to several key advantages that align well with the objectives of OTFT development. One of the primary reasons is its inherently high charge carrier mobility, which is essential for efficient charge transport within the transistor channel, thereby enhancing the overall device performance. TIPS-pentacene also demonstrates excellent crystallinity, a crucial factor that directly influences the mobility of charge carriers by reducing grain boundary scattering and facilitating smoother charge flow.

Another significant reason for selecting TIPS-pentacene is its compatibility with solution-based deposition techniques, such as spin coating, inkjet printing, and drop casting. This compatibility is particularly valuable for scalable and cost-effective fabrication processes, as solution processing enables large-area device fabrication and roll-to-roll manufacturing, making it a promising material for commercial applications. Furthermore, TIPS-pentacene exhibits good chemical and structural compatibility with various organic materials commonly used in OTFT fabrication, such as dielectric layers, gate materials, and encapsulation layers. This favorable interaction facilitates the integration of multiple functional layers within the OTFT structure, allowing the development of complex configurations like top-gate and bottom-gate architectures, dual-gate designs, and flexible electronics. The ability to form stable and well-defined interfaces with other organic layers further contributes to the overall stability, reproducibility, and performance of the fabricated OTFTs.

Additionally, the solubility of TIPS-pentacene in common organic solvents provides further flexibility in device processing, enabling fine-tuning of the film morphology, thickness, and uniformity through process parameter adjustments. This adaptability is essential in optimizing the device characteristics to meet specific application requirements, such as in display technologies, sensors, and wearable electronics. Overall, the selection of TIPS-pentacene is justified by its superior electrical properties, processability, and compatibility with OTFT fabrication requirements, making it a highly suitable choice for achieving high-performance organic transistors in this work.

PVP was selected as the dielectric layer in this work due to several critical attributes that align with the performance and fabrication requirements of Organic Thin-Film Transistors (OTFTs). One of the primary reasons is its high dielectric constant (high-k), which is essential for efficiently storing and modulating charges within the transistor. A high-k dielectric allows for greater charge

accumulation at the semiconductor-dielectric interface under lower operating voltages, thereby enhancing the overall performance of the OTFT, particularly in low-power applications. In addition to its dielectric properties, PVP is highly compatible with solution-based fabrication techniques such as spin coating, dip coating, and inkjet printing. This compatibility facilitates cost-effective and scalable manufacturing processes, making it suitable for large-area electronic device fabrication. The ability to process PVP from solution also allows for fine control over film thickness and uniformity, which are crucial parameters for achieving consistent and reproducible device performance.

Most importantly, PVP exhibits notable mechanical flexibility, a critical requirement for the development of flexible and wearable electronic devices. Its inherent flexibility enables the fabrication of OTFTs on bendable substrates such as plastic films, allowing devices to withstand mechanical deformation without compromising electrical performance. This property is particularly advantageous in applications like flexible displays, wearable sensors, and foldable electronics, where mechanical durability is as important as electrical functionality.

Furthermore, PVP offers good thermal and environmental stability, which contributes to the long-term reliability of OTFTs, especially in applications subjected to varying environmental conditions. Its ability to form smooth, uniform thin films with low surface roughness also ensures minimal charge trapping at the dielectric-semiconductor interface, thereby enhancing charge carrier mobility and reducing hysteresis in the transistor operation. Overall, the selection of PVP as the dielectric material is justified by its high-k properties for efficient charge modulation, solution processability for scalable fabrication, and excellent mechanical flexibility essential for the next generation of flexible and wearable electronic devices.

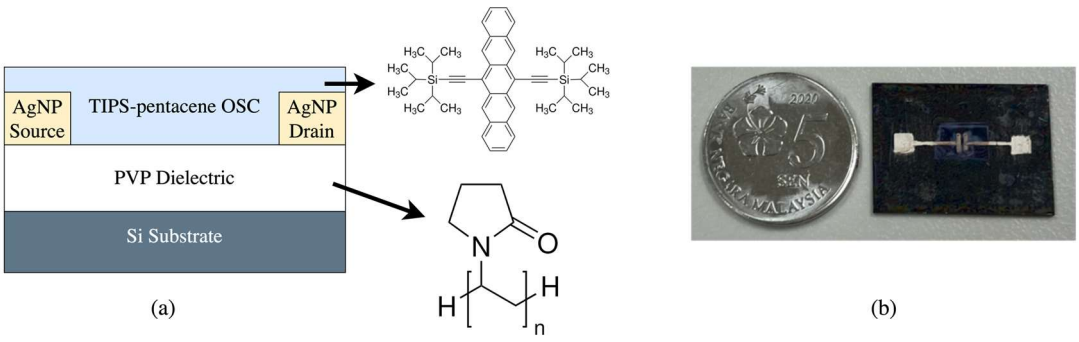

Figure 2. (a) Schematic diagram of the device structure and its corresponding chemical structure for OSC and dielectric layers and (b) Camera photograph of the DIW-printed OTFT device on Si

Previously, the DIW printing method has been investigated for the development of various sensors and electronic circuits, as reported by Hou et. al. in [14]. Despite its potential applications in printed electronics, the DIW printing technique has not yet been extensively explored for OTFT fabrication. This work successfully employed the DIW printing method to deposit the source and drain contacts in OTFT devices with channel lengths of 120 μm.

The proposed DIW printing technology offers advantages over conventional inkjet printing, particularly in terms of material selection due to its compatibility with a wide range of inks. The AgNP conductive ink used in this work exhibits a high viscosity of 2000 mPa.s. No clogging issues were encountered during the deposition process and the printed electrodes were deposited smoothly onto the substrate, as seen in Fig. 2(b). The compatibility of the DIW printer with high-viscosity inks exceeds that of inkjet printing technology, which typically accommodates inks with viscosities of up to 25 mPa.s [11]. This capability not only enables the utilization of a broader range of materials but also simplifies the ink formulation process, which is often limited by viscosity to prevent nozzle clogging issues. AgNP conductive ink was used in this work due to its narrow energy barrier with TIPS-pentacene, characterized by an energy gap of less than 0.4 eV, which facilitates efficient hole injection between the electrodes and the OSC layer [15]. Additionally, AgNP ink requires a curing temperature of less than 150 °C, making it well-suited for flexible electronics applications.

Maintaining consistent line width during DIW printing is essential to ensure uniformity in printed patterns, which significantly influences the electrical performance and reliability of OTFTs. Variations in line width can result in inconsistencies in channel dimensions, thereby affecting charge transport and overall device performance. A key challenge in achieving uniform line width is the precise control of ink flow rate, which is governed by parameters such as kick and rheological setpoint. In DIW printing, kick refers to the initial pressure pulse applied to initiate ink flow through the nozzle at the onset of the printing process. Optimizing the kick is crucial to prevent delays in ink extrusion or excessive deposition, both of which can result in line width variations. Similarly, the rheological setpoint defines the ink's flow characteristics, including viscosity and shear-thinning behavior, ensuring an optimal balance between fluidity during extrusion and structural integrity post-deposition. Precise control of both parameters is essential for maintaining consistent line widths, thereby ensuring the uniformity and reliability of printed OTFTs.

Next, the morphological characteristics of the deposited OSC layer of the fabricated device were analyzed to evaluate the quality of the film, assess its surface roughness, identify any defects or irregularities, and elucidate their relationships to the electrical performance of the device. Fig. 3 presents the morphological characteristics of the fabricated TIPS-pentacene OTFT based on the PVP dielectric layer on the Si substrate. The spin-coated TIPS-pentacene film demonstrated a relatively smooth surface, characterized by surface roughness (RMS) of 1.472 nm (Fig. 3(b)) and a thickness of 67.7 nm (Fig. 3(a)).

Surface roughness directly affects the interface quality between the OSC and the dielectric layer, which in turn influences charge carrier mobility, threshold voltage, and overall device stability. A smoother OSC surface reduces the number of trap sites and defects at the interface, thereby minimizing charge scattering and recombination. This leads to higher charge carrier mobility, as the carriers can move more freely through the well-ordered crystalline domains of the TIPS-pentacene film without encountering barriers or interruptions caused by surface irregularities.

In contrast, a higher surface roughness would introduce more grain boundaries, voids, and defects, increasing the probability of charge trapping and reducing the effective mobility of carriers within the channel. Furthermore, surface irregularities can result in non-uniform electric fields at the semiconductor-dielectric interface, causing instability in the transistor's threshold voltage and increasing hysteresis during device operation.

The relatively smooth surface observed in this work is attributed to the hydrophobic properties of the PVP dielectric layer, with a contact angle of 79.6° as shown in Fig. 3(c). The hydrophobic nature of PVP promotes better molecular ordering of the TIPS-pentacene during the spin coating process, leading to a more uniform and defect-free film. This enhanced film morphology contributes significantly to the stable and high-performance electrical characteristics of the fabricated OTFTs, such as high charge carrier mobility, low threshold voltage, and reduced hysteresis. In summary, the surface roughness of the TIPS-pentacene film is a crucial morphological parameter that correlates directly with the electrical performance of the OTFT. The smooth surface achieved in this study ensures reduced charge trapping, improved charge transport, and stable transistor operation, highlighting the importance of optimizing surface morphology during the fabrication process.

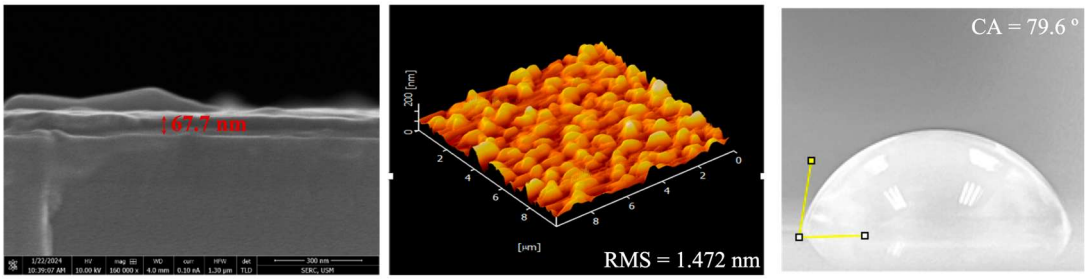

Figure 3. Morphological characterization of the fabricated device: (a) SEM cross-sectional image and (b) AFM surface profile of the TIPS-pentacene layer, and (c) water contact angle of PVP dielectric layer.

3.2 Electrical characterization of the proposed OTFT

In this section, the electrical characteristics of the proposed OTFT devices were evaluated. Fig. 4(a) shows the output characteristics (I_D – V_D), while Fig. 4(b) and Fig. 4(c) depict the transfer characteristics ($|I_D|$ – V_G) of the device and the corresponding square-root I_D ($\sqrt{I_D}$ – V_G) curve, respectively. V_D was swept from 0 to –5 V with a step size of –1 V, while V_G was varied from 0 to –5 V. These findings represent the average values obtained from testing across ten devices. Negative voltages were applied because holes serve as the majority charge carriers in TIP-pentacene. From Fig. 4, the proposed TIPS-pentacene OTFT device demonstrates a typical p-type field effect transistor behaviour, with distinct linear and saturation regions observable in the output curves, as shown in Fig. 4(a).

From the transfer curve and the corresponding square-root I_D curve displayed in Fig. 4(b) and Fig. 4(c), saturation mobility (μ_{sat}) of 4.49 × 10^{-1} cm^2/Vs, a threshold voltage (V_{th}) of –1.5 V, and On/Off current ratio (I_{ON}/I_{OFF}) of up to 10^8 (at V_G = –5 V and V_D = –2.5 V) were determined. Additionally, the device achieved the subthreshold swing (S) of 66.8 mV/decade. The field effect mobility of the OTFT in the saturation region was calculated using Equation 2, as described in [16]. On the other hand, the subthreshold swing was determined from the inverse of the subthreshold slope of the square-root I_D curve and can be expressed as Equation 3, as outlined in [17]. Apart from that, the subthreshold swing can also be represented by Equation 4, which can be employed to calculate the lowest theoretical S at room temperature.

$$\mu_{sat} = \frac{L}{W}\frac{1}{C_i}\frac{\delta^2 I_D}{\delta V_G{}^2} \tag{2}$$

Where μ_{sat} is the saturation mobility, C_i is the capacitance of the dielectric, while L and W are the channel length and width, respectively.

$$S = \frac{dV_G}{d(\log I_D)} \tag{3}$$

$$S = \frac{K_B T}{q}\ln 10 \tag{4}$$

Where K_B is Boltzmann's constant, T is temperature in Kelvin, and q is the elementary charge. At a room temperature of 300 K, the value of S was determined to be 57 mV/decade.

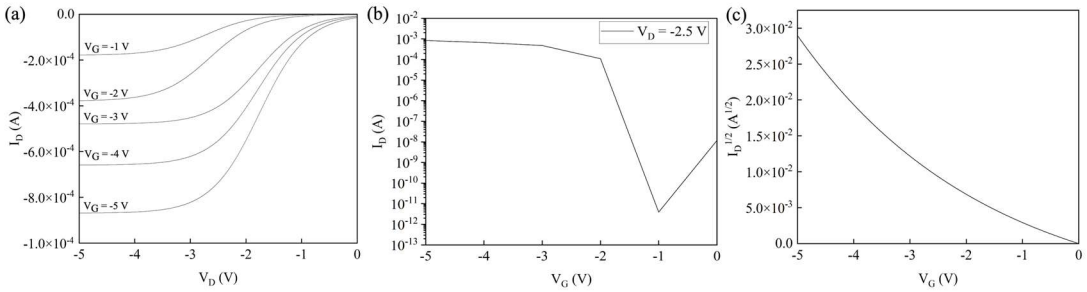

Figure 4. Electrical characterization of the fabricated device: (a) Output (I_D – V_D), (b) Transfer (I_D – V_G), and (c) Square-root I_D ($\sqrt{I_D}$ – V_G) curves.

In general, the electrical performance of OTFT devices is closely linked to their morphological characteristics [18]. The quality of OSC film typically influences the mobility of the device, while the quality of its interface significantly affects the overall performance of the OTFT, including parameters such as I_{ON}/I_{OFF} and S [19], [20]. The smooth and good adhesion between the deposited TIPS-pentacene and dielectric layers, characterized by low surface roughness

(RMS) and subthreshold swing S nearly reaching the theoretical limit at room temperature, improved the overall device performance, exceeding the values reported by other researchers, as indicated in Table 1. Minimal surface defects and interface traps between OSC and dielectric layers facilitate an enhancement of the I_{ON}/I_{OFF} current ratio by diminishing the leakage currents within the device. As a result, the proposed OTFT significantly enhances its I_{ON}/I_{OFF} performance, with an improvement of up to eight orders. A subthreshold slope close to the theoretical limit (~60 mV/decade at room temperature) is significant as it indicates efficient gate control over the channel, enabling rapid switching between the off and on states with minimal voltage change. This leads to lower power consumption, reduced leakage current, and faster switching speeds, which are critical for energy-efficient, high-performance OTFTs, particularly in flexible and wearable electronics. Achieving a near-ideal subthreshold slope also reflects high interface quality with minimal trap states, enhancing device reliability and scalability, and is often a result of optimized material selection, surface treatment, and fabrication processes.

Apart from that, the fabricated OTFT device displayed improvement in mobility of up to five orders of magnitude as compared to the previously proposed device [12]. The low surface energy of the high-k dielectric layer, characterized by a contact angle of nearly 90°, promotes the growth of the OSC layer by providing a stable foundation for the deposition of the TIPS-pentacene film. This condition enables the formation of a uniform and smooth OSC layer, thereby enhancing its electrical performance, particularly in terms of mobility.

Conventionally, OTFTs have been developed using oxide-based dielectric materials, such as SiO_2. Although SiO_2 is widely recognized for its excellent insulating properties and compatibility with Si substrates, OTFTs fabricated using this dielectric material often face challenges related to high operational voltages, typically more than – 60 V [12], [21], [22]. The high operating voltages in SiO_2-based OTFTs can be attributed to the intrinsic properties of SiO_2, including its low capacitance per unit area. While reducing the thickness of SiO_2 can enhance its capacitance density, this approach may lead to higher leakage current in the devices, thereby complicating their operation [23].

To cater for this problem, high-k dielectric materials were employed in OTFT development. In this work, PVP has been utilized as the dielectric layer, thanks to its compatibility with solution processable methods and OSC material, as well as its high dielectric constant (k = 7.7). The operating voltage of the proposed device demonstrated remarkable improvement, enabling operation at voltages below –5 V. The incorporation of high-k dielectrics increases the gate capacitance of OTFTs, facilitating greater charge storage per unit area within the gate dielectric [24]. This improvement enables enhanced electrostatic modulation of the semiconductor channel. Consequently, lower gate voltages are needed to achieve the desired changes in channel conductivity, resulting in lower operational voltages in OTFT devices. Low operating voltages are crucial in flexible electronics since flexible substrates are susceptible to damage and degradation

when subjected to high voltages, potentially compromising both the overall performance and lifespan of the devices.

Overall, the performance of the fabricated OTFTs surpassed that of devices manufactured using inkjet printing techniques [25],[26], as presented in Table 1. Based on Table 1, the proposed OTFT device not only exhibited a low operating voltage and low V_{th} but also demonstrated an enhancement of up to eight orders of magnitude in the I_{ON}/I_{OFF} current ratio. This device also displayed the highest μ_{sat}, exceeding that of devices fabricated using thermal evaporation [27]. In summary, the results presented in Table 1 confirm that the proposed DIW printing technique can be effectively utilized to develop OTFT devices without compromising their electrical and morphological performances. Besides, the utilization of high-k dielectric successfully reduced the operating voltage of the proposed device. Notably, this technique allows the deposition of the source and drain electrodes with micrometre channel lengths without encountering clogging issues. The integration of DIW printing technology into the high-k dielectrics offers a novel bottom-up approach for fabricating organic devices, particularly OTFTs, at lower processing temperatures suitable for flexible and wearable electronics niches.

Table 1. Comparison of the proposed all-solution-processed low-voltage OTFT performance with other state-of-the-art works.

Reference	**[3]**	**[25]**	**[26]**	**[27]**	**[12]**	**This work**
S/D Deposition	Lithography	Inkjet-printed	Inkjet-printed	Thermal evaporation	DIW-printed	**DIW-printed**
OSC Layer	TIPS-pentacene	TIPS-pentacene	TIPS-pentacene	TIPS-pentacene	TIPS-pentacene	**TIPS-pentacene**
Dielectric Layer	SiO_2	PVP	PVP	PVA	SiO_2	**PVP**
Saturation Mobility µsat (cm^2/Vs)	3.9×10^{-3}	5.8×10^{-3}	3.0×10^{-2}	3.4×10^{-2}	4.3×10^{-5}	**4.5×10^{-1}**
Operating Voltage (V)	0 to -20	0 to -12	0 to -3	0 to -30	0 to -60	**0 to -5**
Threshold Voltage V_{th} (V)	-4.7	-5.8	-0.7	-13.8	-0.4	**-1.5**
On/Off Current Ratio I_{ON}/I_{OFF}	-	10^5	10^2	10^3	10^2	**10^8**
Subthreshold Swing S (mV/decade)	-	-	-	4200	100	**66.8**

4. Conclusion

The DIW printing technique is an innovative approach with the ability to rapidly pattern functional materials over a wide range of substrates without nozzle clogging issues. This advancement has broadened its applications in flexible electronics, including OTFT fabrication. In this work, we successfully developed an all-solution-processed low-voltage OTFT device with a channel length of 120 µm, employing the DIW deposition technique. The utilization of high-k PVP dielectric enabled the fabrication of a low-voltage OTFT working at an operating voltage of less than –5 V. Noticeably, the proposed BGBC TIPS-pentacene OTFT device exhibited μ_{sat} of 4.49×10^{-1} cm^2/Vs, V_{th} of –1.5 V, I_{ON}/I_{OFF} of up to 10^8 (at V_G = –5 V and V_D = –2.5 V), and S of 66.8 mV/decade. Interestingly, the overall processing temperature was kept below 150 ℃ to ensure compatibility with flexible electronics requirements. A comprehensive scalability study focusing on channel length variations could provide critical insights into optimizing processing conditions, improving device uniformity, and reducing material costs, making DIW printing a viable option for large-scale OTFT production. Optimizing channel lengths is particularly important as it directly affects charge carrier mobility, threshold voltage, and switching speed, and successful scalability could enable cost-effective OTFT deployment in flexible electronics, displays, sensors, and wearable devices, expanding their accessibility and applications.

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Author contributions
All authors have contributed equally in preparing and writing the manuscript.

Availability of data and materials
The data that support the findings of this study are available from the corresponding authors upon reasonable request.

Conflict of interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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