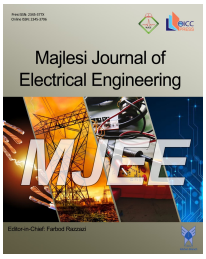

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Original Research

A New ZVS Multi-input Converter with Modular Auxiliary Circuit and Low Voltage Stress for Renewable Energy Applications

Mehdi Khodadadian Zaghmari, Majid Delshad*, Mohammadali Abbasian, Mohammad Rouhollah Yazdani

Department of Electrical Engineering, Isf.C, Islamic Azad University, Isfahan, Iran

***Corresponding author:** majid.delshad@iau.ac.ir

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Abstract:

Renewable energy sources like wind and solar power experience output voltage fluctuations due to changing weather conditions. To maintain a stable power supply, integrating multiple input sources is essential. A Multi-Input Converter (MIC) provides a more efficient solution by reducing the need for numerous passive components, which in turn minimizes cost, size, and weight compared to separate converters. This study introduces a dual-input boost converter with zero voltage switching (ZVS), utilizing a single auxiliary circuit to enable soft switching for all semiconductor elements. This design not only improves efficiency but also retains the advantages of multi-input converters. Additionally, a voltage multiplier is incorporated to enhance the voltage conversion ratio, achieving higher voltage gains. The theoretical analysis of the proposed converter is validated through experimental results, with efficiency measurements demonstrating a 3% improvement over conventional hard-switching designs.

Keywords: DC-DC converter; Coupled inductor; High-gain; Soft-switching

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1. Introduction

In boost converters, the rapid switching of power devices leads to considerable switching losses. To achieve high voltage gain, various topologies and techniques have been developed in traditional boost converter designs [1, 2, 3]. These converters offer multiple benefits, including enhanced transient response, improved thermal management, reduced current ripple, and increased reliability [4, 5]. In multi-phase buck converters, increasing the number of switching stages within a single phase effectively raises the input current's frequency, thereby reducing overall current ripple [5, 6]. Additionally, multi-phase converters improve efficiency by distributing the load current across several phases, which minimizes voltage drops and conduction losses in semiconductor devices. Higher switching frequencies can further enhance the transient response and power density of DC-DC converters. However, operating at higher switching frequencies can also result in reduced overall efficiency and increased switching losses [7, 8].

One of the main challenges in high-frequency converters is electromagnetic interference (EMI). both passive [7, 8] and active [9, 10] switching techniques have been proposed. Among active methods, Zero Voltage Transition (ZVT) is widely regarded as a simple yet effective solution, especially in converters utilizing MOSFETs. ZVT achieves reduced switching losses and lower EMI by enabling or disabling the MOSFET at zero voltage [11, 12, 13]. Furthermore, optimizing ZVT-based converters by minimizing the number of components in the ZVT cell and employing a single ZVT cell across multi-stage

converter structures can significantly reduce both the overall cost and physical size of the converter. Recent studies have explored a range of converter topologies, including those employing boost configuration with particular emphasis on ZVT implementations. Despite their advantages, many of the proposed topologies suffer from certain drawbacks, such as increased component count, added complexity, and reduced efficiency under specific operating conditions.

The high complexity and large number of components significantly increase both the overall cost and physical size of the circuit.

The need for diode replacement along with the associated costs and electromagnetic interference (EMI) issues-can be mitigated through timely maintenance or the use of alternative solutions.

The inclusion of one or more switches in the gate driver control circuit further contributes to system complexity.

In [14], a Zero Voltage Transition (ZVT) soft-switching boost converter is introduced, incorporating an auxiliary circuit with two auxiliary switches configured within a two-phase amplifier. However, this design results in increased voltage stress on the main switch. In contrast, [15] proposes a soft-switching poly-phase boost converter that integrates a resonant choke into its ZVT implementation, but it requires DC auxiliary switches and floating gate control for each phase, adding to design complexity. Recent works [16] have proposed various methods to reduce the number of active components in converter circuits. For instance, the converters presented in [17] achieve smooth operation of the main switch by using an auxiliary switch; however, these configurations still rely on additional semiconductor elements. Notably, [17] requires the auxiliary switch to operate four times per switching cycle, thereby doubling the number of switching states. This extended operation increases conduction time and leads to higher power dissipation [18]. Alternatively, [19] investigates a boost converter design that mitigates additional current and voltage stress on the main switch. Nevertheless, its two-phase structure requires additional components, including two inductors and four diodes. In [20], a ZVT boost converter is reviewed that employs an auxiliary switch and features a relatively simple switching mechanism. Despite this simplicity, it necessitates a high-voltage current converter to maintain load supply during the extended activation of the auxiliary circuit, resulting in increased conduction losses. Efforts in [21] aim to simplify the converter topology by minimizing component count. However, the converter described in [21] is limited by switching frequency constraints, inadequate filtering performance, and elevated stress on the converter switch. Similarly, the inverter presented in [22] demands a secondary switch for sliding gate control and requires a dedicated magnetic core for the secondary winding. In the ZVT design proposed in [23], synchronous rectifier switches are repurposed as auxiliary switches, eliminating the need for additional switching elements. While effective, this method is only applicable to transformer-based systems that already include synchronous rectifiers. It also significantly reduces voltage and current stresses on switch. A simpler ZVT converter design is presented in [24], featuring a streamlined circuit structure; however, it still employs multiple auxiliary components and imposes both current and voltage stress on the auxiliary switch. Reference [25] highlights the inclusion of multiple auxiliary elements in a two-phase transformer design. A buck converter with comparable characteristics is also noted in [25], which, although more compact, encounters similar limitations as those reported in [26]. This paper presents a comprehensive review of a family of interconnected ZVT converters and their various configurations. The proposed design utilizes a single auxiliary circuit, enabling all semiconductor devices to operate in a simple switching mode with only one switch and without the need for chokes, thereby improving efficiency during load variations. In this configuration, the converters employ Zero-Voltage Switching (ZVS) for the main switches and Zero-Current Switching (ZCS) for the auxiliary switches. Moreover, the leakage inductance of the coupled windings can control the output current, reduce stress on complementary diodes, and reduce issues related to reverse recovery. The converter uses transformer cores with couple windings that function as voltage sources, effectively reducing the current in the secondary circuit to zero once the ZVS switch is activated. The integrated ZVT cell absorbs the leakage inductance of the coupled coils and utilizes the parasitic MOSFET capacitors as suppression capacitors. This integration eliminates the need for additional resonance inductance, significantly lowering the cost, weight, and size of the auxiliary circuit. The proposed ZVT converters were theoretically validated through a step-up design process, and a 300 W boost converter prototype operating at 100 kHz was built to confirm the experimental results. Furthermore, additional variants of the converter family have been developed based on the ZVT concept, with new versions. While a basic ZVT cell was introduced in [27], its application was initially confined to single-phase converters and did not extend to other two-input DC-DC converter types. In this study, the cell is employed to develop a full series of low-cost, compact, and soft ZVT AC converters, all sharing a common sub-circuit.

2. The proposed ZVT dual-input high step-up converter integrates two inputs

Figure 1 (a) illustrates Conventional designs for dual-input step-up converters Fig. 1 (b) illustrates Proposed ZVT dual input step-up converter, along with the core structure of the ZVT cell. The primary inductors, L_3 and L_4, are connected to the auxiliary input terminals L_{a1} and L_{a2}, which in turn are linked to inductors L_5 and L_6. Switches S_1 and S_2 are the main switches, while D_1 and D_2 function as input diodes. V_{in1}, V_{in2}, and V_o denote the input and output voltages, respectively. C_{S1} and C_{S2} are the snubber capacitors for switches S_1 and S_2. C_o is the output filter capacitor, and R_o represents the load.

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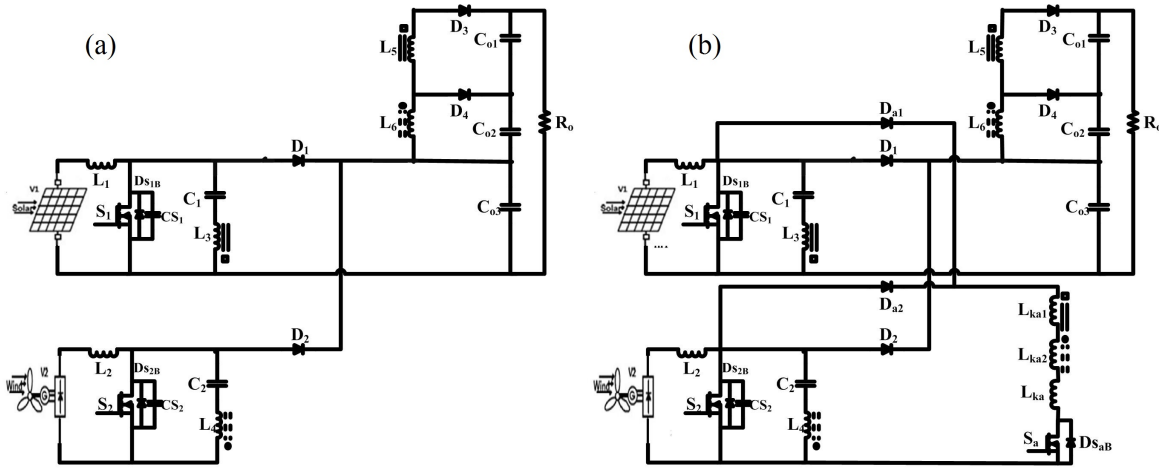

Figure 1. (a) Conventional designs for dual-input step-up converters. (b) Proposed ZVT dual input step-up converter.

The equivalent circuit of the converter is also depicted in Fig. 1 (b), where N_1, N_2 and N_3 correspond to the number of turns in each of the three windings. L_{m3}, L_{m4} are magnetic inductances, with L_{ka} representing both the leakage inductance on one side of the transformer and the magnetically induced inductance from primary to secondary. Additional components include a switch and diodes D_{a1} and D_{a2}. All winding ratios are assumed to be equal, and the N_a/N ratio is defined as proportional to n. A minor transformation occurs in the converter when the duty cycle (D) is less than 50%. For $D >$ 50%, the operational characteristics are detailed below. Each primary circuit operates across fourteen distinct switching modes. However, due to the symmetry in the dual-input topology, only seven modes related to the operation of main switch S_1 are analyzed in detail.

Figures 2 and 3 provide the corresponding waveform diagrams and equivalent circuits for each mode. Prior to time t_0, switch S_2 and diode D_1 are assumed to be turned off, while all other semiconductor devices are in the on-state. At this moment, C_{S1} is charged to the output voltage V_{out}.

Mode 1 [t_0–t_1] (Fig. 3 (a)): To charge C_{S1} and enable Zero-Voltage Switching (ZVS) for switch S_1, the auxiliary circuit must be activated prior to applying the gate signal to S_1. At time t_0, auxiliary switch S_a is turned on. Due to the presence of series leakage inductance L_{ka}, both diode D_{a1} and switch S_a conduct under Zero-Current Switching (ZCS) conditions. As a result of the positive voltage across L_{ka}, the current I_{Lka} begins to rise, while the current through diode D_1 decreases accordingly. At time t_1, the diode current I_{D1} reaches zero, turning D_1 off under ZCS conditions and thereby ending this switching mode. During this interval, the circuit behavior can be described by the following equations:

$$I_{Lka}(t) = \frac{V_o[1 - n(1 - 2D)](t - t_0)}{L_k a} \tag{1}$$

$$I_{D1}(t) = I_{L1} - (n + 1)I_{Lka}(t) \tag{2}$$

where I_{L1} represents the current through L_1, which equals half of the midpoint input current ($I_{\text{in}}/2$), accounting for the distribution between the two components.

Mode 2 [t_1-t_2] (Fig. 3 (b)): At time t_1, diode D_1 turns off, initiating a resonant transition between capacitor C_{S1} and inductor L_{ka}. By the end of this mode, the energy initially stored in C_{S1} is fully transferred to L_{ka}, resulting in the voltage across C_{S1} (V_{CS1}) dropping to zero. At this moment, switches S_1 and S_2 are turned on under ZVS conditions. The corresponding resonance behavior can be described by the following equation:

$$I_{Lka}(t) = A + B\sin(\omega(t - t_1)) \tag{3}$$

$$V_{Cs1}(t) = \left[L_{ka}\frac{dI_{Lka}}{dt} + 2nV\right]\frac{1}{n+1} \tag{4}$$

where

$$\omega = \frac{n+1}{\sqrt{L_{ka}C_{S1}}} \tag{5}$$

$$A = \frac{I_{Lm}}{n+1} \tag{6}$$

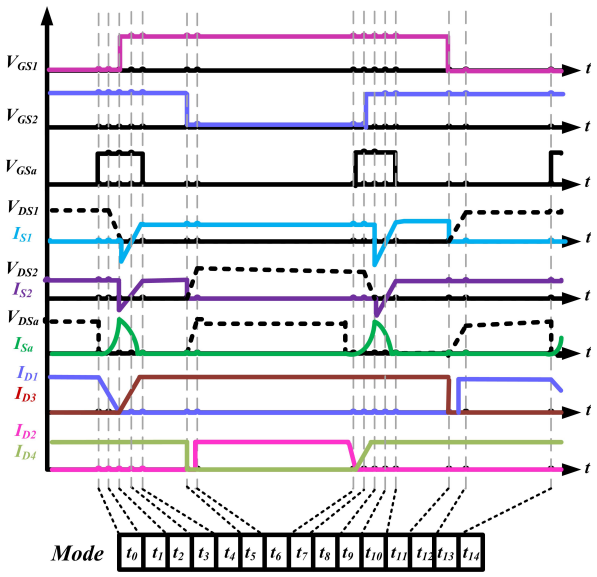

Figure 2. Theoretical waveforms.

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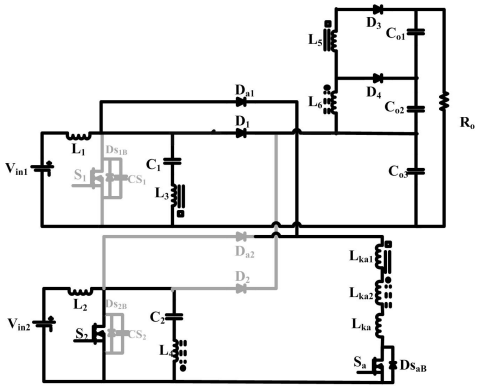

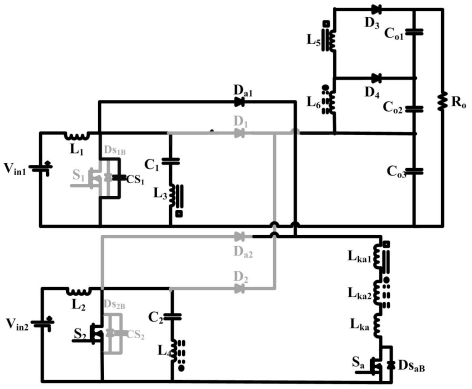

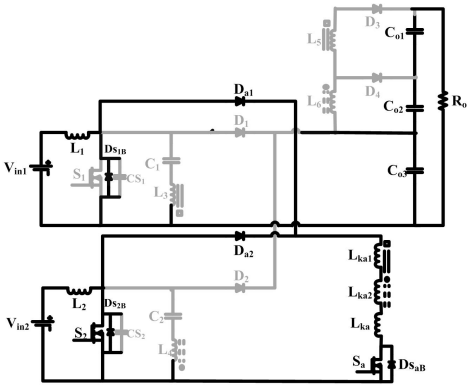

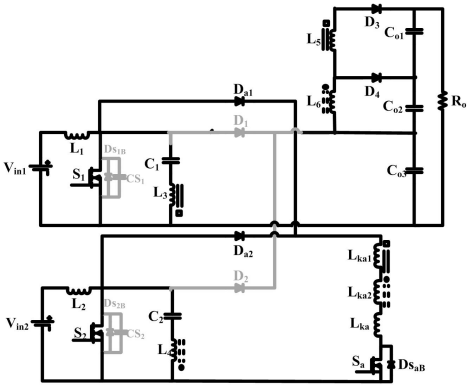

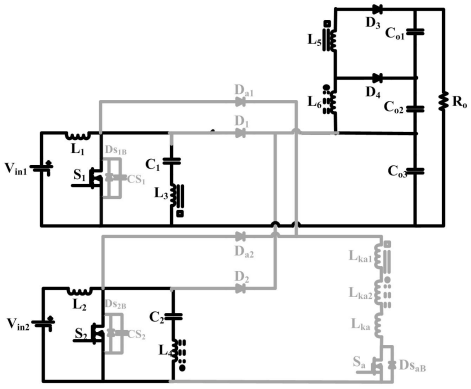

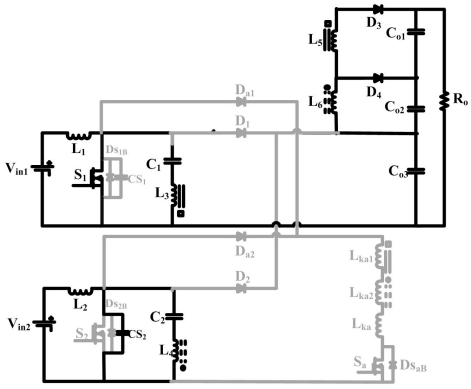

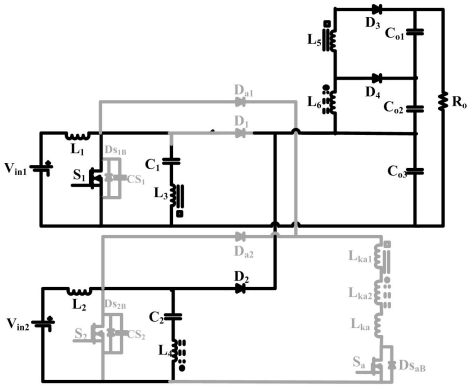

Figure 3. Equivalent circuit models of each mode.

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$$B = \frac{V_{\text{out}}[1 - n(1 - 2D)]}{\omega_{Lka}} \tag{7}$$

Mode 3 [t_2-t_3] (Fig. 3 (c)): At time t_2, the anti-parallel diodes of S_1 and S_2 are turned on. During this mode, the voltage decreases due to a voltage source associated with I_{Lka}, with the expression $-(V_{La1} + V_{La2} = -2nV_{\text{in}}$, which results from the secondary side reflection of L_1 and L_2. The anti-parallel diodes, T_3, S_1, and S_2, turn off under Zero Current Switching (ZCS), marking the end of this mode. During this interval, the gate signal for S_1 can be applied, enabling the switch to turn on under Zero Voltage Switching (ZVS) conditions, while the current through D_3 increases under ZCS conditions. The following equation applies to this mode:

$$I_{sa}(t) = I_{Lka}(t) = I_{Lka}(t_2) - \frac{2n(1 - D)V_{\text{out}}}{L_{ka}}(t - t_2) \tag{8}$$

where $I_{Lka}(t_2)$ can be determined from the previous equation (3) by substituting t_2 for t.

Mode 4 [t_3-t_4] (Fig. 3 (d)): In this mode, I_{Lka} decreases linearly at a constant rate until it becomes zero at t_4, which leads to Sa turning off under ZCS conditions.

Mode 5 [t_4-t_5] (Fig. 3 (e)): In this mode, both main switches are activated, while the auxiliary circuit is turned off. L_1 and L_2 are linearly charged by the input voltage source V_{in}, while the output capacitor supply the load.

Mode 6 [t_5–t_6] (Fig. 3 (f)): At the start of this mode, the ZVS condition of S_2 is interrupted by the capacitor C_{S2}. During this transition, the current in L_2 charges C_{S2} almost linearly. At t_6, the drain-source voltage of S_2 ($V_{Ds2} = V_{CS2}$) increases to V_{out}, causing D_2 to turn on. The following equation can be written for this period:

$$V_{Ds2} = V_{CS2} = \frac{I_{L2}}{C_{S2}}(t - t_4) \tag{9}$$

Here I_{L2} is the current of L_2.

Mode 7 [t_6–t_7] (Fig. 3 (g)): During this mode, the stored energy is transferred to the gate of L_2, while L_1 continues to be linearly charged by V_{in1}. At t_7, the second half of the switching cycle starts, and the auxiliary switch is turned on once more to sustain the ZVS condition for S_2 as it turns off.

3. Analysis of the converter

To achieve Zero Voltage Switching (ZVS) for the main switches, diode D_1 must turn off at time t_1, initiating a resonant loop with inductor L_{ka}. L_{ka} is part of the auxiliary circuit, which also includes capacitor C_{S1} and the output voltage across the three inductors. This resonant loop enables the discharge of C_{S1}. Consequently, the inductance in the auxiliary circuit must be lower than the equivalent impedance determined by the output voltage, establishing a design criterion valid for any $n > 0$. According to equation (4), C_{S1} can be fully discharged in Mode 2, provided certain conditions are met. The minimum required time interval to turn off the switch and trigger diode conduction is denoted as TZVT, which is the combined duration of Modes 1 and 2. Specifically, TZVT represents the minimum delay before applying the main gate signal to the switch. ZVS occurs when the main switch turns off with zero voltage across its, minimizing switching losses. Zero Current Switching (ZCS), on the other hand, occurs when the auxiliary switch turns on with zero current through it, also reducing switching losses. To maintain ZCS, it is essential to remove the control signal from the auxiliary gate once the auxiliary current (I_{Sa}) drops to zero. The time during which the auxiliary switch remains off is critical for sustaining ZVS during the transition of the main switch between its on and off states. Proper synchronization is important to ensure efficient operation of both switches, minimizing energy losses and maintaining soft-switching performance.

3.1 Voltage gain

The voltage conversion ratio, which relates the output voltage to each input source voltage, can be formulated as:

$$V_{Co3} = \frac{V_{\text{in1}}}{1 - D_1} = \frac{V_{\text{in2}}}{1 - D_2} \tag{10}$$

$$V_{Co1} = \frac{nD_1V_{\text{in1}}}{1 - D_1} \tag{11}$$

$$V_{Co2} = \frac{mD_2V_{\text{in2}}}{1 - D_2} \tag{12}$$

$$V_o = V_{Co1} + V_{Co2} + V_{Co3} = \frac{(1 + nD_1)V_{\text{in1}}(1 - D_2) + mD_2V_{\text{in2}}(1 - D_1)}{(1 - D_1)(1 - D_2)} \tag{13}$$

If $V_{\text{in1}} = V_{\text{in2}}$ and $D_1 = D_2$ the voltage conversion ratio It can be considered as such:

$$\frac{V_o}{V_{\text{in}}} = \frac{1 + (m + n)D)}{1 - D} \tag{14}$$

$$m = n \rightarrow \text{Gain} = \frac{V_o}{V_{\text{in}}} = \frac{1 + 2nD}{1 - D} \tag{15}$$

3.2 Voltage stresses athwart power switches and diodes

The association between the output voltage and the voltage of the individual input sources can be written as Semiconductors are designed to endure the voltage applied to them, which is required. The proposed converter has less voltage across the current switches/diodes, so it works in the same way as a conventional step-up converter. The power converter can be calculated using the following equation:

$$V_{S1} = V_{S2} = V_{D1} = V_{D2} = \frac{V_o}{1 + 2nD} \tag{16}$$

$$V_{S3} = V_{D3} = \frac{V_o}{1 + 2nD} + V_{Cr,P} \tag{17}$$

$$V_{D5} = V_{D4} = \frac{V_o(n + 1) - 1}{1 + 2nD} \tag{18}$$

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3.3 Design process

The design of the converter is presented, and the conversion process is demonstrated using the example of a two-phase ZVT converter. In this case, the input voltages are $V_{in1} = 24$ V and $V_{in2} = 96$ V, with an output voltage of $V_o = 10$ V, a total output power of 300 W, and a switching frequency of $f_{sw} = 100$ kHz. Based on the characteristics of the operating structure, it is assumed that $L_1 = L_2 = L_{in}$, $C_{S1} = C_{S2} = C_S$, and that S_1 is identical to S_2, as well as D_1 being identical to D_2.

3.4 Selection of passive elements

The magnetic inductors (L_{m3}, L_{m4}, L_{m5}, L_{m6}, L_{ka1}, and L_{ka2}) and the output capacitor (C_o), used as amplifier inductors, are designed similarly to a simple boost converter, as referenced in [28]. As illustrated in Table 1, a 10 µF electrolytic capacitor was used for C_{o1}, C_{o2}, and C_{o3}, with an inductance value of 200 µH for L_{in} to maintain continuous conduction mode (CCM) operation. According to equations (14) and (15), the voltage across the switch and the output diode is 330 volts. Therefore, the C3M0015065D can be selected as the main switch, and the MUR860 as the diode. The same semiconductor and diode types can be used for ZVT cells, as detailed in the following section.

3.5 Auxiliary circuit configuration

The auxiliary circuit is primarily designed to enable soft switching for the main switches while ensuring smooth transitions for all other semiconductor devices. Due to simple structure of The auxiliary circuit, only the values for L_{ka}, C_S, and the turns ratio n need to be determined.

1) Capacitors and snubber inductances are selected as 1 nF and 100 µH, respectively, as referenced in [29]. Thus, 100 µH is chosen for the snubber inductance used. This value can be achieved with the connected inductor.

2) The condition $I_{Lka}(t_2) = I_{Sa}(\max)$ must exceed the combined maximum values of $I_{L1}(\max)$ and $I_{L2}(\max)$ to ensure that the anti-parallel diodes S_1 and S_2 operate in mode 3 under Zero Voltage Switching (ZVS) conditions.

3) Once the snubber capacitor L_{ka} is discharged, the auxiliary switch should be turned off as quickly as possible to minimize conduction losses in the auxiliary circuit and impose less limitations on the duty cycle (D). Additionally, it should be turned off before the main switch S_2 is activated. In other words, the duration of mode 3 and 4 ($t_{2,4} = t_4 - t_2$) should be much shorter than $t_{2,5} = t_5 - t_2$, as shown in Fig. 2.

$$T_{25(\min)} = D_{\min} T_{sw} - \frac{T_{sw}}{2} \tag{19}$$

$$T_{24(\max)} \leq 0.2 T_{25(\min)} \tag{20}$$

where:
T_{sw} represents the switching time. Therefore, considering equation (8), the turns ratio n must be greater than 0.26 to satisfy equation (20).

4) The duration of mode 2 should be less than 10% of the total transmission mode duration. From mode 6, C_S should be less than 8.7 nF.

5) The current stress on the auxiliary switch should be less than twice the sum of $I_{L1}(\max)$ and $I_{L2}(\max)$. Therefore, according to equation (18), C_S should be less than 1.5 nF.

Thus, considering modes 1, 5, and 6, the value of C_S is chosen to be 1 nF. By selecting these values for L_{ka}, C_S, and n, the situation specified by (10) and (11) will always be fulfilled. In addition, controller circuit proposed in figure 4. By IC ucc28220 and logic circuit can be made required signal for gates. The parameters have been designed in this way based on practical results.

$$C_{S1} > \frac{I_{sw} tf}{2V_{sw}} = \frac{0.76 * 4.5 \text{ ns}}{2 * 60} = 0.028 \text{ nF} \simeq 1 \text{ nF}. \tag{21}$$

$$C_{S2} > \frac{I_{sw} tf}{2V_{sw}} = \frac{0.9 * 4.5 \text{ ns}}{2 * 24} = 0.08 \text{ nF} \simeq 1 \text{ nF}. \tag{22}$$

$$L_{ka} > \frac{V_{sw} tr}{I_{sw}} = \frac{150 * 4.5 \text{ ns}}{0.9} = 0.9 \text{ µH} \simeq 10 \text{ µH}. \tag{23}$$

Table 1. Significant design specifications.

Symbol	Component	Specification
V_{in1}, V_{in2}	Input voltage	24 V, 60 V
V_{out}	Output voltage	310 V
P_{out}	Output power	300 W
f_{sw}	Switching frequency	100 kHz
S_1, S_2, S_a	Switches	C3M0015065D
D_1, D_2, D_3, D_4, D_5	Diodes	MUR860
C_1, C_2	Charge-pump capacitor	20 µF
C_{o1}, C_{o2}, C_{o3}	Output capacitor	10 µF

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$$
\begin{aligned}
I_C =& C\frac{dv}{dt} => C = \frac{I_C dt}{dv} = \frac{I_o DT}{\Delta V_o} = \frac{I_o D}{\Delta V_o f sw} => \\
& C_o = \frac{0.9 * 0.65}{0.03 * 100} = 2.92\ \mu F, \\
& \frac{1}{C_o} = \frac{1}{C_{o1}} + \frac{1}{C_{o2}} + \frac{1}{C_{o3}}, \\
& C_{o1} = C_{o2} = C_{o3} = 8.7\ \mu F \simeq 10\ \mu F.
\end{aligned} \tag{24}
$$

$$
\begin{aligned}
V_L =& L\frac{di}{dt} => L = V_L\frac{dt}{di} => L_{m1} = \frac{V_{C1} D}{\Delta i f_{sw}} = \\
& \frac{24 * 0.75}{0.01 * 100000} = 180\ \mu H \simeq 200\ \mu H, \\
& L_{m2} = \frac{V_{C2} D}{\Delta i f_{sw}} = \frac{60 * 0.65}{0.02 * 100000} = \\
& 195\ \mu H \simeq 200\ \mu H.
\end{aligned} \tag{25}
$$

$$
\begin{aligned}
L_1 &= \frac{V_{in1} D}{\Delta i f} = \frac{24 * 0.75}{0.02 * 100000} = 90\ \mu H \simeq 100\ \mu H, \\
L_2 &= \frac{V_{in2} D}{\Delta i f} = \frac{60 * 0.65}{0.04 * 100} = 97.5\ \mu H \simeq 100\ \mu H.
\end{aligned} \tag{26}
$$

In Fig. 4 (a) block diagram of the control and gate-driving circuit used to generate the switching signals for the converter. Delay blocks, monostable circuits, and logic circuits are employed to produce the required gate signals. Fig. 4 (b) illustrating the sequence and coordination of the switching pulses.

4. Power losses

This section provides a detailed description of the influence of the non-idea components of the proposed converter on overall losses. Conduction losses in the MOSFET and diode, as well as the conduction losses of the coupled inductors and capacitors, are evaluated by considering non-ideal components. The Zero Voltage Switching (ZVS) condition ensures that no activation drop occurs for the main switch. However, capacitive turn on losses of the auxiliary switch are taken into account. The core losses, which are considered negligible, can be minimized. The conduction losses of the switches are determined based on RMS current, while discharge losses are calculated based on The drain-source on resistance. The conduction loss of a MOSFET can be estimated as follows:

$$
\begin{aligned}
& P_{\text{Conduction}-sw} = R_{DS}(I_{\text{RMS}'S1} + I_{\text{RMS}'S2} + I_{\text{RMS}'Sa} = \\
& 0.015(4.12 + 28.09 + 0.32) = 0.49\ \text{W}.
\end{aligned} \tag{27}
$$

Due to the Zero-Voltage Switching (ZVS) condition achieved for the main switch, its capacitive turn-on losses are effectively eliminated. Consequently, only the capacitive turn-on losses associated with the auxiliary switch remain, which can be quantified as follows:

$$
\begin{aligned}
& P_{cto-sa} = \frac{1}{2} C_{o-s} V_{sw}^2 f_{sw} = \\
& \frac{1}{2} * 289 * 10^{-12} * 982 * 100 * 10^3 = 0.139\ \text{W}.
\end{aligned} \tag{28}
$$

The conduction losses associated with all diodes are determined by their respective forward voltage drops and the average current flowing through each device. These parameters can be derived as follows:

$$
\begin{aligned}
& P_{\text{Conduction}'\text{main } D} = V_f(I_{avg'D1} + I_{avg'D2} + I_{avg'D3} + \\
& I_{avg'D4} = 1.5(0.9 + 0.94 + 0.82 + 0.8) = 5.19\ \text{W}.
\end{aligned} \tag{29}
$$

$$
\begin{aligned}
& P_{\text{Conduction}'\text{aux } D} = V_f I_{avg'D_{a1}} + \\
& V_f I_{avg'D_{a2}} = 1.5(0.01 + 0.036) = 0.069\ \text{W}.
\end{aligned} \tag{30}
$$

The conduction losses in the inductors are also taken into account due to the presence of their inherent parasitic resistances. These losses are evaluated using the following expressions:

$$
\begin{aligned}
& P_{\text{Capacitors}} = R_{C1} I_{\text{RMS}'C1}^2 + R_{C2} I_{\text{RMS}'C2}^2 + R_{Co} I_{\text{RMS}'Co}^2 = \\
& 0.2 * 0.65^2 + 0.2 * 0.99^2 + 2.3 * 0.37^2 = 0.65\ \text{W}.
\end{aligned} \tag{31}
$$

The power losses associated with the capacitors are also taken into account, as they are a function of the equivalent

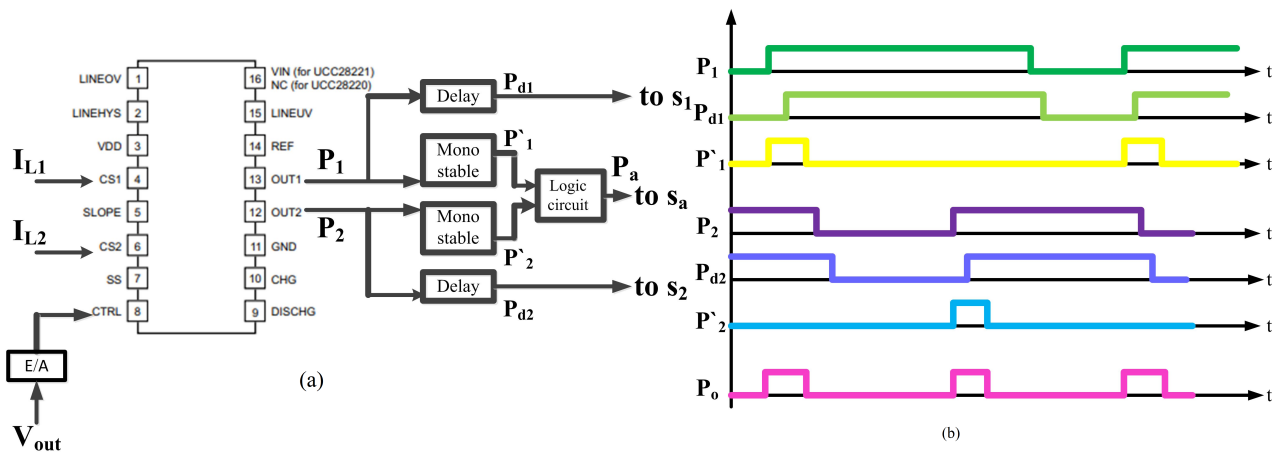

Figure 4. (a) Structural diagram of the controller. (b) Generated pulses.

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series resistance (ESR) and the current flowing through them. These losses are computed as follows:

$$P_{\text{winding}} = R_{L1} I^2_{\text{RMS}'L1} + R_{L2} I^2_{\text{RMS}'L2} + R_{L_{m3}} I^2_{\text{RMS}'L_{m3}} + R_{L_{m4}} I^2_{\text{RMS}'L_{m4}} + R_{L_{m5}} I^2_{\text{RMS}'L_{m5}} + R_{L_{m6}} I^2_{\text{RMS}'L_{m6}} + R_{Lka} I^2_{\text{RMS}'Lka} = 0.98 + 0.85 + 0.93 + 0.87 + 0.63 + 0.65 = 4.91 \text{ W}. \quad (32)$$

In Fig. 5 (a) comparison of efficiency versus output power for the proposed ZVT converter and the conventional hard-switching converter. The ZVT topology shows higher efficiency over the entire power range. Fig. 5 (b) distribution of power losses among the main components, including diodes, inductors, capacitors, and switches.

5. Experimental results

The 300 W prototype of the hypothetical converter described in the previous section was created for feasibility testing. All switches and diodes are model numbers C3M0015065D and MUR860. In this section, we present the experimental results for the proposed dual-input converter. Figure 6 shows a photograph of the recommended converter. In Figs. 7 (a,b), it can be observed that the main switches are activated in the Zero Voltage Switching (ZVS) state and disabled in the Zero Voltage (ZV) state. As shown in Fig. 7 (c), the auxiliary switch is turned off in the Zero Current (ZC) state. The diode in the main circuit is displayed in the zero-voltage state in Fig. 7 (d). The simulations and theoretical analysis were verified through experiments. However, the current waveforms exhibit some amount of ringing, indicating a discrepancy between the simulations, theoretical analysis, and experimental results. This discrepancy is attributed to the resonance between parasitic capacitors and inductors. Specifically, the resonant inductor and the auxiliary output capacitor resonate at the same frequency. Using data collected under controlled laboratory conditions, a performance curve was generated. The efficiency of the recommended converter is approximately 3% higher than the efficiency of the hard-switching option, as indicated in the graph. This improvement is achieved by eliminating losses such as line losses. efficiency was obtained under test conditions comprising a switching frequency of 100 kHz, an ambient temperature of 60 °C, and a nominal load of 200 W.

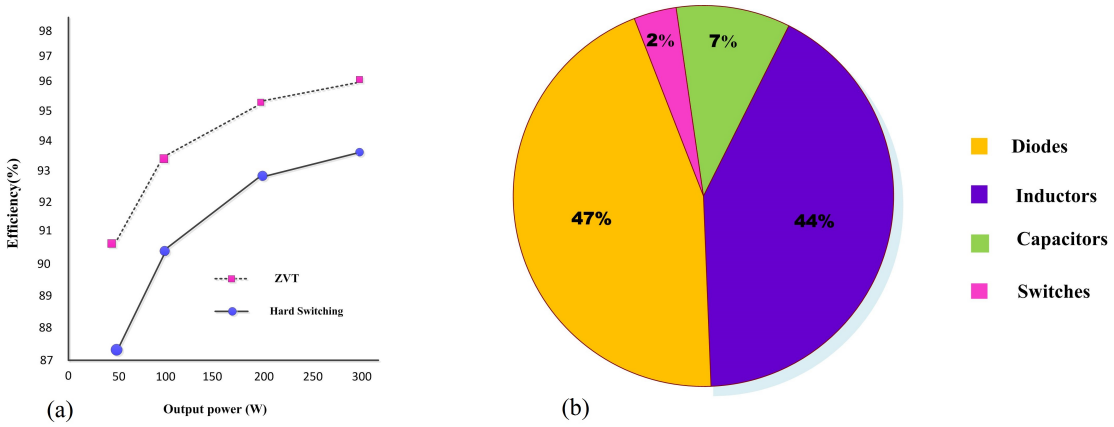

Figure 5. (a) Efficiency of the recommended converter. (b) The losses distribution of the recommended converter.

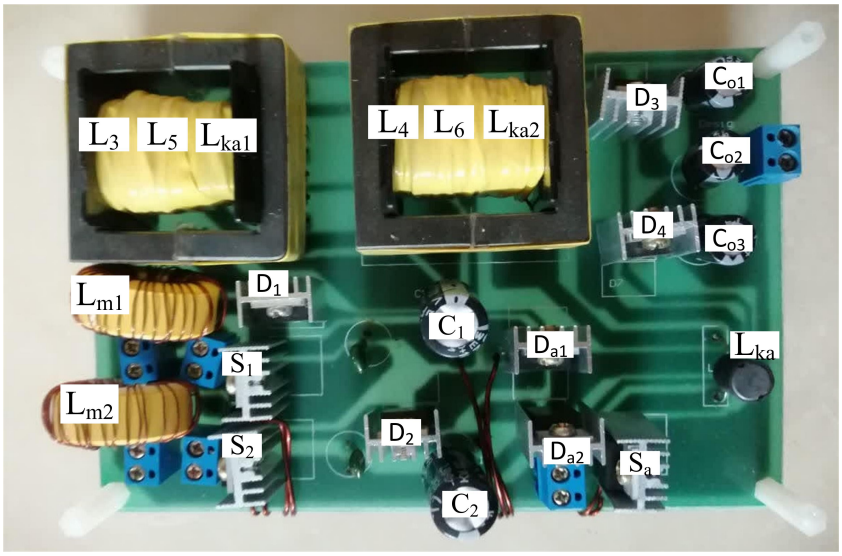

Figure 6. Photograph of the Recommended converter.

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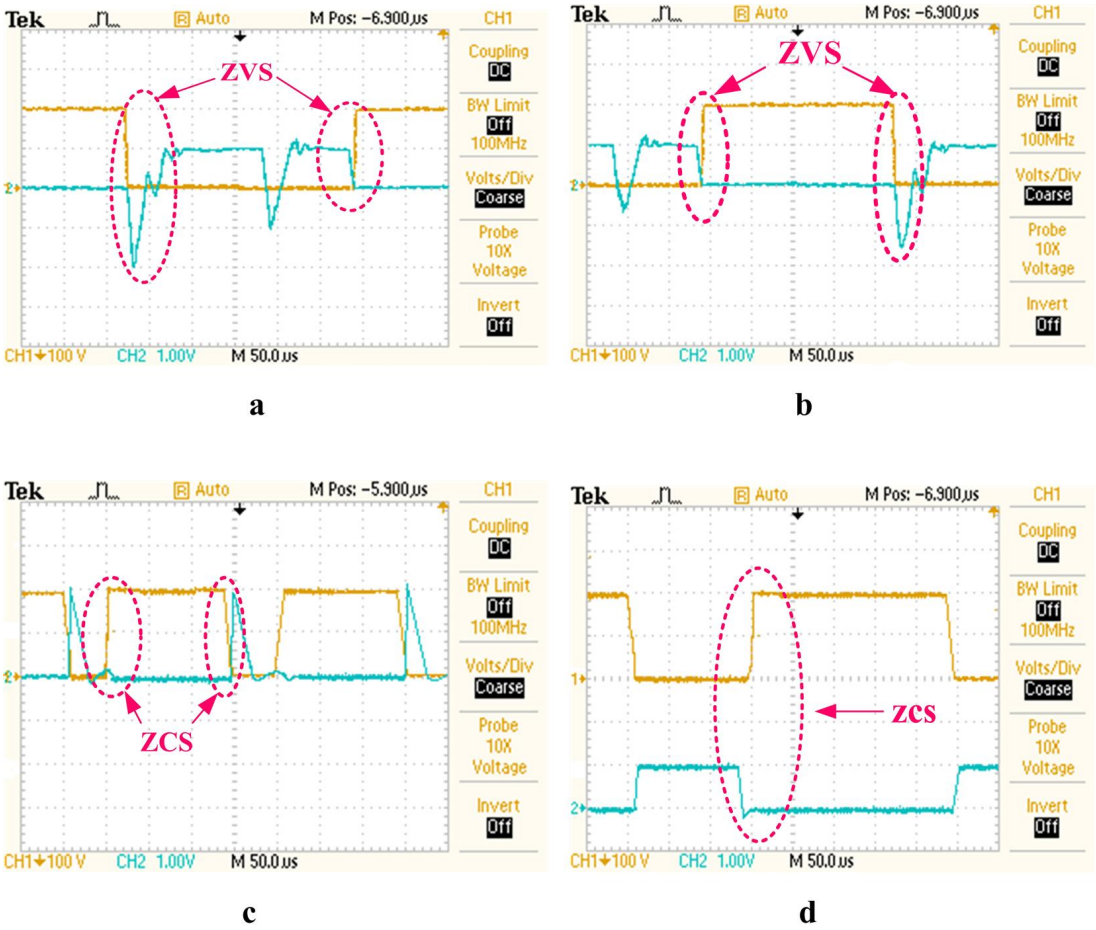


Figure 7. (a) Waveforms of voltage and current. Main switch S_1. (b) Waveforms of voltage and current. Main switch S_2. (c) Waveforms of voltage and current. auxiliary switch (d). Waveforms of voltage and current. Main diode D_1.

6. Practical EMI test results

Electromagnetic interference (EMI) measurements were conducted using a CISPR22-compliant LISN and a GWINSTEK GSP-830 spectrum analyzer. The EMI performance of the proposed converter, operating under full load, was compared to that of a conventional hard-switching converter. Both systems used identical components and setups. In this configuration, the spectrum analyzer was connected to the RS, respectively as shown in figure 8 and the LISN was placed between the converter's input and the power supply's 24 V and 60 V outputs [28]. Measurements were taken in peak detection mode to account for the significant influence of common-mode noise on differential-mode interference. Figures 9 and 10 display the EMI characteristics for both converter types. According to the CISPR 22 standard, the conducted EMI frequency range spans from 150 kHz to 30 MHz [29], with EMI levels on the vertical axis ranging from 20 dBµV to 100 dBµV. Specifically, Figs. 9 (a) and 10 (a) show the EMI of the proposed converter, while Figs 9 (b) and 10 (b) show the EMI of the hard-switching converter, which recorded peaks of 73 dBµV and 84 dBµV, respectively. Notably, the proposed converter exhibited an EMI peak of 13 dBµV-9 dBµV lower than the peak observed in the hard-switching design.

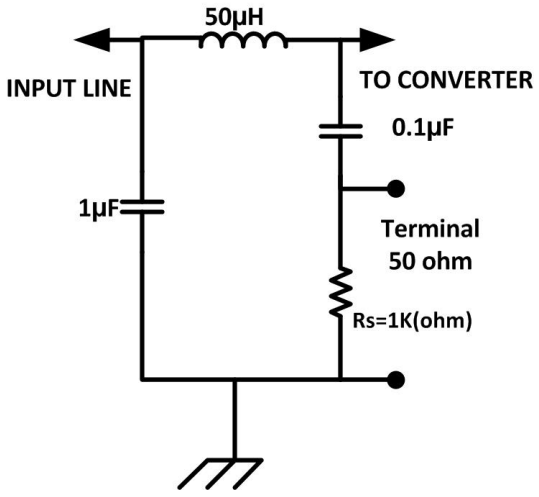
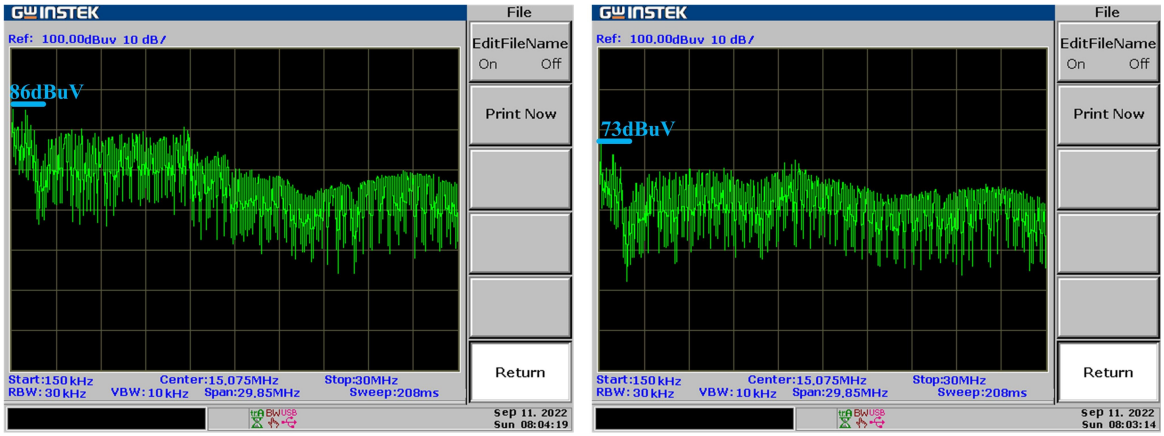


Figure 8. Prototype circuit of CISPR22 LISN [28].

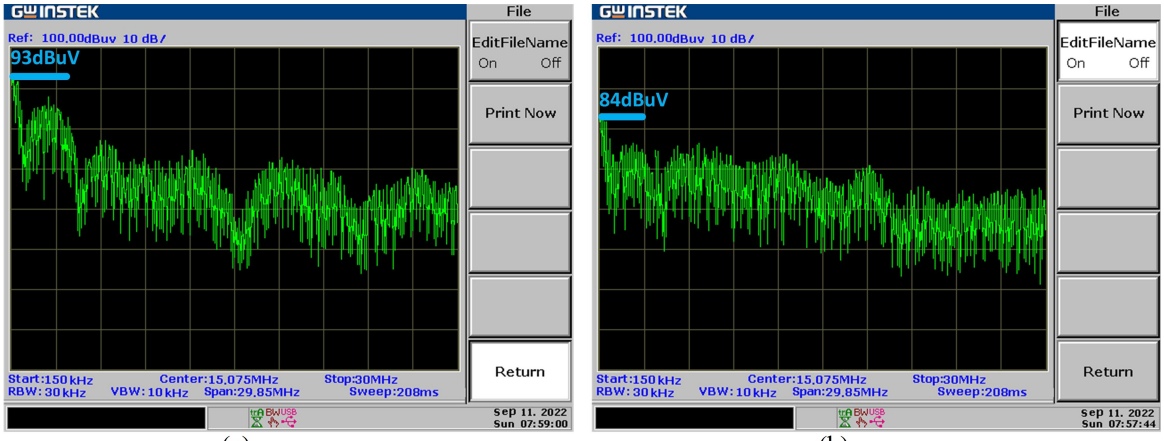
7. Comparative analysis of the proposed converter against alternative designs

Table 2 provides a comparative analysis between the proposed converter and recently reported topologies in terms of maximum voltage gain, peak voltage stress on switches and diodes, switching technique, efficiency, and the number of components. The converters presented



(a) (b)

Figure 9. Full-load EMI Consequences of (a) Hard switching topology for V_{in1}. (b) Recommended converter V_{in1}, (Horizontal axes: 150 kHz – 30 MHz, Vertical axes: 20 – 100 dBμV).



(a) (b)

Figure 10. Full-load EMI Consequences of (a) Hard switching topology for V_{in2}. (b) Recommended converter V_{in2}, (Horizontal axes: 150 kHz – 30 MHz, Vertical axes: 20 – 100 dBμV).

Table 2. The comparison of accomplishing the converters and the proposed structure.

Converter	Voltage gain	Maximum voltage of switch	Maximum voltage of diode	Soft switching	Efficiency (%)	Number of				
						MC*	SW	D	C	T**
[30]	$\frac{3-2D}{(1-D)^2}$	$\frac{V_o}{3-2D}$	V_o	Hard	91.7	3	3	3	3	12
[31]	$\frac{5}{1-D}$	$\frac{V_o}{5}$	$\frac{2V_o}{5}$	Hard	94.24	2	2	5	5	14
[32]	$\frac{4}{1-D}$	$\frac{V_o}{4}$	$\frac{V_o}{2}$	Hard	95	2	2	6	6	16
[33]	$\frac{4}{1-D}$	$\frac{V_o}{4}$	$\frac{V_o}{2}$	ZVS	95	2	2	8	6	18
[34]	$\frac{3+D}{1-D}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	Hard	94.7	2	2	3	3	10
[35]	$\frac{2}{1-D}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	Hard	90.5	2	2	3	4	11
[36]	$\frac{n}{1-D}$	$\frac{V_o}{n}$	V_o	ZCS	94	1	2	4	3	10
[37]	$\frac{2nD}{1-D}$	$\frac{V_o}{2nD}$	$\frac{V_o}{2-2D}$	Hard	90.2	4	2	6	2	14
[38]	$\frac{(2-D_4)(1-D_1)V_2+D_1V_1}{(1-D_1)(1-D_2)(1-D_4)}$	$\frac{V_{in}}{1-D_1}$	$\frac{V_o}{2-D_4}$	Hard	93.5	3	4	4	4	15
[39]	$\frac{2+n}{1-D}$	$\frac{V_o}{2+n}$	$\frac{(1+n)V_o}{2+n}$	Hard	94.5	1	3	5	3	12
[40]	$\frac{V_{in1}+V_{in2}(1-D_1)}{(1-D_1)(1-D_2)}$	$\frac{(1-D_3)V_o}{2}$	V_o	Hard	95	3	3	4	3	13
[41]	$\frac{V_{in2}}{(1-D_1)}+\frac{V_{in1}(1+D_3)}{(1-D_3)}$	V_o	V_o	ZVS/ZCS	95.5	3	4	3	2	11
Proposed	$\frac{1+2nD}{1-D}$	$\frac{V_o}{1+2nD}$	$\frac{V_o}{1+2nD}$	ZVS	96.3	2	3	7	5	17

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in [30, 32, 34, 35, 37, 38, 39, 40] lack soft-switching capability and exhibit lower efficiency compared to the proposed design. Although the topology in [33] achieves a desirable voltage gain and benefits from soft switching, it involves a greater number of components. The converter introduced in [36] features a lower component count with zero-current switching; however, it shows inferior performance in terms of voltage gain and voltage stress, and its main switch is subject to capacitive turn-on losses. The converter in [41] offers an extremely high voltage gain and reduced component count, yet it suffers from high peak voltage stress across both the switch and the diode.

8. Extraction of auxiliary circuit

The proposed converter implements a new auxiliary ZVT circuit, designed to use as few components as possible in order to achieve a soft-switching state for the power switch. It is recommended to employ a dual-input boost converter that utilizes zero-voltage transition (ZVT). In addition to the benefits previously discussed for multi-input converters, the efficiency of the recommended converter is enhanced by using a single auxiliary circuit to establish soft-switching conditions for all semiconductor components. A sample of this setup is shown in figure 11.

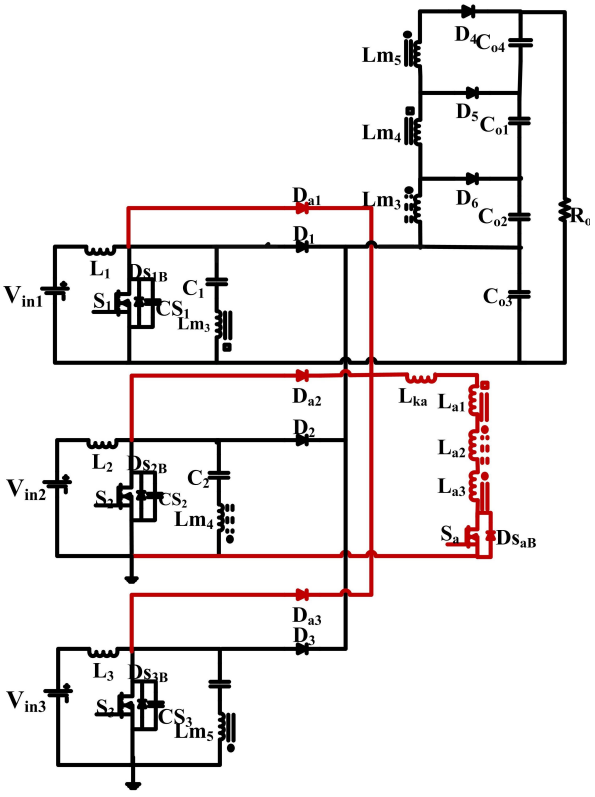

Figure 11. Extraction high step-up converter with the recommended ZVT auxiliary circuit.

9. Conclusions

In this study, a novel ZVT converter with dual inputs is proposed. All semiconductor components benefit from the presence of a soft-switching technique. Various operational modes, simulation results, and experimental outcomes are analyzed in conjunction with theoretical predictions. The simulation results demonstrate that the proposed method can improve the efficiency of the converter by approximately 3% at nominal load conditions. The reported efficiency was obtained under test conditions comprising a switching frequency of 100 kHz, an ambient temperature of 60 °C, and a nominal load of 200 W.

Nomenclature.

ZCT	Zero current transition
MIC	Multi-input converter
PFC	Power factor correction
EMI	Electromagnetic interference
I_{Lm}	Magnetizing current
I_{Lk}	Leakage inductance current
V_{DS}	Drain source voltage
ω	Angular frequency
ZVT	Zero Voltage Transition
VR	Voltage regulation
ZCS	Zero current switching
ZVS	Zero voltage switching
n	Turn ratio
m	Tertiary turn ratio
D	Duty cycle
V_{cs}	Snubber voltage

Authors contributions
All authors contributed equally to the conception, design, execution, and writing of this work. All authors read and approved the final manuscript.

Availability of data and materials
The authors declare that the data supporting the findings of this study are available within the paper.

Conflict of interests
The authors assert that they do not have any identifiable conflicting financial interests or personal relationships that might be perceived to influence the work presented in this paper.

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