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An Interleaved Step-up DC-DC Converter with Lossless Snubber

Arman Hovsep[1], Majid Delshad[2], Bahador Fani[3], Mahdi Sajadieh[4]

1- Department of Electrical Engineering, Isf.C., Islamic Azad University, Isfahan, Iran.
Email: arman.hovsep@iau.ir

2- Department of Electrical Engineering, Isf.C., Islamic Azad University, Isfahan, Iran.
Email: delshad@khuisf.ac.ir (Corresponding author) 0000-0002-2637-5965

3- Department of Electrical Engineering, Isf.C., Islamic Azad University, Isfahan, Iran.
Email: b.fani@khuisf.ac.ir

4- Department of Electrical Engineering, Isf.C., Islamic Azad University, Isfahan, Iran.
Email: m.sajadieh@khuisf.ac.ir

ABSTRACT:

In this paper, an interleaved step-up converter with two lossless snubbers is introduced, where the snubbers ensure zero-current switching for the main switches, eliminating the need for extra switches. Additionally, the energy from the snubbers is transferred to the output. All the switches in the converter are grounded, which negates the requirement for an isolated driver circuit. Another key characteristic of the converter is the balanced current across both phases. Moreover, the low voltage stress on the switches allows for the use of switches with lower drain-source resistance. The proposed converter has been thoroughly analyzed, and to validate the theoretical analysis, a prototype was simulated in PSPICE software and a 100W prototype was fabricated. The efficiency at full load is 96%, showing a 5% improvement compared to its hard-switching counterpart.

KEYWORDS: Step-up converter, Lossless snubber, Zero-voltage switching, Zero-current switching.

1. INTRODUCTION

Renewable energy sources, such as solar, wind, hydro, geothermal, and biomass, are naturally replenishing and not constrained by the limitations associated with fossil fuels. The adoption of renewable energy technologies not only mitigates environmental pollution but also reduces dependence on finite energy resources like oil and gas. Over the past few decades, significant advancements in renewable energy technologies, particularly in solar and wind power generation, have led to substantial reductions in cost and improvements in efficiency [1-3]. Consequently, the integration of renewable energy into industrial and daily applications has become a central global priority.

Interleaved boost converters are commonly employed as interface circuits in renewable energy systems, which often experience unstable, unregulated, and low output voltages, and their development is ongoing [4,5].

These converters typically involve the combination of two or more basic boost converters to achieve higher output current and power [6,7].

Interleaved boost converters offer several advantages, including the distribution of power across branches, rapid transient response, reduced size of passive components, and minimized input current and output voltage ripple, all of which are crucial for system performance [8,9]. Increasing the operating frequency of the converter enables higher power density and improved transient response. However, raising the frequency in hard-switching converters can lead to elevated switching losses and increased electromagnetic interference, thus soft-switching techniques are employed to minimize switching losses and enhance the overall efficiency of the converter [10,11]. Numerous soft-switching techniques have been proposed to address these challenges

In [12], an active clamp auxiliary circuit is utilized to enable zero-voltage switching (ZVS) in an interleaved converter. However, since the auxiliary circuit remains operational throughout the entire switching cycle, it leads to increased conduction losses.

An alternative method for achieving ZVS is the zero-voltage transition (ZVT) technique [13,14], where the auxiliary circuit conducts only for a short duration, thereby minimizing conduction losses. In [15], a single auxiliary circuit is employed to establish soft-switching conditions for both branches of the converter, reducing the component count and overall circuit size. In this approach, both the main and auxiliary switches turn off under zero-current switching (ZCS) conditions. However, the auxiliary switch is still subjected to a voltage stress equivalent to the output voltage, which contributes to higher capacitive losses. The work presented in [16] introduces an auxiliary circuit that facilitates soft-switching, ensuring that the main switches operate under both ZCS and ZVS conditions. Nevertheless, the auxiliary switch continues to experience high voltage stress, which can negatively impact overall system efficiency. In [17], a dual-winding structure combined with two auxiliary switches is implemented to achieve ZVS for the main switches and ZCS for the auxiliary switches. This configuration significantly reduces voltage stress on the auxiliary switches, leading to a considerable decrease in capacitive losses. The study in [18] proposes a soft-switching approach by incorporating a pair of series-connected inductors within the auxiliary circuit. The main switches operate under ZVS, while the auxiliary switches undergo ZCS during turn-on and turn-off. However, due to the series inductor configuration, the auxiliary switch experiences voltage stress exceeding the output voltage, resulting in increased capacitive and conduction losses. In interleaved boost converters, integrating a single ZVT cell across multiple branches helps in reducing the number of semiconductor components, which in turn decreases system costs and optimizes the converter's overall size. This paper presents a highly interleaved ultra-step-up converter incorporating two lossless snubber circuits. These snubbers facilitate zero-current switching (ZCS) for the primary switches without introducing additional switching components. Moreover, the stored energy in the snubber circuits is efficiently transferred to the output, enhancing overall efficiency. Additionally, all switches feature a ground-referenced source, eliminating the necessity for an isolated gate driver circuit. Section 2 provides a comprehensive introduction to the proposed converter, detailing its structure and operational principles. Following this, Section 3 presents a thorough analytical evaluation of the converter, including mathematical modeling and performance assessment. In Section 4, both simulation and experimental results are presented to validate the theoretical analysis and demonstrate the converter's effectiveness in practical applications. Finally, in Section 5, a comparative analysis is conducted, benchmarking the proposed converter against existing similar topologies to highlight its advantages and performance improvements.

1. THE PROPOSED INTERLEAVED CONVERTER

In this section, the proposed converter is introduced, and its operation is explained in detail. The working principles, circuit topology, and key design considerations are thoroughly discussed to provide a comprehensive understanding of its functionality.

1.1. Interleaved converter description

The proposed converter is depicted in Fig. 1, comprising two primary sections: a voltage-boosting circuit and a set of lossless snubbers designed to enhance efficiency. The voltage-boosting stage consists of coupled inductors L_{11}–L_{12} and L_{21}–L_{22}, capacitors C_1 and C_2, and diodes D_1, D_{o1}, D_2 and D_{o2}. Additionally, it includes switching

devices S_1 and S_2.

The lossless snubber network is composed of coupled inductors L_{a1}–L_{a2} and L_{a3}–L_{a4}, snubber capacitors C_{r1} and C_{r2}, and auxiliary diodes D_{a1} and D_{a2}. Furthermore, an output capacitor C_o is implemented to minimize output voltage ripple. The switches S_1 and S_2 operate with a phase shift of 180 degrees, while the diodes D_{o1} and D_1, as well as D_{o2} and D_2, function in a complementary manner.

1.2. Converter operation

The proposed converter operates in eight distinct switching Modes within a single switching cycle. The main waveforms of the converter are depicted in Fig. 2, while the equivalent circuits corresponding to each Mode are presented in Fig. 3 to 10. To simplify the analysis, it is assumed that the voltage levels across capacitors C_1, C_2, and C_o do not vary throughout the switching cycle due to their large capacitance.

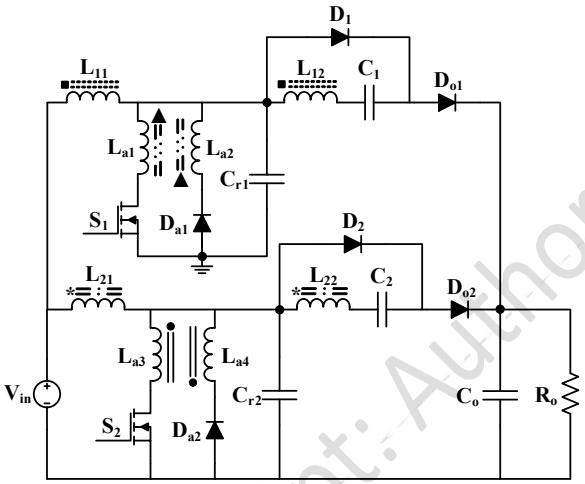


Fig. 1. Schematic of the proposed high step-up

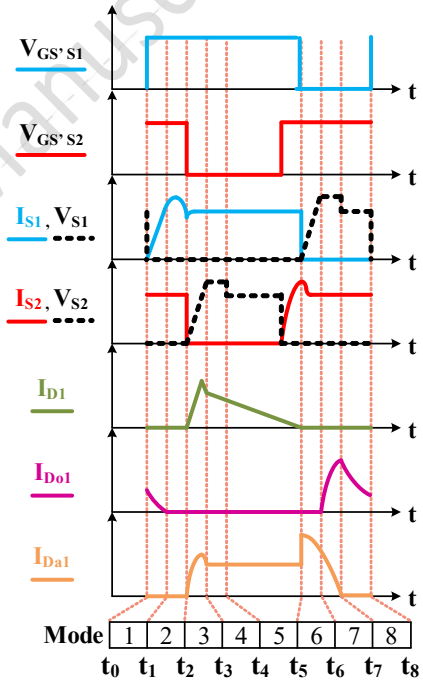


Fig. 2. Main waveforms of the proposed converter

Preceding Mode (Before Mode 1)

Before the first Mode begins, S_2 is ON and S_1 is OFF. This causes diodes D_{o1} and D_2 to conduct, while diodes

D_{o2} and D_1 are OFF.

Mode 1: This Mode starts when S_1 turns ON. The current increases linearly due to the inductor L_{a1}, and the current through D_{o1} decreases linearly until it reaches zero, turning D_{o1} OFF under Zero-Current (ZC) switching. This Mode ends when the current through S_1 reaches the magnetizing current of L_{11}.

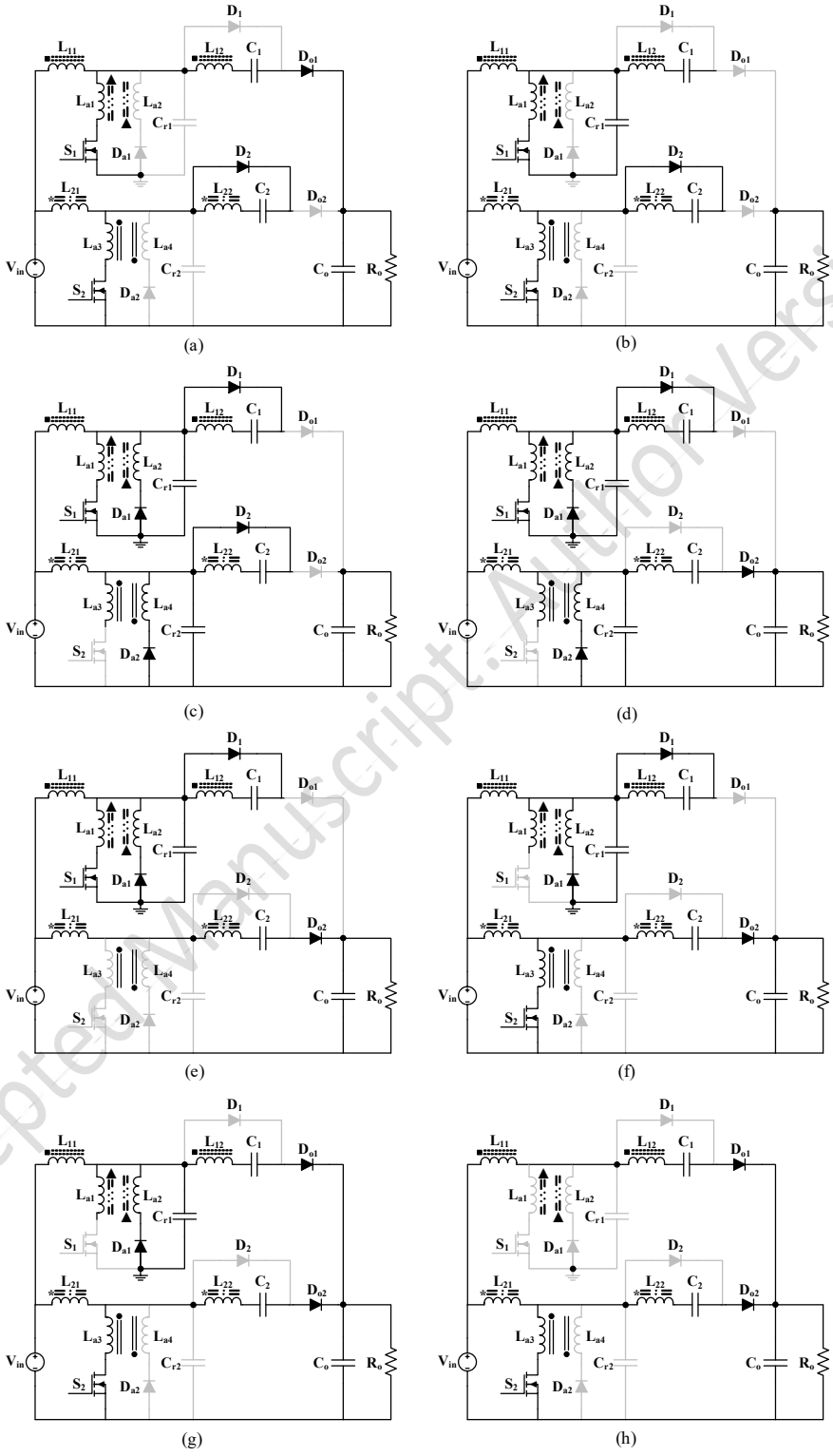


Fig. 3. The equivalent circuit in each mode (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4 (e) Mode 5 (f) Mode 6 (g) Mode 7 (h) Mode 8

Mode 2: When D_{o1} turns OFF, C_{r1} and L_{a1} interact resonantly, transferring energy stored in C_{r1} to L_{a1}. This Mode ends when L_{r1} is fully discharged.

Mode 3: This Mode begins when C_{r1} is fully discharged, causing D_1 and D_{a1} to turn ON under ZC switching. At the same time, S_2 turns OFF, which leads to the linear charging of capacitor C_{r2}.

Mode 4: In this Mode, capacitor C_1 charges through diode D_1, and diode D_{02} remains ON, allowing L_{21} to discharge into the output through D_{02}. Meanwhile, L_{11} is linearly charged.

Mode 5: S_1 remains ON in this Mode, while the current through D_1 decreases linearly. As the energy stored in L_{a3} is depleted, the voltage across S_2 starts to drop. This Mode ends when S_1 turns OFF.

Mode 6: When S_1 turns OFF, capacitor C_{r1} begins charging linearly, and D_1 turns OFF under ZC switching at the end of this Mode.

Mode 7: In this Mode, D_1 turns OFF under ZC switching, and D_{01} turns ON under ZC conditions. L_{11} discharges into the output, while S_2 turns ON and L_{21} charges linearly. The current through the auxiliary diode decreases linearly, and D_{a1} turns OFF under ZC switching at the end of this Mode.

Mode 8: In this Mode, D_a turns OFF, and the snubber associated with switch $\mathbf{S_1}$ is completely removed from the circuit. Meanwhile, L_{11} continues discharging into the output. The Mode concludes when $\mathbf{S_1}$ turns ON again, marking the start of a new switching cycle.

2. EVALUATION OF THE PROPOSED CONVERTER

This section describes the gain characteristics of the converter, the voltage stress on its components, and the design considerations for the snubber elements.

2.1. Converter Gain

The gain of the converter is derived by utilizing the volt-second balance principle on the magnetizing inductor. The relationship between input and output voltage depends on the duty cycle and the transformer turns ratio. By considering the energy transfer mechanism, it is observed that the output voltage increases as the duty cycle approaches its upper limit. A higher turns ratio further enhances the voltage gain, making the converter suitable for high step-up applications. The graph in Fig. 4 illustrates how the gain changes with variations in these parameters.

$$V_{in}DT + (V_{in} - V_{Cr1})(1 - D)T = 0 \quad (1)$$

$$V_{Cr1} = \frac{V_{in}}{1-D} \quad (2)$$

$$V_o = nV_{in} + V_{C1} \quad (3)$$

$$\frac{V_o}{V_{in}} = \frac{n+1}{1-D} \quad (4)$$

2.2. Voltage Stress on Components

The voltage stress on the semiconductor components is analyzed using Kirchhoff's Voltage Law when the switches are in the OFF Mode. The auxiliary winding turns ratio affects the stress levels on the switches, adding an extra voltage component. The impact of this additional stress is visualized in Fig. 5, which shows the normalized voltage stress on different semiconductor elements as the turns ratio changes.

$$V_{S1} = V_{S2} = \frac{Vo}{n+1} \quad (5)$$

$$V_{Do1} = V_{Do} = V_o \quad (6)$$

$$V_{D1} = V_{D2} = \frac{nVo}{n+1} \quad (7)$$

2.3. Design of Snubber Capacitors

To ensure soft switching and reduce voltage spikes, snubber capacitors are designed based on the energy dissipation requirements. The capacitance value is selected considering the switch current, voltage level after turn-off, and the switching transition time. Proper selection of these capacitors minimizes switching losses and improves overall efficiency.

$$C_{r1} = C_{r2} = \frac{I_{sw} t_f}{2V_{sw}} \quad (8)$$

Where I_{sw} is the switch current, V_{sw} represents the switch voltage after turn-off, while t_f denotes the fall time of the switch current.

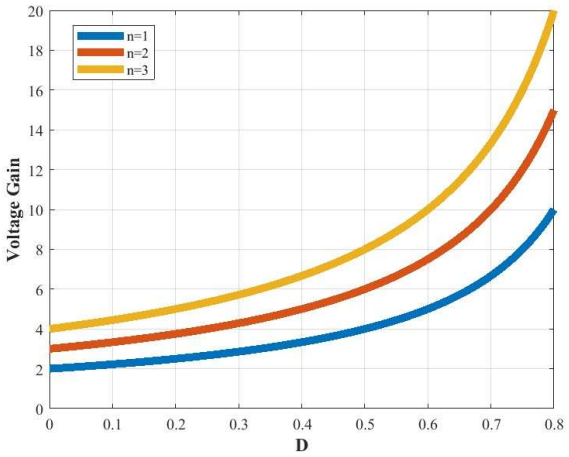


Fig. 4 Converter gain diagram based on variations in the duty cycle and turn ratio.

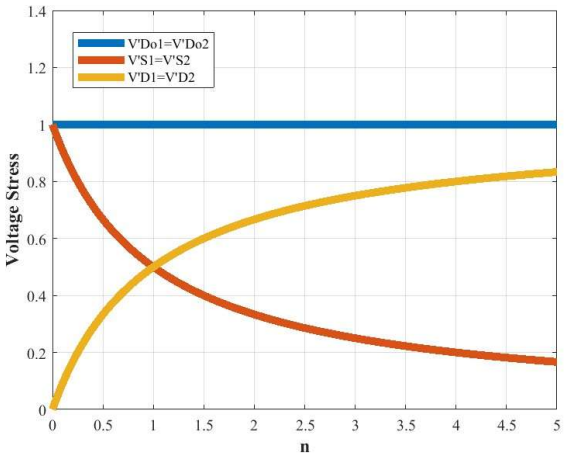


Fig. 5 Normalized stress diagram of the converter's semiconductor components.

2.4. Design of Snubber Inductors

The snubber inductors, which are connected in series with the main switches, are designed to control the switching current slope. Their values are determined based on the voltage across the switches and the required current rise time.

$$L_{a1} = L_{a3} = \frac{V_{sw} t_r}{I_{sw}} \quad (9)$$

Where **tr** refers to the duration required for the switch current to increase from zero to its peak value.

Additional auxiliary inductors are sized in proportion to the transformer turns ratio, ensuring optimal performance. By appropriately choosing these inductors, the voltage stress on switches is mitigated, leading to reduced switching losses and enhanced efficiency.

$$L_{a2} = L_{a4} = m^2 L_{a1} \quad (10)$$

Where m is turns ratio of auxiliary coupled-inductors L_{a3}-L_{a4}.

2.5. Design of Output Capacitor and Magnetizing Inductors

The magnetizing inductors are designed to regulate the current ripple based on the desired operational characteristics. Their values are chosen to ensure stable operation and minimize fluctuations in the energy transfer

process.

$$L_{m1.2} = \frac{V_{in}D}{\Delta I_{Lm}f} \quad (11)$$

Similarly, the output capacitor is selected to effectively filter out voltage ripple, providing a stable DC output. The capacitor's value is determined considering the output voltage ripple requirement and the load resistance to maintain a smooth and consistent output.

$$C_o = \frac{DV_o}{R\Delta V_o f} \quad (12)$$

3. PRACTICAL DESIGN OF PASSIVE COMPONENTS FOR THE PROPOSED CONVERTER

This section presents the design of the proposed converter based on specifications including 100 W output power, 30 V input voltage, and 180 V output voltage, operating at a switching frequency of 100 kHz. The input current ripple is constrained to 0.5 A, while the output voltage ripple is maintained within 0.5 V. The component values are determined using the design methodology outlined in Section 3.

$$C_{r1} = C_{r2} > \frac{I_{sw}t_f}{2V_{sw}} = 0.14nF \quad (13)$$

$$L_{a1} = L_{a3} > \frac{V_{sw}t_r}{I_{sw}} = \frac{98*5*10^{-9}}{2.2} = 2.3\mu H \quad (14)$$

$$L_{m1.2} = \frac{V_{in}D}{\Delta I_{Lm}f} = \frac{30*0.6}{1*10^5} = 180\mu H \quad (15)$$

$$C_{1,2} = \frac{(1-D)V_o}{2\Delta V_o f} = \frac{0.4*0.56}{2*0.2*10^5} = 5.6\mu F \quad (16)$$

$$C_o = \frac{DV_o}{R\Delta V_o f} = \frac{0.6*180}{324*0.5*10^5} = 6.7\mu F \quad (17)$$

It should be noted that, since the calculated values are non-standard, commercially available standard component values have been selected instead, as listed in Table 1.

Table 1. The main specifications of the converter

Specification/element	Part no./Value
Vin	30V
Vo	180V
All switches	20N60C3
All diodes	MUR860
L_{11}, L_{21}	200µH
n	1.4
L_{a1}-L_{a2}	10 µH
m	2
C_1, C_2	10µF
P_O	100W
f_S	100kHz
C_{r1}- C_{r2}	10nF
Co	10 µF

4. SIMULATION AND EXPERIMANTAL RESULTS

In order to assess the validity of the analytical results, the proposed converter was both simulated using PSPICE and experimentally prototyped in the laboratory, based on the design parameters derived in Section 4. Fig. 6 illustrates the experimental setup of the fabricated converter, and Fig. 7 presents a comparative view of the

simulation and experimental outcomes. Figures 7(a)–(d) depict the simulated and experimental voltage and current waveforms of switches S_1 and S_2. As observed, the current through the switches exhibits a positive slope at turn-on, which confirms the achievement of zero-current switching (ZCS). Additionally, the presence of capacitors C_{r1} and C_{r2} results in a gradual voltage rise during the turn-off interval, indicating that the main switches operate under zero-voltage switching (ZVS) conditions. Figures 7(e)–7(g) present the simulated and experimental output current waveforms of diodes D_{o1} D_{o2}, D_{a1} and D_{a2} respectively. The smooth current transition during both turn-on and turn-off confirms zero-current switching (ZCS) operation, effectively mitigating reverse recovery problems. As observed in the experimental waveforms shown in Figures 7(b), 7(d), and 7(g), unintended oscillations occur during the turn-off periods of the switches and diodes, which are not present in the simulation results. These oscillations are caused by the resonance between the leakage inductance and the parasitic capacitances of the diodes and switches, which were neglected in the analytical modeling due to their relatively small values. Figures 7(h) and 7(i) display the simulated and experimental current waveforms of diodes D_1 and D_2. The observed current slopes during turn-on and turn-off confirm zero-current switching (ZCS) operation, effectively preventing reverse recovery effects. As a result, the diodes in the proposed converter contribute minimal conduction losses to the overall system. Fig. 8 shows the measured input current of the proposed converter, which is the sum of the currents from the two branches. As predicted by the analysis, the input current exhibits a low ripple, approximately equal to 0.5 A.

The simulation and experimental findings confirm that the switches operate under zero-current (ZC) switching during turn-on and zero-voltage (ZV) switching during turn-off, while all diodes achieve turn-off under ZC conditions. Furthermore, the low voltage stress on the switches allows for the integration of low drain-to-source resistance switches, enhancing overall efficiency. The observed switch voltage waveforms further validate the effective absorption of leakage inductance energy by the auxiliary circuit, as no noticeable voltage spikes are present.

On the other hand, it can be observed that due to the perfect symmetry of the converter in both phases, the current distribution in each phase is equal. This symmetry ensures that there is no thermal imbalance between the phases, which is a crucial factor in maintaining the efficiency and longevity of the converter. By balancing the current flow evenly across both phases, the system minimizes the risk of overheating or excessive thermal stress, which can otherwise lead to component failure or degraded performance. The absence of thermal imbalance allows for more reliable operation enabling the converter to perform at optimal levels without the need for additional thermal management solutions.

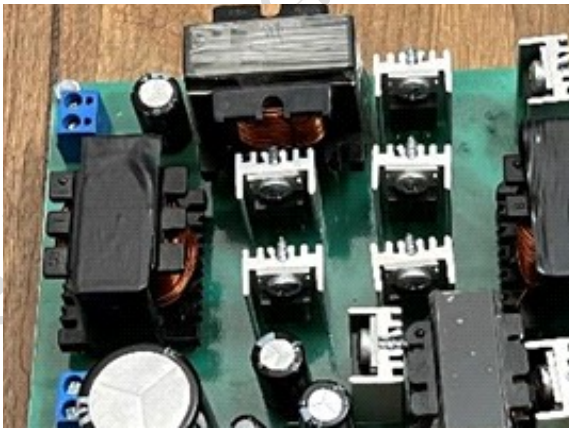


Fig. 6. The implemented converter

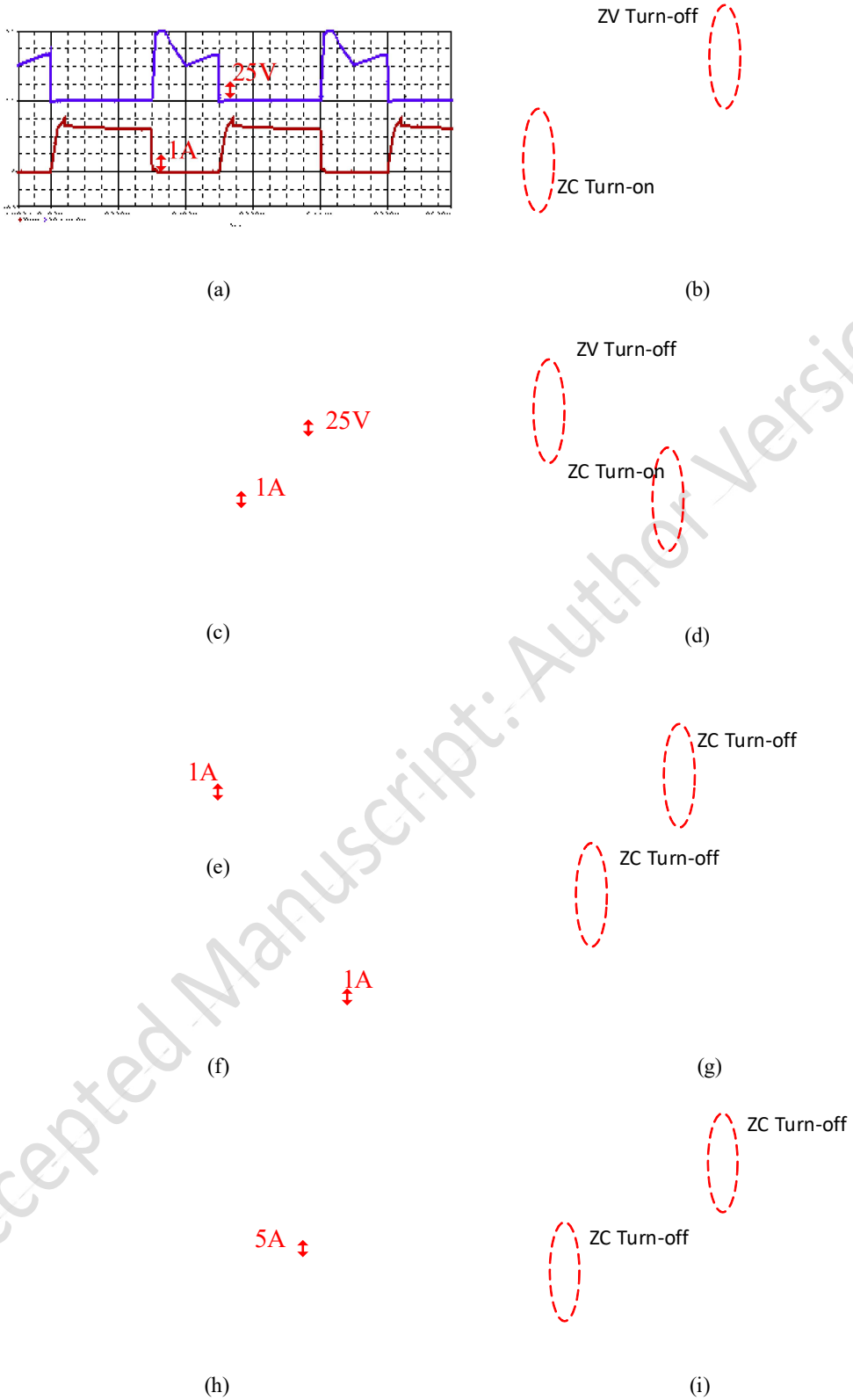


Fig. 7. The simulated and experimental results: (a),(c) simulated waveforms of the drain-source voltage (up) and the current (bottom) in S_1 and S_2 (b) , (d) Experimental waveforms of the drain-source voltage (up) and the current (bottom) in S_1 and S_2 (e) ,(f), (g) current waveforms of diodes Da_1 (bottom) and D_{o1} (up) (h),(i) current waveforms of diodes D_1 (bottom) and D_2 (up)

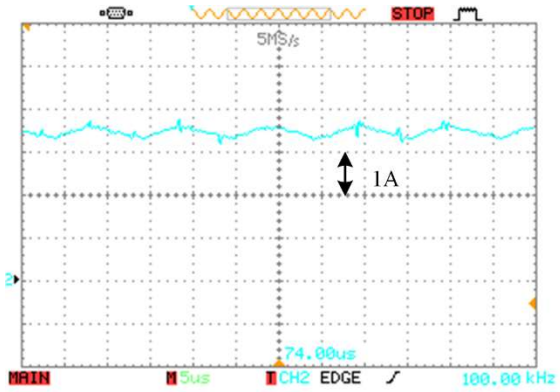


Fig. 8. The practical input current waveform of the proposed converter

1. LOSS ANALYSIS

This section presents the theoretical calculation of the losses in the proposed converter. The analysis considers the loss contributions from the switching devices, diodes, inductors, and capacitors. However, losses associated with ferrite cores are disregarded due to their insignificance. The power loss calculations for the converter components are presented below. Owing to the soft-switching behavior of the converter switches, switching losses are negligible. However, conduction losses as well as capacitive turn-on losses are present and are evaluated using equations (18) and (19)

$$2 * R_{DS}(on) * I^2_{RMS,Si} \quad nrm^*_{60℃} = 2 * 0.19 * 1.46^2 * 1.3 = 1.05W \tag{18}$$

$$2*\frac{1}{2} C_{oss} * V^2_{Si} \quad * f = 780 * 10^{-12} * 98^2 * 10^5 = 0.749\text{W} \tag{19}$$

The diode losses in the converter are primarily determined by the forward voltage drop and the average current flowing through each diode, as expressed in Equation (20).

$$V_{F,D} * \left(I_{av,D_{1,2}} + I_{av,D_{o1,o2}} + I_{av,D_{a1,a2}}\right) = 0.9 * (0.59 + 0.55 + 0.28) = 1.28W \tag{20}$$

The losses in the inductors are caused by the winding resistance, and are directly proportional to the square of the RMS current flowing through them. The resistance of the snubber circuit windings has been neglected due to the very low number of turns. These losses are calculated as follows

$$R_{DC,L11,21} * I^2_{RMS,L_{11,21}} + R_{DC,L12,22} * I^2_{RMS,L_{12,22}} = 0.03*16.44+0.11*3.44=0.87\text{W} \tag{21}$$

The losses due to the equivalent series resistance (ESR) of the converter's electrolytic capacitors are also calculated as below. It should be noted that the losses associated with the snubber capacitors are negligible due to their small capacitance values and polyester type, and are therefore omitted from the analysis.

$$ESR_{C1} * I^2_{RMS,C_1} + ESR_{C2} * I^2_{RMS,C_2} + ESR_{Co} * I^2_{RMS,C_o} = 0.05 * (1.12 + 1.12 + 0.84) = 0.15W \tag{22}$$

Based on the loss analysis under full-load conditions, the total power dissipation is sufficiently low to allow the proposed converter to reach an overall efficiency of 96%. The distribution of these losses among the main components is illustrated in the pie chart shown in Fig. 9.

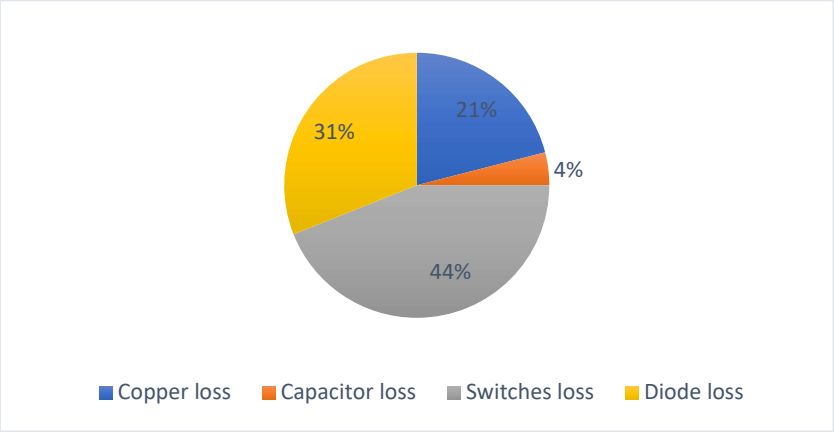


Fig.9. Breakdown loss in the proposed converter

1.1. Comparison of measured efficiency between the proposed converter and its hard-switching counterpart

Fig. 10 illustrates the measured efficiency of the proposed converter in comparison with its hard-switching counterpart (without the auxiliary circuit). As observed, at full load, the proposed converter achieves a 5% improvement in efficiency. It is noteworthy that in the proposed converter, the efficiency does not significantly decrease with reduced power. In contrast, the hard-switching converter exhibits a more pronounced efficiency drop due to the presence of passive clamp circuits. This indicates that the auxiliary circuit in the proposed converter helps maintain high efficiency even under partial load conditions, while the hard-switching counterpart suffers more significant losses as the power level decreases. The efficiency of the proposed converter at full load closely aligns with the theoretical predictions, with a deviation of 0.4% primarily attributed to core losses and unintended oscillations induced by parasitic elements.

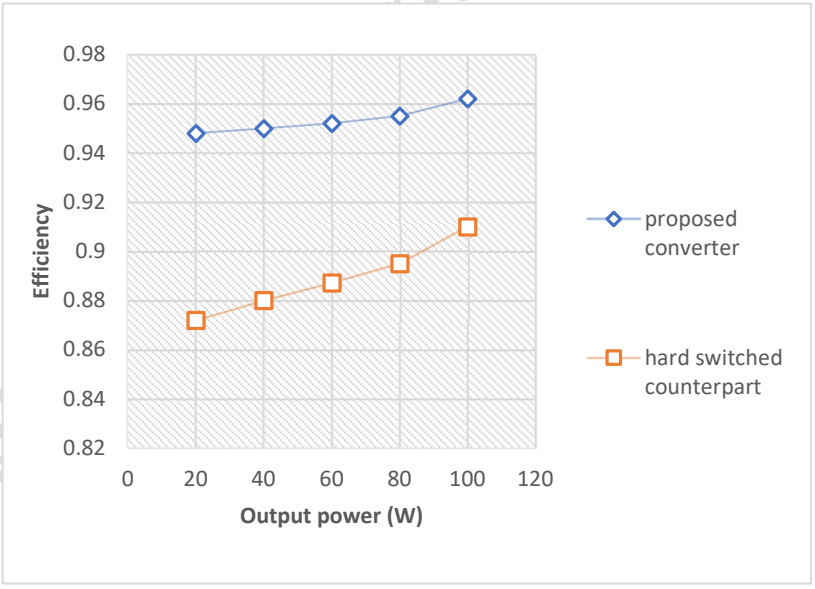


Fig.10. Efficiency comparison of the proposed interleaved step-up converter with its hard-switching counterpart

2. COMPARISON ANALYSIS

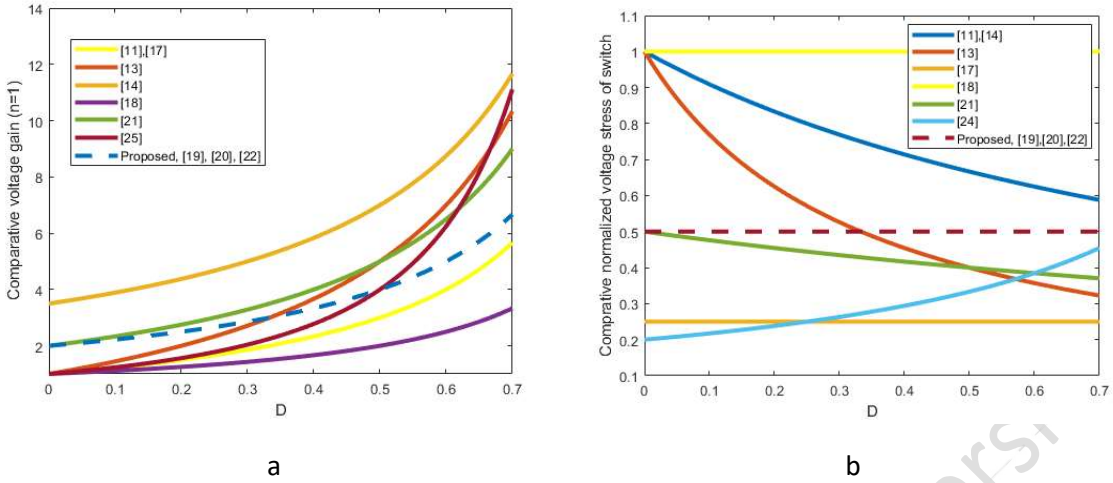
In this section, the proposed converter is analyzed in comparison with previously developed similar converters. Table. 2 presents a comparative evaluation based on voltage gain, switch voltage stress, the number of active and passive components, switching methodology, and common-ground configuration. As indicated in the table, converters [11], [14], [18], and [21] incorporate fewer components than the proposed design. However, converters [11] and [14] exhibit both lower voltage gain and hard switching operation, which leads to reduced efficiency and limits the switching frequency. Converter [18] achieves a voltage gain comparable to that of a conventional boost converter, while converter [21] lacks a common ground between the input and output, significantly restricting its

practical applications. Although converter [17] offers a higher voltage gain than the proposed topology, it employs a greater number of components and operates under hard switching conditions. Converters [19] and [20] feature a similar number of components to the proposed design; however, converter [20] utilizes hard switching and lacks a common-ground structure, while converter [19], despite maintaining a common ground, requires a larger number of switches, complicating control and increasing circulating current within the auxiliary circuit. The converters presented in [22] and [23] utilize a voltage multiplier configuration combined with coupled inductors to improve the voltage gain in interleaved topologies. Nonetheless, due to their hard-switching nature, the switching frequency is inherently constrained, which in turn limits both efficiency and power density. The converters described in [24] and [25] utilize the quadratic conversion principle to achieve elevated voltage gain. While they benefit from high gain and relatively low switch voltage stress, the nonlinear relationship between gain and duty cycle complicates output voltage regulation, especially under load variations. Moreover, their operation under hard-switching conditions results in the typical associated limitations. Additionally, Converter [25] employs four switches, leading to increased cost and circuit complexity. To facilitate a more comprehensive comparison, Figure 11 presents the voltage gain and normalized voltage stress characteristics of the proposed converter alongside those of the converters listed in Table 2.

Table 2. Comparison specification between the proposed converter with other similar converters

Reference	Voltage gain	Switch voltage stress	Component					S.C[2]	C.G[3]
			S	D	C	M.C[1]	Total		
[11]	$\frac{1+D}{1-D}$	$\frac{V_o}{1+D}$	2	4	4	4	14	Hard	Yes
[13]	$\frac{1+3nD}{1-D}$	$\frac{V_o}{1+3nD}$	3	6	4	3	16	Hard	Yes
[14]	$\frac{1+nD}{1-D}$	$\frac{V_o}{1+nD}$	1	2	5	3	11	Hard	No
[17]	$\frac{2n+2}{1-D}$	$\frac{V_o}{2+2n}$	2	7	7	2	18	Hard	Yes
[18]	$\frac{1}{1-D}$	V_o	3	4	2	4	13	Soft	Yes
[19]	$\frac{2n}{1-D}$	$\frac{V_o}{2n}$	4	2	7	4	17	Soft	Yes
[20]	$\frac{2n}{1-D}$	$\frac{V_o}{2n}$	4	6	6	1	17	Hard	No
[21]	$\frac{1+n+D}{1-D}$	$\frac{V_o}{1+n+D}$	4	2	4	3	13	Soft	No
[22]	$\frac{2n}{1-2D}$	$\frac{V_o}{2n}$	2	7	7	2	18	Hard	No
[23]	$\frac{2+3n}{1-D}$	$\frac{V_o}{2+3n}$	2	8	6	2	18	Hard	Yes
[24]	$\frac{A^*}{(1-D)^2}$	$\frac{V_o}{A^*}$	2	5	8	2	17	Hard	Yes
[25]	$\frac{1}{(1-D)^2}$	$\frac{V_o(4-D)}{1-D}$	4	4	3	1	12	Hard	Yes
Proposed	$\frac{1+n}{1-D}$	$\frac{V_o}{1+n}$	2	6	5	4	17	Soft	Yes

1Magnetic core 2Switching condition 3Common ground *A=3+2n-D(3+n-D)



a b

Fig. 11. Comparative graphs of the Proposed Converter: (a) Voltage Gain, (b) Normalized Maximum Voltage Stress of the Switch

3. CONCLUSION

In this paper, an interleaved step-up converter with soft switching is presented, which has several notable features. One of the key features of this converter is zero-current switching of the switches, which helps reduce switching losses. Additionally, the number of auxiliary circuit components in this converter has been minimized, which reduces complexity and costs. Furthermore, no reverse recovery issues are observed in the diodes, thus avoiding common problems such as reverse recovery found in similar circuits. The voltage stress on the switches is also low in this converter, improving the performance and longevity of the switches. The converter is controlled using PWM, which provides high flexibility in controlling voltage and current. In this design, all switches are grounded, reducing electromagnetic interference. Other positive features of this converter include equal current distribution across the phases and thermal balance, which prevent damage to components and enhance the overall system performance. Additionally, the circulating current in the snubber circuit is low, reducing losses and increasing system efficiency. The only significant drawback of this converter is the capacitive turn-on losses in the switches, which may be considered for future optimizations.

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Ethics. The authors declare that the present research work has fulfilled all relevant ethical guidelines required by COPE.

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