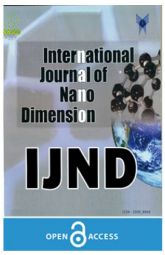


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# Performance analysis of the novel Quad Gate Stacked nano-sheets FinFET device and its application in common source amplifier

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**Original Research**

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**Abstract:**

Stacked Nano-sheets FinFET device has evolved as a viable alternative to FinFET in designing low power circuits. The performance analysis of the novel Quad Gate Stacked Nano-sheets (QG-SNS) FinFET device and its comparison with FinFET and Stacked Nano-sheets devices have been carried out. QG-SNS FinFET device is designed on Cogenda TCAD tool at 30 nm technology node. Device simulation results indicate a steep sub-threshold slope of 26.7 mV/decade, ON current of is $1.0\times10^{-5}$ A, and OFF current of is $9.85\times10^{-14}$ A. The maximum cutoff frequency of 381 GHz is reported. The designed device shows higher early voltage and better device efficiency. Further, the performance-based comparative analysis of common source amplifier circuit designed with QG-SNS FinFET device is done with FinFET based amplifier. Circuit simulations have been performed utilizing the Look up table based Verilog-A model. Amplification of factor 1.93 has been achieved by QG-SNS FinFET based amplifier which is 60.8% better than that achieved by FinFET based amplifier, highlighting the capability of QG-SNS FinFET device for high frequency circuits having input signals of frequency 100 MHz. Average power dissipation and leakage power are reduced by 1.12 and $10^{-6}$ times respectively in QG-SNS FinFET based amplifier.

**Keywords:** Amplification; Common source amplifier; Leakage power; Nano-sheet stacking; OFF current; Quad gate FinFET

## 1. Introduction

FinFETs have been implemented in volume production because of improved Sub-threshold slope (SS), enhanced scalability, superior channel electrostatics and high performance over CMOS technology [1, 2]. Gate-all-around (GAA) Nano-sheet transistor constitutes a potential device to replace traditional FinFET below 7 nm technology node [3–5]. Recently vertically stacked GAA Nano-sheet FETs (NSFETs) have emerged as the perfect replacement for FinFET technology because vertical stacking of sheets allows the drive current to maximize [6, 7].

In [8], P-type horizontally stacked Ge-NSFET fabrication process has been revealed primarily. In [9], the fabrication process of vertically stacked GeSn P-type GAA NSFET having 3 Nano-sheets (NSs) has been illustrated experimentally. The analog performance of NSFETs has been determined by the key attributes: gate length ($L_g$), number of NSs, NS width, work function of metal gate, gate dielectric thickness and channel thickness [10–16]. An inter-bridge channel in-between the NSs of vertically stacked GAA NSFET can be a significant part in enhancing the device's drive current ability [17]. The ballistic current and the drift diffusion current are the two components of the total drain current in NSFETs [18]. Ballistic current varies with NS thickness and width. Drift diffusion current depends on the NS thickness and effective mass of charge carriers in the NS channels. To

improve the drift-diffusion current, a lower $L_g$ is required for NSFETs. One of the other serious concerns in NSFETs is self-heating effect. To reduce the self-heating effects, it is required to select the substrate material properly. In [19], the first stacked Si NSFET with negative capacitance has been revealed. High drive current and steep SS have been offered by negative capacitance in Si NSFET. Hence, it could be outlined that NSFETs have turned up as an antidote to high density memories and integrated circuit applications of the next generation. So NSFETs are required to be explored for superior performance [20].

In [21], the RF performance of the junction-less accumulation-mode bulk FinFETs has been analyzed, considering the effect of the variations of fin shape. Various RF parameters have been calculated for distinct fin shapes to conclude the implementation of designed device in analog applications. In [22], the design and structural impact of the NS transistors have been studied for enhanced analog performance. Several techniques have been explored for better RF applications using NS transistors. In [23], FinFET performance improvement has been done by incorporating the concepts of bottom spacer, dual-material, and ground-plane together. Also, the performance evaluation of the designed device has been done based on the study of analog and electrical parameters. In [24], comprehensive RF performance investigation of GAA stacked NSFET having two NSs channels has been done. Also, the device performance has been evaluated depending upon the results of gate length and NS width variations. In [25], power gating technique based hybrid TFET CMOS has been proposed. This hybrid technique is based on the utilization of minimum number of TFETs. This is done to decrease the leakage current during sleep mode and to enable a temperature variation tolerant sleep mode. In [26], GAAFET having dual metal hetero-dielectric has been proposed. This device alleviates the issue of Drain Induced Barrier Lowering (DIBL). The device performance is also analyzed, and it shows better $I_{ON}/I_{OFF}$ ratio, improved transconductance and early voltage, making it suitable for RF applications.

However, developing the device design options having RF competence will aid in acquiring RF along with logic system on chip to avail the benefit of logic power and performance using GAA NSFET transistors. Most of the previous work reported till date, investigated the performance parameters of GAA NSFET devices for analog and digital applications and have not performed the circuit level implementation for RF applications. In our earlier work [16, 27], QG-SNS FinFET device has been designed at 30 nm technology node. The performance of the designed device has been evaluated considering various Figure of Merit (FOM) related parameters. The device's analysis revealed low leakage current, better ON current with improved sub-threshold slope. The device is also suitable for working at high frequency analog signals.

In this work, analog performance analysis of the designed QG-SNS FinFET device has been done. Also, it has been compared with the existing literature to highlight the device's propensity in RF circuit designing. Subsequently, the device has been applied in the designing of a common source (CS) amplifier circuit and has been compared with the same circuit using BSIM-CMG FinFET model, in the absence of any similar work, to the best of our knowledge. In fact, our QG-SNS FinFET device has been found to perform better for this application than the compared device. Better performance parameters of this device make it suitable for applications like IoT, memories, cyber security, and computer networks for future advancements. The paper is structured as follows: Design parameters and structural attributes of the device designed in [16] are given in section 2. The $I_D$-$V_{GS}$ characteristics and variation of drain current with drain voltage are also given. In section 3, device analog performance is discussed, highlighting important FOM parameters. section 4 outlines the designing procedure for Look up Table (LUT) based Verilog-A model, which will be utilized in the circuit level simulations of the designed device. Simulation results of CS amplifier circuit implemented using the designed device are given in section 5. In this section, performance comparison of QG-SNS FinFET based CS amplifier with BSIM-CMG FinFET based CS amplifier is done. Different parameters affecting the performance of designed amplifier circuit are also highlighted. Conclusion has been elicited in section 6.

## 2. Materials and methods: QG-SNS FinFET device design

In our previous work [16], QG-SNS FinFET device has been calibrated and designed at 30 nm technology node. The designed device has been calibrated with respect to the data available in [28]. Simulations have been conducted on Cogenda TCAD tool [29]. Basic and mobility models along with Drift Diffusion Model (DDM) have been incorporated to carry out the simulations. Band Gap Narrowing Model was also invoked to ensure the simulations accuracy [30]. Recombination of charge carriers was accounted by Shockley-Read-hall (SRH) model [31]. The schematic of designed device is shown in Fig. 1. Table 1 highlights the adopted device design parameters. The device's $I_D$-$V_{GS}$ characteristics are given in Fig. 2.

In our earlier work [16], parametric analysis of the proposed device has been done with variations in the NSs count, work function, drain and source doping concentrations. The designed device gave better results with 3 stacked NSs at work function of 4.73 eV for drain and source doping of 8E18 and 1E20 atoms per $cm^3$. The designed device has shown significant ON current of $1.0 \times 10^{-5}$ A and extremely low OFF current of $9.8 \times 10^{-14}$ A. A steep SS of 26.7 mV/decade is manifested. The variations of $I_D$ with $V_{DS}$ at different values of $V_{GS}$ are given in Fig. 3.

## 3. Analog performance of QG-SNS FinFET

The device analysis must be done in terms of various important parameters to observe the device performance for analog circuits. In our previous paper [16], we have done the performance analysis of the device and compared the results with the devices namely FinFET and Stacked NSs designed in [32]. The analog performance of the device depends on the miller capacitances; gate to drain capacitance ($C_{GD}$), gate to source capacitance ($C_{GS}$) and total gate

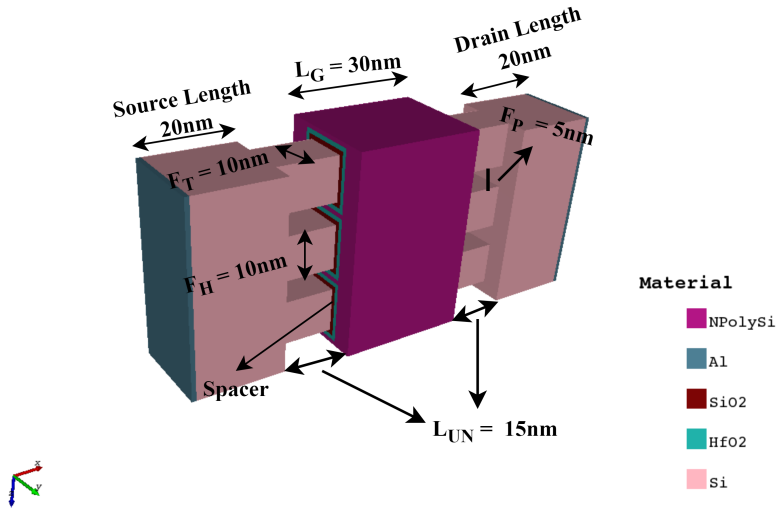


**Figure 1.** 3-D view of QG-SNS FinFET device.

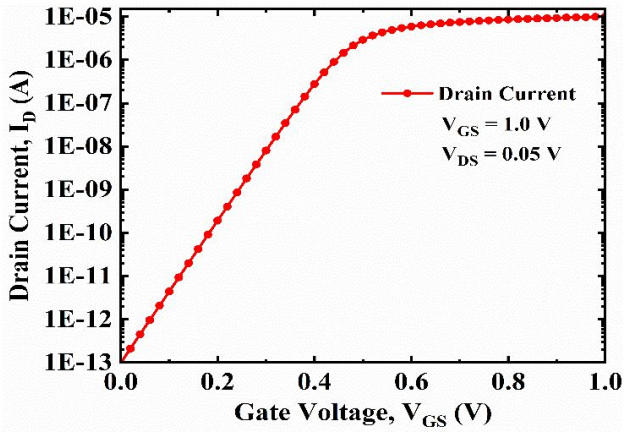


**Figure 2.** $I_D$-$V_{GS}$ plot of QG-SNS FinFET device.

**Table 1.** Device design parameters.

| Parameters | Dimension |
|---|---|
| Gate length | 30 nm |
| Source/Drain length | 20 nm each |
| Equivalent oxide thickness | 1 nm ($HfO_2$, $SiO_2$) |
| Gate underlap (LUN) | 15 nm |
| Fin thickness (FT) | 10 nm |
| Fin height (FH) | 10 nm |
| Fin pitch (FP) | 5 nm |
| Channel doping profile | 1.00E+16 |
| Source/Drain doping profile | 1E20/8E18 |
| Gate work function | 4.73, 4.75 |
| Gate dielectric Constant | 25 |
| Mobility model | Lombardi |
| Spacer | $SiO_2$ |
| Supply voltage | 1 V |

capacitance ($C_{GG}$) where $C_{GG} = C_{GD} + C_{GS}$. These capacitances are extracted during ac simulations of the device. The $C_{GG}$ values are extracted by ramping the $V_{GS}$ from 0 to 0.8 V and by applying a source of frequency 1 MHz against the gate terminal and the same is shown in Fig. 4. The $C_{GD}$, $C_{GS}$ and $C_{GG}$ of the designed device has been found as $1.72\times10^{-17}$ F, $4.33\times10^{-18}$ F, and $2.15\times10^{-17}$ F respectively at $V_{GS} = 0.8$ V. The transconductance ($G_m$) that evaluates the change in $I_D$ with varying $V_{GS}$ at a certain value of $V_{DS}$ [33] has been found to be $3.8\times10^{-5}$ Siemens (S). The unity gain frequency ($F_T$) of a device depends on miller capacitances and $G_m$ [34]. $F_T$ is also known as device's cut off frequency and is expressed as in Equation 1. To attain high $F_T$, the $G_m$ of the device must be high and $C_{GG}$ must be low.

$$F_T = \frac{G_m}{2\Pi(C_{GS} + C_{GD})} \tag{1}$$

The maximum $F_T$ for QG-SNS FinFET calculated using the Equation 1 is found out to be 381 GHz at a $V_{GS}$ value of 0.48 V which is 1.73 and 1.58 times higher than the maximum $F_T$ in [32] for FinFET and Stacked NSs devices respectively. The higher value of $F_T$ means the device can be put through high frequency signal [34] and can exhibit improved performance. The $F_T$ variations with $V_{GS}$ are shown in Fig. 5.

Some performance related parameters other than those reported in [16] have been analyzed in this paper. These parameters are related to the FOM. Device performance has been analyzed and compared with the results of FinFET and Stacked NSs in [32] at 30 nm technology node. Table 2 highlights the comparison.

### 3.1 Output conductance

Output conductance ($G_D$) is defined as drain current variations with varying $V_{DS}$ at a given value of $V_{GS}$ [35]. Here $V_{DS}$ is varied from 0 to 1 V and $V_{GS}$ is kept constant at a value of 1 V. The $G_D$ has been calculated using the Equation 2 and it came out to be $1.24\times10^{-4}$S which is 1.85 and 1.83

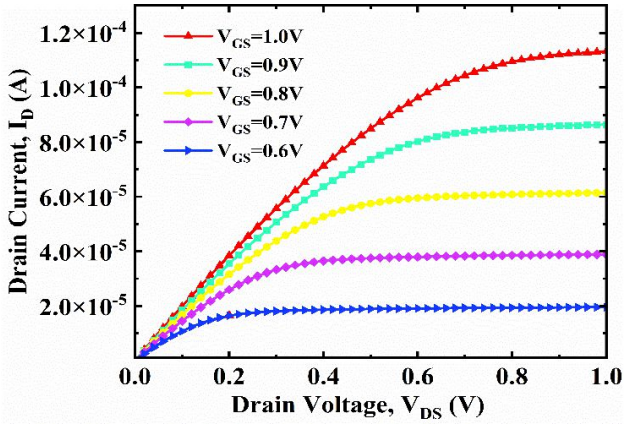


**Figure 3.** $I_D$-$V_{DS}$ with varying $V_{GS}$.

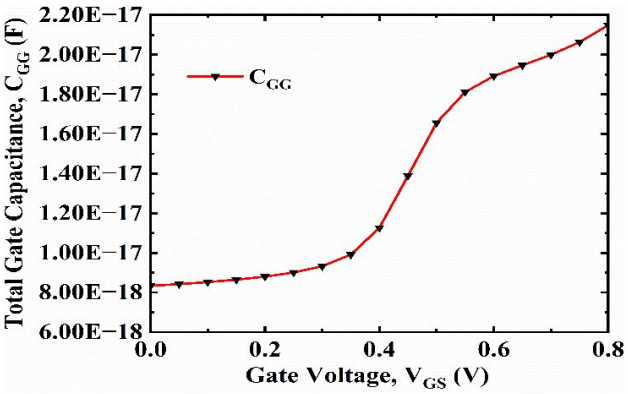


**Figure 4.** Total Gate Capacitance curve with varying $V_{GS}$.

times less than that of FinFET and Stacked NSs devices [32] respectively. The $G_D$ variations with $V_{DS}$ are given in Fig. 6. The control of drain voltage on the channel of the device is restrained as the $G_D$ value reduces [35]. But at the same time, lower $G_D$ ensures higher early voltage.

$$G_D = \frac{\partial I_D}{\partial V_{DS}} \tag{2}$$

### 3.2 Early voltage

Early voltage ($V_{EA}$) is the ratio of $I_D$ and $G_D$ at a constant value of $V_{GS}$ for varying $V_{DS}$ [35]. It is given by Equation 3. As the device shifts from sub-threshold region to saturation region, the value of $V_{EA}$ increases. It has been seen that the higher value of $V_{EA}$ is because of the lower value of $G_D$. The variations in early voltage with $V_{DS}$ are shown in Fig. 6. A peak early voltage of value 12.14 V is seen at $V_{DS} = 0.98$ V.

$$V_{EA} = \frac{I_D}{G_D} \tag{3}$$

### 3.3 Transconductance gain factor

One of the important FOM is Transconductance Gain Factor ($TGF$), which is used to discover the efficiency of a device. Hence $TGF$ is also called device efficiency and is given as the ratio of $G_m$ and $I_D$ [35] as shown by Equation 4.

$$TGF = \frac{G_m}{I_D} \tag{4}$$

The high value of $TGF$ signifies superior input drivability. Correspondingly, power dissipation will be less in circuits with capacitive load [36]. The $TGF$ curve with $V_{GS}$ is given in Fig. 7. The designed QG-SNS FinFET shows maximum efficiency in sub-threshold region. A significant improvement in $TGF$ is seen in the moderate inversion region with comparable amount in strong inversion region. The efficiency of the proposed device is 56 $V^{-1}$ at $I_D$ value of $10^{-10}$ A which is better than FinFET and Stacked NSs devices with efficiency of 3.5 $V^{-1}$ and 10 $V^{-1}$ respectively.

## 4. Device to circuit modeling

Many researchers have used LUT dependent Verilog-A model for building FinFET based circuits in SPICE. This approach is valid and has been used for many years for devices whose compact models are still required to be devised. There is no availability of validated compact model for NSs FinFET device to carry out SPICE simulations. Verilog-A model employs capacitance and transfer characteristics of NSs FinFET device. The flow of device to circuit modeling is given in Fig. 8. Three tables namely $C_{GS}$.tbl, $C_{GD}$.tbl and $I_DV_G$.tbl are extracted through device simulations. These extracted tables are called up by Verilog-A code used to conduct the analysis of QG-SNS FinFET based common source amplifier circuit in Symspice tool.

It is evident that the resistances and parasitic capacitance are not incorporated in Fig. 8. So, these can be incorporated within the SPICE netlist during the circuit level simulations [37]. Both transient and DC characteristics of QG-SNS FinFET device can be captured accurately by Verilog-A based

**Table 2.** RF performance parameters.

| RF parameters | $L_g$ (nm) | $I_{ON}/I_{OFF}$ ratio ($10^6$) | $C_{GS}$ (F) | $C_{GD}$ (F) | $C_{GG}$ (F) | $G_m$ (S) | $F_T$ (GHz) | $TGF$ ($V^{-1}$) | $G_D$ (S) | $R_O$ (kΩ) |
|---|---|---|---|---|---|---|---|---|---|---|
| FinFET [32] | 30 | 1 | $1.5\times10^{-15}$ | $1.2\times10^{-15}$ | $2.7\times10^{-15}$ | $3.4\times10^{-3}$ | 220 | 3.5 | $2.2\times10^{-4}$ | 4.5 |
| Stacked NSs [32] | 30 | 10 | $1.9\times10^{-15}$ | $1.4\times10^{-15}$ | $3.4\times10^{-15}$ | $5.0\times10^{-3}$ | 240 | 10 | $2.3\times10^{-4}$ | 4.3 |
| QG-SNS FinFET | 30 | 87.3 | $4.33\times10^{-18}$ | $1.72\times10^{-17}$ | $2.15\times10^{-17}$ | $3.8\times10^{-5}$ | 381 | 56 | $1.27\times10^{-4}$ | 7.8 |

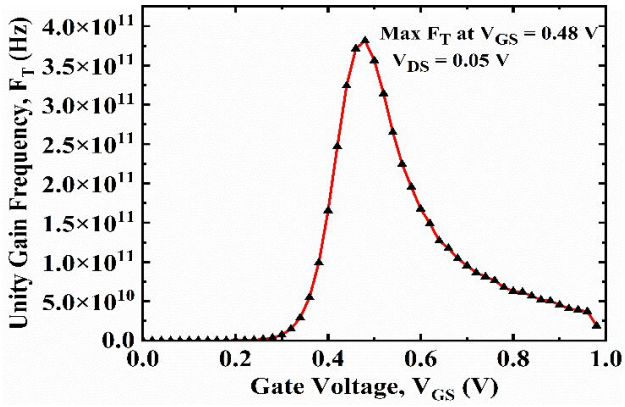


**Figure 5.** Cut off frequency curve.

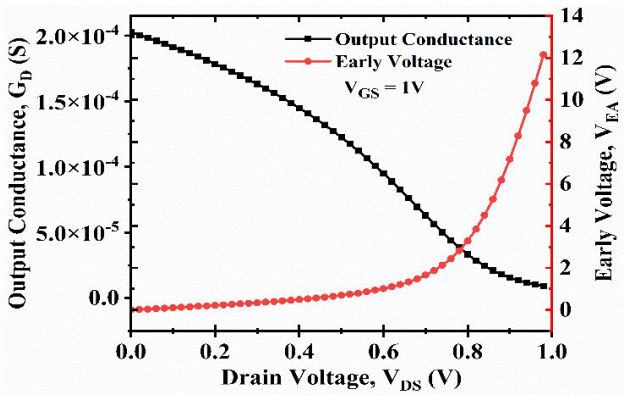


**Figure 6.** Variation in output conductance and early voltage with $V_{DS}$ at $V_{GS} = 1.0$ V.

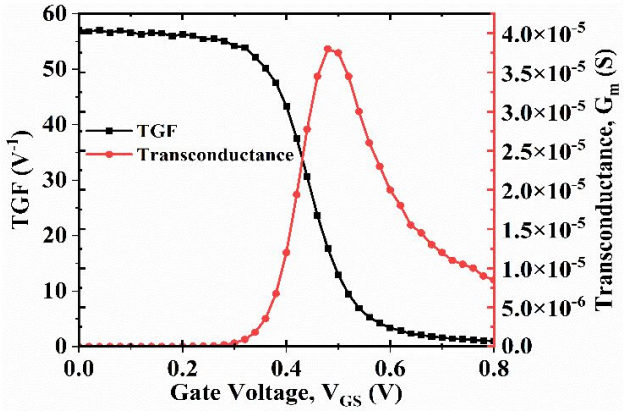


**Figure 7.** Device efficiency curve of QG-SNS FinFET.

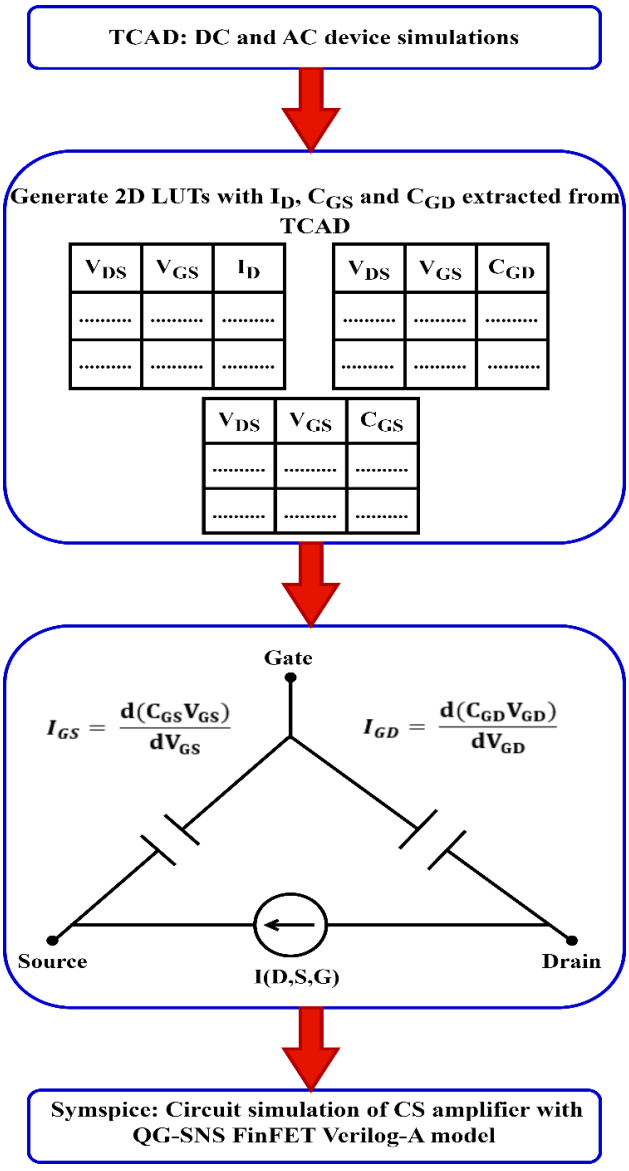


**Figure 8.** Flow chart for device to circuit modeling.

model approach. The device characteristics of transient analysis are derived by the source charge ($Q_S = C_{GS}V_{GS}$), drain charge ($Q_D = C_{GD}V_{GD}$) and potential at terminals ($V_{GS}$ and $V_{GD}$).

DC analysis uses the LUT variables mentioned in $I_DV_G$.tbl file to calculate the device's DC characteristics. The simulations of the optimized and validated QG-SNS FinFET device have been done on Cogenda Visual Fab tool. After that a python script has been accustomed for excerpting $C_{GS}$.tbl, $C_{GD}$.tbl and $I_DV_G$.tbl tables which have been used to design Verilog-A model of the designed device. The values to $I_D$, $C_{GS}$ and $C_{GD}$ have been given from the LUTs in .tbl according to the terminal voltages.

## 5. Results and discussion: common source amplifier circuit

This work focuses on the application of the designed device for analog circuit implementation. A resistive load CS amplifier circuit composed of QG-SNS FinFET device is shown in Fig. 9. Transient analysis included a sinusoidal input signal, $V_{ac}$ of frequency 100 MHz applied at gate terminal with 0.2 V peak to peak amplitude, which is required to be amplified. $V_{Bias}$ is a DC offset voltage applied at the input signal and is taken as 0.7 V. Resistance, R1 of 100 Ω is connected in-between the gate terminal and the applied AC signal. Also, resistance, R2 of 15 kΩ is connected in-between the supply voltage and the drain terminal. R3 and C2 are the load resistance and capacitance of values 1000 kΩ and 1 fF respectively. The removal of DC components out of the output signal is done using a capacitance (C1) of 1 μF.

The device's gain is expressed as in Equation 5. $R_O$ is the output resistance of the device and is given as reciprocal of $G_D$. $G_m$ is transconductance. To achieve high amplification in an amplifier, both $G_m$ and $R_O$ values are required to be on the higher side [33]. The voltage transfer characteristics of the CS amplifier circuit are depicted by Fig. 10. It is evident that the steep switching characteristics are basically because of the output resistance ($R_O$) and transconductance of the device.

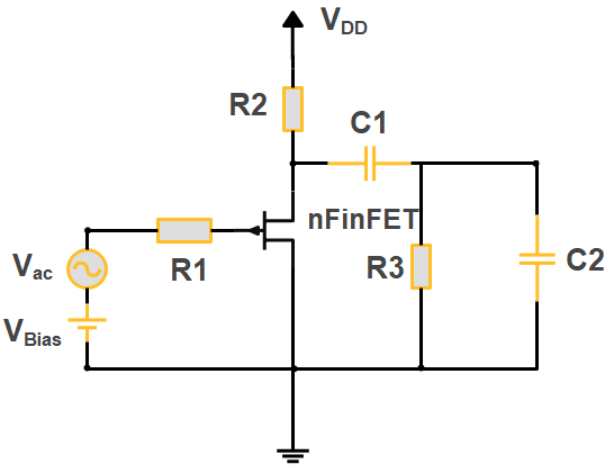


**Figure 9.** CS amplifier circuit design.

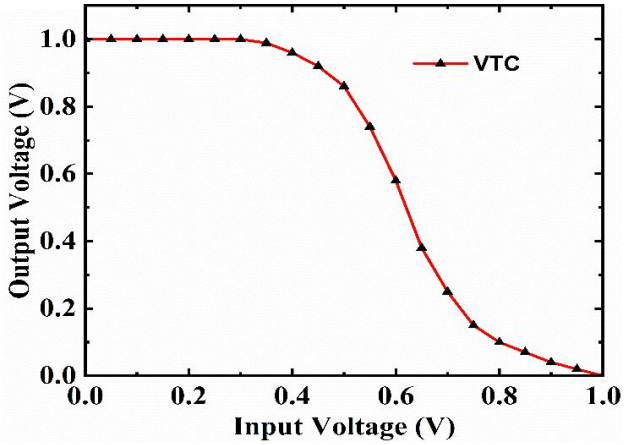


**Figure 10.** VTC characteristics plot.

$$A_v = G_m R_O \tag{5}$$

To compare the results, CS amplifier has been designed using BSIM-CMG model file of n-type FinFET device at 30 nm technology node [38]. Performance evaluation of QG-SNS FinFET based CS amplifier is done by comparing it with above mentioned FinFET based CS amplifier circuit. Fig. 11 shows the transient analysis results of both QG-SNS FinFET and FinFET based CS amplifier circuits. It is evident from Fig. 11 that an excellent amplification of 1.93 times is attained by CS amplifier circuit with the designed QG-SNS FinFET device. FinFET based CS amplifier circuit gives amplification of 1.2 times. Hence, QG-SNS FinFET device gives better amplification and can be used to design an amplifier which is among the several prime elements of analog circuits.

The gain variations with respect to input signal frequency variations are given in Fig. 12. The results reveal that the CS amplifier designed using QG-SNS FinFET device can operate at a wide frequency range of inputs from 100 kHz to 0.1 GHz with amplification of factor 1.93. At frequencies beyond 0.1 GHz, the gain started degrading.

The analysis is done based on the amplification, leakage

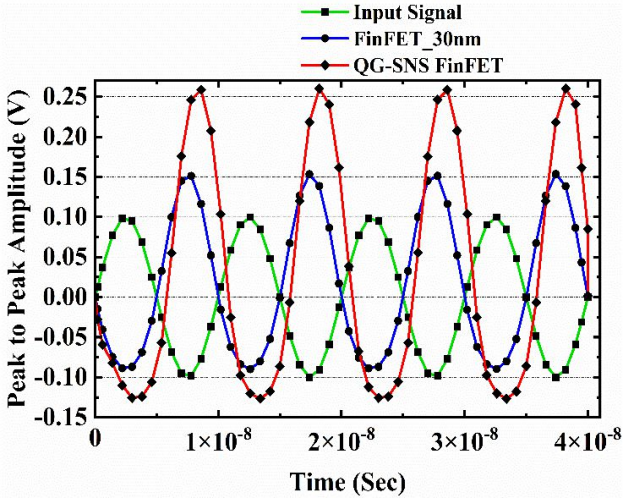


**Figure 11.** Transient analysis at input signal of frequency 100 MHz.

**Table 3.** Performance evaluation of CS amplifier.

| CS amplifier circuit | Load (R3) | Gain | Peak power (µWatt) | Average power (µWatt) | Leakage power |
|---|---|---|---|---|---|
| QG-SNS FinFET | 1000 kΩ | 1.93 times | 39.6 | 33.9 | 0.14 pWatt |
| FinFET | 1000 kΩ | 1.2 times | 41.3 | 38 | 7.58 µWatt |

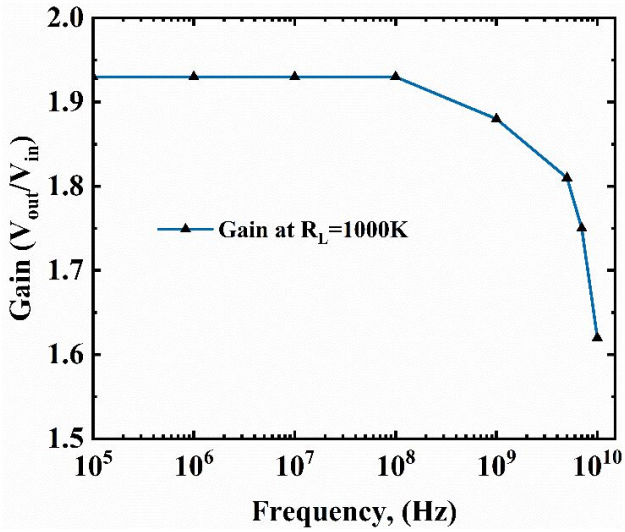


**Figure 12.** Variation in gain with frequency of input signal.

power, peak power, and average power dissipation. For better performance, the designed circuit must show higher amplification and lower power dissipation. The average and peak power of the circuit are calculated by applying an ac input signal of 100 MHz frequency at the gate terminal. QG-SNS FinFET based CS amplifier circuit shows average power dissipation of 33.9 µWatt which is less than that of FinFET based circuit. The circuit is switching at very high frequency hence its average power consumption will be more. The peak power of QG-SNS FinFET based circuit is also less. The dc source ($V_{Bias}$) is removed to calculate the circuit leakage power in the presence of an ac input signal. The circuit level simulations reveal that the QG-SNS FinFET based CS amplifier circuit dissipates very less leakage power of 0.12 pWatt and it is about $10^{-6}$ order less when compared to FinFET based counterpart. This is quite apparent from the fact that the OFF current in the designed QG-SNS FinFET device is of order $10^{-14}$ and very less when compared to what flows in FinFET with similar device dimensions. This shows its dominance over FinFET to design power effective amplifier circuits. Performance comparability of designed CS amplifier circuit using QG-SNS FinFET with FinFET device is shown in Table 3.

The power sustaining behavior of QG-SNS FinFET device is significant for IoT applications which are predominantly battery driven. Although the QG-SNS FinFET based amplifier circuit exhibits good power saving and amplification features, it is sensitive to certain parameters like load resistance (R3) and DC offset voltage. The operating point of amplifier voltage will shift due to change in these parameters. The change in temperature can lead to load resistance fluctuations which may severely affect the amplification factor of the amplifier. Hence to tackle these issues and to ensure better amplification, different strategies must be carefully implemented by the designers at the circuit level.

## 6. Conclusion

A detailed investigation of CS amplifier circuit designed using QG-SNS FinFET device has been carried out. Simulation results reveal that exceptional performance has been exhibited by the QG-SNS FinFET device in the designing of analog application circuits. The device is suitable for designing high performance and low power circuits because the device has steep sub-threshold slope, low OFF current and high ON current. Also, the $C_{GS}$ and $C_{GD}$ values are very low. The cutoff frequency of maximum 381 GHz is obtained at $V_{GS}$ value of 0.48 V. This shows that high frequency input signals can be subjected to gate terminal. The device efficiency of 56 $V^{-1}$ has been achieved. The applied AC signal of 100 MHz gets amplified up to 1.93 times proving its capability for better amplification at high frequency. Leakage power reduction of order $10^{-6}$ in comparison to BSIM-CMG FinFET based CS amplifier circuit shows the device ability in designing low power VLSI circuits.

**Authors Contributions**
All authors have contributed equally to prepare the paper.

**Availability of Data and Materials**
The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Conflict of Interests**
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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