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Design of wide dynamic range MOS current mirror using nano dimension MOS field effect transistor

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Abstract:

A nanoscale metal oxide semiconductor field effect transistor based current mirror circuit operating in a sub volt supply for low power analog applications has been proposed in this paper. Current mirror is a fundamental block of current-mode circuits. In the proposed research, current mirror uses a level-shifted folded flipped voltage follower cell for class AB mode of operation. Usually at nano meter scale, the conventional architecture performance especially for analog gets deteriorates, so to meet the goal proposed design incorporates locally generated feedback & level shifter approach. It also shows improved wide current dynamic range with the use of folding transistors. The current mirroring is performed using folded MOS transistors along with feedback which increases the current mirroring range, results in low input resistance in megahertz range bandwidth. For improvement in output resistance, the architecture uses regulated cascode along with super transistor approach. The performance of the proposed current mirror has been validated small signal analysis and their simulations and corner analysis on Cadence. As observed, the current mirroring is performed with minimum error to 2 milli amperes consuming headroom of 0.14 volt. The input & output resistance is calculated as 1.35 ohm & 2.11 giga ohms respectively. The proposed current mirror is designed in 180 nano meter technology & operates at $\pm$0.5 volt.

Keywords: Dynamic range; Feedback; Input resistance; Output resistance; Super transistor

1. Introduction

With the advent of low power battery operated portable devices; the CMOS has gained the potential interest due to design flexibility & the scaling approach to meet the requirements [1]. In the current scenario, there is a great challenge with IC industries in context to the scaling down of MOS devices as the maximum limits have been almost reached. The performance has been sacrificed in nano scale applications. Moreover, with reduced dimensions in nano meter, the required supply voltage to operate the MOS devices also gets reduced [2–6]. However, the supply scaling factor is not the same as the device scaling factor, i.e. supply voltage scaling is not in proportional to device scaling. So, to achieve satisfactory performance at low supply, low voltage circuit design approaches have been reported in the literature. Such an approach can be applied at MOS structure where the input is processed not in a conventional way & such is referred as non-conventional approach [7–9]. Alternatively, the approach applied at design level instead of MOS structure where local feedback like concepts is used & is referred to as low voltage circuit design approach [10–12]. In this paper, based on the latter approach one of the fundamental analog blocks, current mirror is proposed designed using nano scale MOS devices. Current mirror is one of key block used in current mode circuits. It has a wide variety of uses right from biasing the circuits to active loading in amplifiers.

Some high-performance current mirrors designed in 180 nano meter technology based on non-conventional MOS device can be found in [13–16]. In such an approach, the gate terminal is used to bias the device in the required operating region whereas the signal is processed through auxiliary input. This way the threshold voltage hurdle is removed from the signal path. However, such an approach requires special fabrication steps. In the other approach mentioned, low voltage cells are being used among which one of the most frequently used in recent research is flipped voltage

follower [17]. It is a voltage follower cell which includes local feedback in shunt configuration. This causes low impedance at the output terminal which is one of the requirements of a current mirror. The ideal characteristic includes wide dynamic range, large bandwidth, low input & high output resistance. Using FVF's output as an input of current mirror accommodates one of its desired characteristics, i.e. low input resistance. Such type of current mirrors can be found in [18–21] where emphasis has been kept on resistance part. As per literature survey, the input resistance achieved ranges in ohms & even some reported below an ohm however they were at the cost of increased complexity & additional sources [22–25]. In the proposed current mirror, the feedback approach is used which scales down the input resistance around one ohm & also improves the current mirror dynamic range. The other parameters like output resistance range in giga ohms & also offer large bandwidth with robust performance.

The structure of the paper is outlined as follows: Section 2 introduces the materials & methods followed to design the current mirror which also includes the detailed description of proposed work along with its small signal analysis. Section 3 discusses the results & discussion, and the paper concludes in Section 4.

2. Material and Methods

Fig. 1(a) is the proposed current mirror design that employs a modified FVF cell for high-precision current replication that consists of a level shifter MOS transistor (M_5) to enhance the input/output voltage swing of the FVF cell and a folding MOS transistor (M_4) to enhance the performance. In the modified FVF cell, the M_5 transistor is connected in the feedback path between the nodes 'n3' and 'n6'. A constant current source, I_{b6}, bias the M_5 transistor, which is realized using a diode-connected MOS transistor, M_6. The M_5 transistor acts as a DC level shifter, enhancing the input/output voltage swing of the modified FVF cell. The current source I_{b1} provides the constant bias current in the transistor M_1. The PMOS-based folding transistor M_4 is driven through the drain of M_2 providing the alternative path for sourcing current.

The transistor M_3 is connected between the node 'n2' and 'n3' to generate voltage drop V_b providing the complementary voltage variations at the gate terminals of transistors M_4 and M_5. The dc voltage (V_c) is given at the gate of transistor M_2, and the output voltage is drawn from the drain terminal of M_1 MOS transistor of the modified FVF cell. Thus, the modified FVF cell shows low output resistance. Therefore, in the proposed current mirror, the drain of transistor M_1 acts as an input node.

In the proposed current mirror architecture, when the input current is fed at the input node (drain of M_1), it converts the gate to source voltage (V_{GS}) of M_1. The drain current as sum of bias current (I_{b1}) and input current (I_{in}) flowing through transistor M_1. Since transistors M_1 and M_7 are perfectly matched, the same current is flowing through transistor M_7. The output stage of the proposed current mirror uses regulated cascode where the output transistor M_8 is stacked on the top of M_7 forming the cascode configuration. The feedback transistor M_{11} is isolated from the output voltage variation and ensures that the voltage drop across M_8 remains constant. To further increase the output resistance value, the output is driven by the locally generated feedback formed by M_8, M_9, and M_{10} along with DC current sources as shown in fig. 1(b). This feedback network increases the output resistance by a factor of $(g_m r_o)^2$. The drain terminal of MOS transistor M_8 acts as the output node of the current mirror.

2.1 Small signal analysis of input resistance

For the calculation of input resistance (R_{in}), a voltage source (V_x) is connected at the input (drain of MOS transistor M_1) which supplies current (I_x) as illustrated in fig. 2.

By applying KCL at node 'n3'and assuming $g_m r_o \gg 1$, we get

$$V_3 = g_{m3}(r_{o3} \parallel R_1)V_2 \tag{1}$$

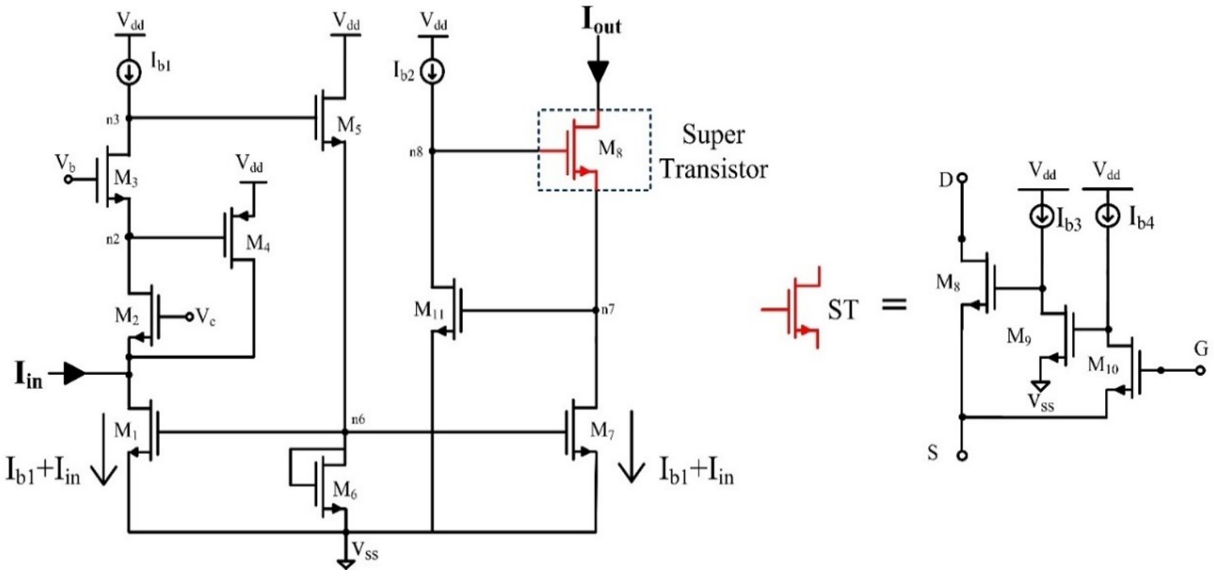

Figure 1. (a) Proposed current mirror; and (b) super transistor.

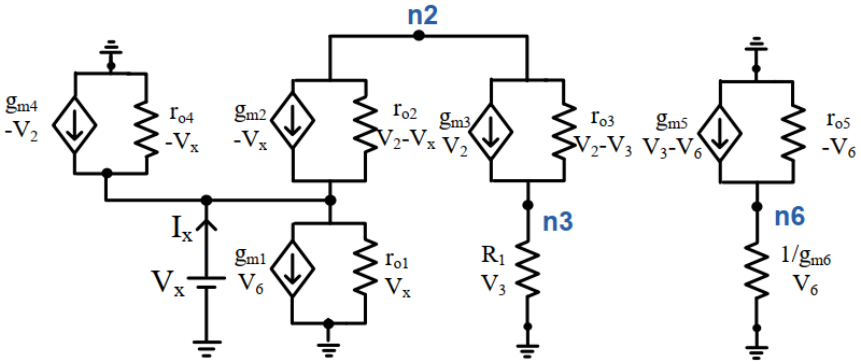

Figure 2. Small-signal equivalent model to calculate input resistance.

Apply KCL at node 'n2' and simplified expression can be written as

$$\frac{(V_2 - V_3)}{r_{o3}} + g_{m3}V_2 = \frac{(V_2 - V_X)}{r_{o2}} - g_{m2}V_X \tag{2}$$

$$V_2 = g_{m2}r_{o2}V_X \tag{3}$$

By applying KCL at node 'n6', we get

$$V_6 = \frac{g_{m5}}{g_{m5} + g_{m6}}V_3 \tag{4}$$

Assume $R_1 = \infty$, as current source and substitute the value of V_3 , voltage V_6 can be written as

$$V_6 = \frac{g_{m5}}{g_{m5} + g_{m6}}(g_{m2}r_{o2})(g_{m3}r_{o3})V_X \tag{5}$$

Apply KCL at input node, we get

$$I_X = \left(\frac{V_X}{r_{o1} \parallel r_{o4}} + g_{m2}V_X\right) + g_{m1}V_6 + g_{m4}V_2 - \frac{V_2}{r_{o2}} \tag{6}$$

Substituting V_2, V_6 , and assume $r_{o1} \ll r_{o4}$ the Input resistance (R_{in}) is expressed as

$$\begin{aligned} I_X = &\left(\frac{V_X}{r_{o1} \parallel r_{o4}} + g_{m2}V_X\right) \\ &+ g_{m1}\frac{g_{m5}}{g_{m5} + g_{m6}}(g_{m2}r_{o2})(g_{m3}r_{o3})V_X \\ &+ g_{m4}g_{m2}r_{o2}V_X - \frac{g_{m2}r_{o2}V_X}{r_{o2}} \end{aligned} \tag{7}$$

$$R_{in} = \frac{V_X}{I_X} = \frac{(g_{m5} + g_{m6})}{(g_{m2}r_{o2})(g_{m1}g_{m5}g_{m3}r_{o3} + g_{m4}(g_{m5} + g_{m6}))} \tag{8}$$

2.2 Small signal analysis of output resistance

For the calculation of output resistance (*R*out), a voltage source (V_x) is connected at the output (drain of transistor M_8) which supplies current (I_x) as illustrated in fig. 3. By applying KCL at node 'n8', 'n9', and 'n11', we get

$$V_9 = -\frac{V_8}{g_{m9}r_{o9} \parallel R_3} \tag{9}$$

$$V_7 = -\frac{V_9}{g_{m10}r_{o10} \parallel R_4} \tag{10}$$

$$V_7 = -\frac{V_8}{g_{m11}r_{o11} \parallel R_2} \tag{11}$$

By applying KCL at node 'n7'

$$I_X = \frac{V_7}{r_{o7}} + g_{m10}V_7 + \frac{V_9}{r_{o10}} \tag{12}$$

Substitute V_9 and assume output resistance of the current source is infinite, the simplified equation can be shown in Eq. 14

$$I_X = \frac{V_7}{r_{o7}} + g_{m10}V_7 - \frac{(g_{m10}r_{o10})V_7}{r_{o10}} \tag{13}$$

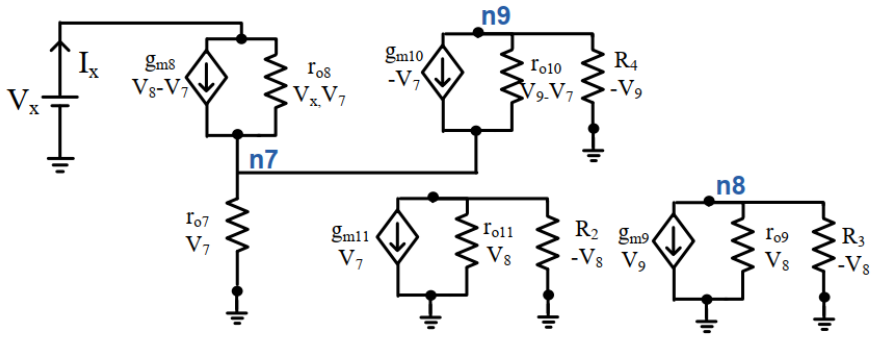

Figure 3. Small-signal equivalent model to calculate output resistance.

$$V_7 = I_X r_{o7} \tag{14}$$

By applying KCL at output node and substituting V_7 and V_8, the output resistance (Rout) is expressed as

$$I_X = g_{m8}(V_8 - V_7) + \frac{V_X - V_7}{r_{o8}} \tag{15}$$

$$R_{out} = \frac{V_X}{I_X} = r_{o8} + r_{o7}(g_{m8} r_{o8})(g_{m11} r_{o11}) + r_{o7}(g_{m8} r_{o8}) \tag{16}$$

3. Results and discussion

The proposed current mirror is designed in 180 nm CMOS technology and simulations have been performed in the Cadence tool. The aspect ratio of the proposed current mirrors is listed in Table 1.

In fig. 4, the DC characteristics of the proposed current mirror is shown which indicates that the output current accurately mirrors the input current across a broad range, 2 milli amperes. The current tracking error is shown in fig. 5. The DC error in the proposed current is obtained as 2.1%. The I-V characteristic of the proposed current mirror shown in fig. 6, clearly achieves a wide operating range to 2 milli amperes consuming minimum output compliance voltage. The gain versus frequency plot of the proposed current mirror is shown in fig. 8.

The proposed current mirror offers a low value of input resistance of 1.35 ohm as shown in fig. 8 whereas a high output resistance of 2.21 giga ohm is achieved through the implementation of a regulated cascode output stage, as depicted in fig. 9. The input resistance and output resistance are shown in frequency domain and their value is measured at low frequency since at high frequency the parasitic capacitances turn on.

Variations in temperature, process, and supply voltage can impact the biasing conditions. Therefore, corner analysis is conducted at different process corners (TT, FNSP, SNFP, SS, and FF) to confirm the robustness of the biasing conditions of the proposed current mirror. Table 2 presents various electrical parameters at these process corners, demonstrating that the proposed current mirror operates within an acceptable range across all corners.

The comparison between reported structures of the current mirror and proposed work is made in Table 3. It is observed from the table that the proposed current mirror offers a wide current mirroring range with low power dissipation compared to all the reported current mirrors. The current tracking error of reported current mirrors is lower than the proposed current mirror.

The proposed circuit overcomes the limitations of existing current mirrors and offers low input resistance, large current mirroring range with high accuracy, wide bandwidth, and high output resistance.

Table 1. Aspect ratio of MOS transistor used in proposed current mirror.

MOS Transistors	W [nm]	L [nm]
M_1-M_3, $M_{7,8,9}$	3000	440
M_4, M_6, M_9	240	240
M_5	2000	440
M_{11}	1000	1000
Supply = ±0.5 V, I_{b1}, I_{b4} = 30 µA, I_{b2} = 500 nA, I_{b3} = 15 µA		

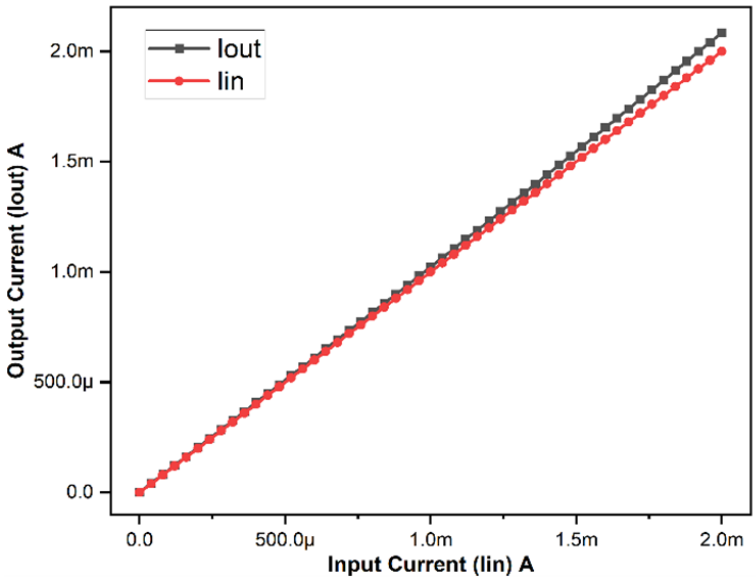

Figure 4. Output current vs. input current transfer characteristics.

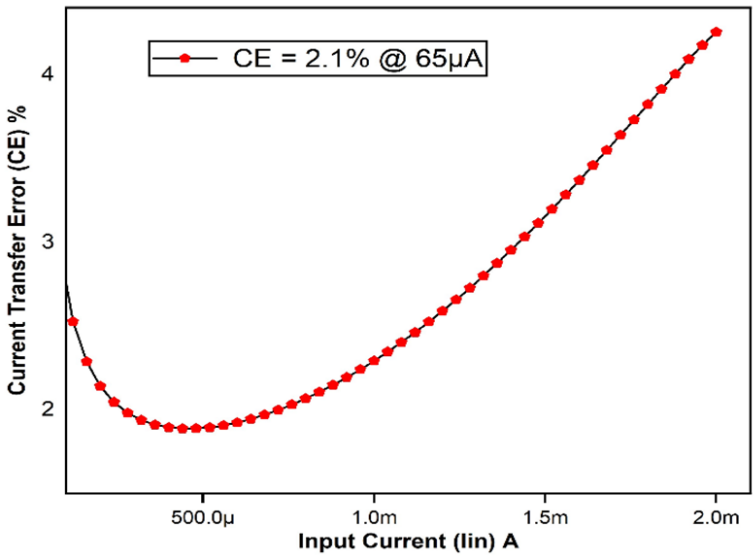

Figure 5. current transfer error.

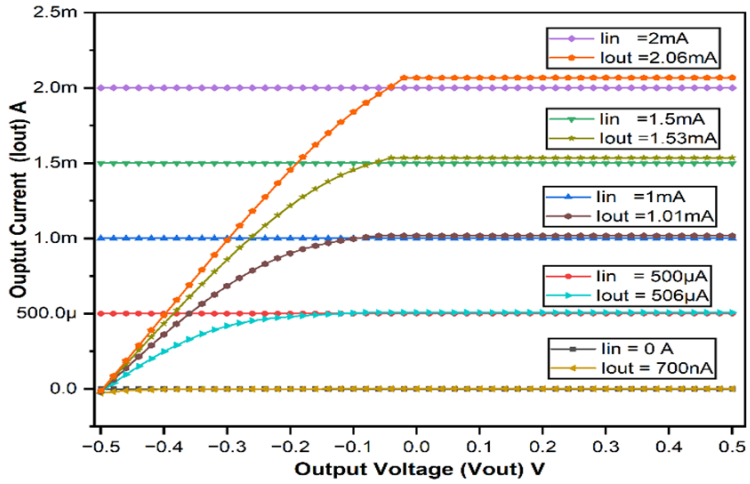

Figure 6. I-V. characteristics at the output node.

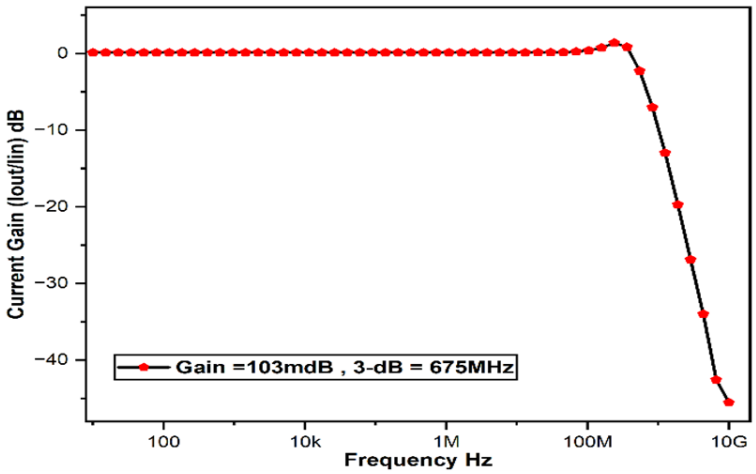

Figure 7. Frequency response.

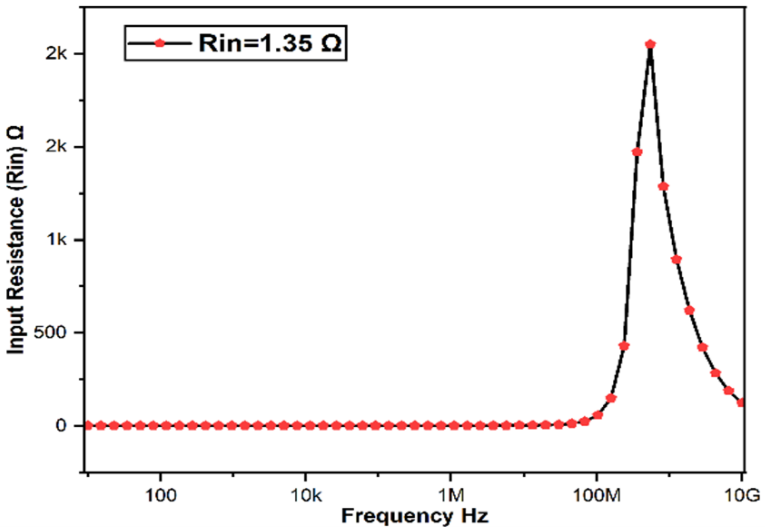

Figure 8. Input resistance (Rin) vs frequency plot.

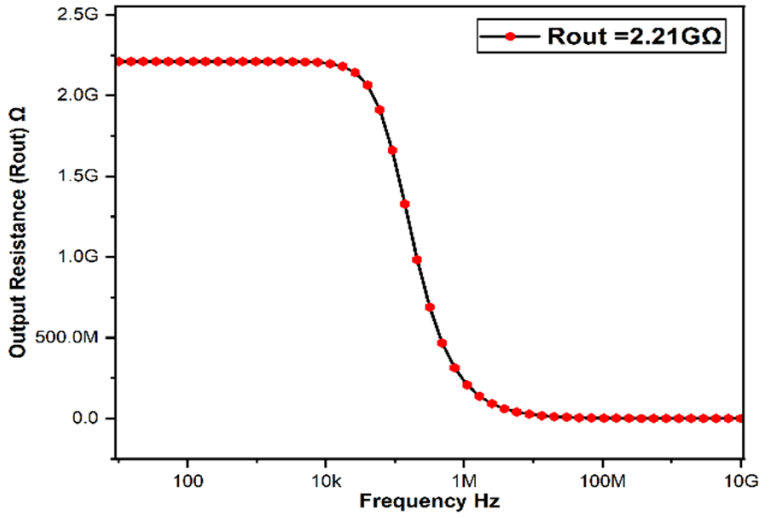

Figure 9. Output resistance (Rout) vs. frequency plot.

Table 2. Electricals Parameters of various corners.

Analysis→	Process Corner					Temperature				
Parameter↓	FF	FNSP	SNFP	SS	TT	−25	0	25	50	75
CE (%)	2.35	2.1	2.88	2.51	2.41	2.96	2.67	2.43	2.21	2.02
ICV(V)	1 m	1.1 m	1.45	1.46	1.6 m	0.7 m	0.9 m	1.5 m	1.38	1.32
Gain(mdB)	89.4	97.1	111.3	119.4	103.9	133	118.1	104.9	93.1	82.4
Rin (Ω)	1.51	1.49	1.42	1.43	1.46	0.88	1.13	1.43	1.82	2.34
Rout (GΩ)	1.60	1.92	2.46	2.62	2.21	2.63	2.44	2.23	2.01	1.79
Power dissipation (μW)	33.3	33.2	33.4	33.3	33.3	33.5	33.4	33.3	33.2	33.2

Table 3. Comparison between proposed current mirror and current mirrors reported in the literature.

Parameters	[16]	[19]	[20]	[21]	[22]	Proposed CM
Supply Voltage (V)	1	±0.5	±0.5	±0.5	0.9	±0.5
Technology (nm)	180	180	180	180	180	180
Current Range (μA)	0-440	0-500	0-1000	0-1000	0-100	0-2000
% Error	1.71	—	0.15	0.38	0.6	2.1
Minimum V_{in} (V)	0.52	—	—	—	0.04	0.14
Input Resistance (Ω)	21.43	17	48.7	0.407	496	1.35
Minimum V_{out} (V)	—	—	—	—	0.1	-0.1
Output Resistance (Ω)	1.14 G	750 k	3.06 G	50 G	1 M	2.11 G
Bandwidth (Hz)	6.17 G	4.5 G	875 M	2.1 G	181 M	675 M
Power dissipation (μW)	916.65	140	160	156	154	33.5

4. Conclusion

This paper presented a level shifted folded FVF class AB mode current mirror design using 180 nano meter MOS transistors with the help of Cadence. The performance of the proposed current mirror has been validated through small signal analysis which is supported through the simulation results and process corner analysis. The design has a wide current operating range up to 2 milli amperes with minimum error. The input compliance voltage also remains in the milli volt range. The current mirror's low input resistance of less than one ohm & large output resistance of 2 giga ohms has been achieved through feedback techniques. Such features at microwatt power dissipation can be useful in the realization of low voltage low power nanoscale VLSI circuits and bio-medical applications.

Authors Contributions
All authors have contributed equally to prepare the paper.

Availability of Data and Materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of Interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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