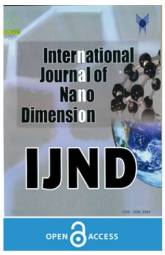

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Performance enhancement of flipped voltage follower current mirror in nanoscale technology

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Abstract:

The trend of technology downscaling to accommodate low supply requirement has been a continuous motivation for the IC industry. The nanoscale dimension MOSFET demands low supply but at the same time results in poor performance of analog circuits due to MOSFET secondary effects. In this paper, a fundamental block of current mode circuit, current mirror is proposed designed using MOSFET in nanoscale technology. The performance enhancement is done using modified structure of recently reported low voltage cell, flipped voltage follower. The modification incorporates cascoding of self cascode stage in flipped voltage follower. Further enhancement of this configuration is done in terms of MOSFET operating region for which quasi-floating gate technique is adopted. As a result, the final proposed quasi-floating gate based flipped voltage follower structure results is extremely low impedance at its output node compared to conventional flipped voltage follower. This property helps to achieve the ideal requirement of current mirror's input resistance. For output resistance the regulated cascode super cascode modified again with quasi-floating gate technique is used. The proposed current mirror results in input resistance of 81 ohms have been showed output resistance of 112 giga ohms & bandwidth of 2.8 giga hertz. The proposed circuit is designed using MOS technology of 180 nanometer & analyzed using Spice simulator at a dual polarity supply of $\pm$0.5 volt.

Keywords: Current mirror; FVF; Quasi floating gate; Input resistance; Output resistance; Self-cascode

1. Introduction

In the current scenario, MOS technology has evolved as a basic approach for performing computation at low power. With the advent of CMOS nano-scale technology, it got widely spread in almost all each electronic domain like telecommunications, consumer electronics, defense systems etc. The scaling approach fulfilled the market requirements but posed many challenges for semiconductor industries when it comes to nanoscale design. The IC designers faces challenges in terms of ICs reliability, productivity etc. Also, when it is about analog circuits that time the precision is not up to the mark, is mainly due to MOS second order effects. Since precision is one of the key requirements in analog, the analog design in nanoscale faces challenges at different stages of design & so requires new design approaches to fulfil the goal. It has been observed, in nanoscale technology with increase in gate current the current gain gets decreased so for current-mode circuits like current mirror does not achieve their ideal performance. In this paper, performance enhancement of current mirrors through use of new approach is shown. Current mirror is one of the widely used blocks in analog for biasing, active loading etc. [1]. The current mirror, being a fundamental block of current-mode circuits, needs to be designed in such a way that it achieves its desired performance. The ideal characteristics include zero input resistance, high output resistance,

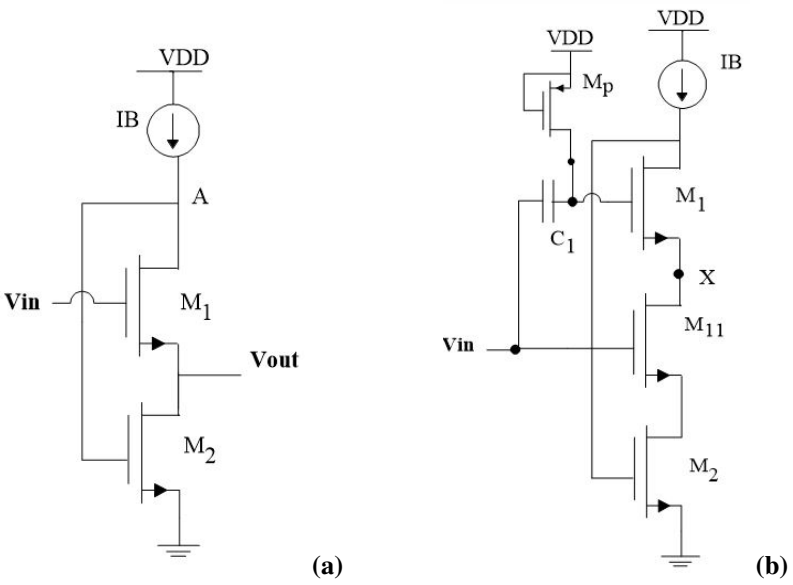

Figure 1. (a) Conventional flipped voltage follower; (b) Quasi floating gate self cascode flipped voltage follower.

wide bandwidth & for low power it should work in low supply voltage. With an aim to fulfil these goals, the flipped voltage follower (FVF) [2] & quasi floating gate (QFG) [3] approach has been used to enhance the performance of recently reported FVF current mirror in terms of input resistance whereas for output resistance enhancement the regulated cascode [4] followed to super cascode [5] is used. Here the role of FVF is to make the current mirror circuit work on low supply whereas the QFG technique is used to enhance the performance of FVF. A few recently reported low voltage current mirrors using QFG can be found in [6–11] & few relevant based on FVF structure can be found in [12–21]. Performance enhancement can also be achieved at low voltage through threshold voltage scaling [22–26]. However, these require special fabrication steps.

In the proposed method, FVF offers a low impedance node, so it is used as input of a current mirror which results in low input resistance. However, for further improvement the performance of conventional FVF is modified through self cascode (SC) structure. The use of SC enhances the effective transconductance of FVF but due to one of its transistors working in linear region the enhancement gets limited. Further to overcome this issue the QFG is incorporated in the SC structure resulting in change of the mode of transistor to saturation region. The final self cascode structure based FVF as Quasi-floating Gate Self Cascode (QFG-SC) FVF when applied to input node of current mirror, it significantly reduces the input resistance of proposed current mirror. The similar approach QFG-SC is used at the output of proposed current mirror as an inverting amplifier stage. This helps to achieve boosted output resistance in a range of giga ohms. These improvements do not require any complex circuits and external sources so the effective increase in power is also negligible.

The proposed work is divided into subparts as: The materials and method is discussed in section 2 which also discusses proposed work including small-signal detailed analysis. The results and discussion is carried out in section 3 followed to conclusion in section 4.

2. Material and methods

The conventional FVF, being a low voltage structure is widely adopted wherever low impedance requirement is demanded. It overcomes the associated drawback of standard voltage follower in terms of offset, output resistance, bandwidth, low power etc. due to presence of shunt feedback in the configuration. The schematic of NMOS based FVF architecture is shown in Fig. 1(a). The presence of feedback results in ($g_m r_0$) factor is seen by the output & the impedance level seen at output is ($1/gm_2gm_1r_{01}$). However, when applied as input in a current mode circuit, the achieved impedance is not found to be sufficient since the ideal case is zero impedance. To further reduce the impedance of FVF, the structure is modified through quasi-floating gate based self cascode (QFG-SC) stage as shown in Fig. 1(b) where output is shown through node X.

The problem associated with conventional self cascode is that one of the transistors, i.e. M_{11} operates in linear mode due to which limited enhancement in transconductance is observed for the complete structure. The mode of M_{11} can be changed to saturation by scaling the threshold voltage of MOSFET. So, when M_2 change in quasi-floating state the threshold voltage changes to

$$V_{th11,eff} = \frac{C_{T,qfg}}{C_1} V_{th11} - \frac{C'_{GD,MP}}{C_1} V_{DD} \quad (1)$$

Such shift helps to easily achieve the condition, $V_{DS,sat.M_{11}} \geq V_{th,M_1} - V_{th,M_{11}}$ & which when this condition becomes valid, it changes the mode of M_{11} to saturation. At this stage the effective transconductance gets significantly boosted. In the proposed FVF current mirror design, the input performance is improved through use of QFG-SC FVF block. Such improvement leads to much better input resistance & bandwidth response without affecting the output

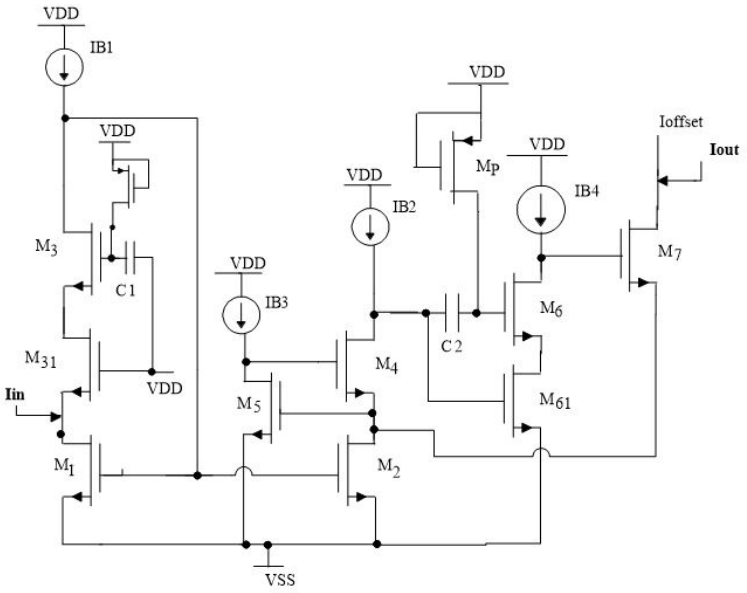

Figure 2. Proposed current mirror.

resistance.

2.1 Proposed work

The proposed current mirror using the FVF QFG-SC is shown in Fig. 2. As seen at input, it is modified using QFG-SC FVF structure.

Here a local negative shunt feedback loop is established using MOS transistor M_1, M_3, and M_{31} and DC current source I_{B1}. Since the transistor M_3 & M_{31} forms a self cascode stage, the effective transconductance experienced by M_1 gets boosted. Due to modification by QFG approach the achieved transconductance gets improved. As is known, the input resistance of a current mirror is inversely proportional to the transconductance on input transistor. The effective low impedance node at drain of M_1 results in reduced input resistance value, one of the key requirements of current mirror. Use of FVF also helps in reducing the input compliance voltage. For boosting output resistance, the output is configured as regulated cascode followed to super cascode. However, in proposed design instead of going for conventional super cascode stage it is again modified with QFG-SC structure. This modification is carried out for inverting amplifier stage driving the output of regulated cascode. The concept here too remains the same of changing the mode of region of operation. When both transistors turn in saturation, it leads to significant boosted output resistance to almost in range of hundreds of giga ohms. The change in structure results in effective threshold of M_6 as

$$V_{th,M6eff} = \frac{C_{T,qfg}}{C_1} V_{th,M6} - \frac{C'_{GD,MP}}{C_1} V_{DD} \qquad (2)$$

Due to scaled threshold of M_6, increase in the value of drain-to-source voltage of transistor M_{61} is observed which leads to change its mode from linear to saturation. The

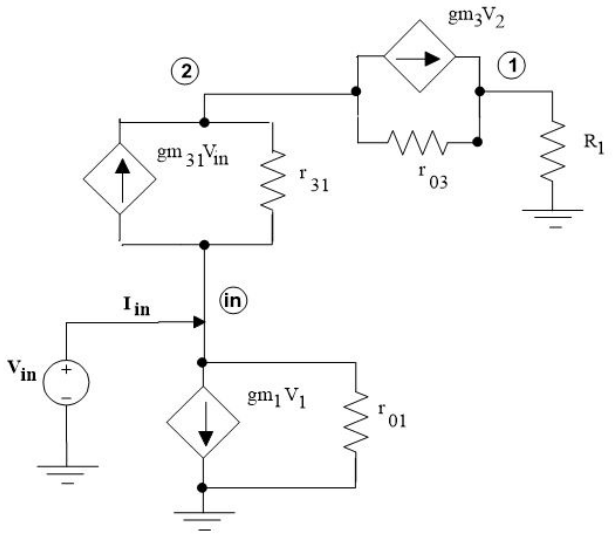

Figure 3. Small signal model to calculate input resistance.

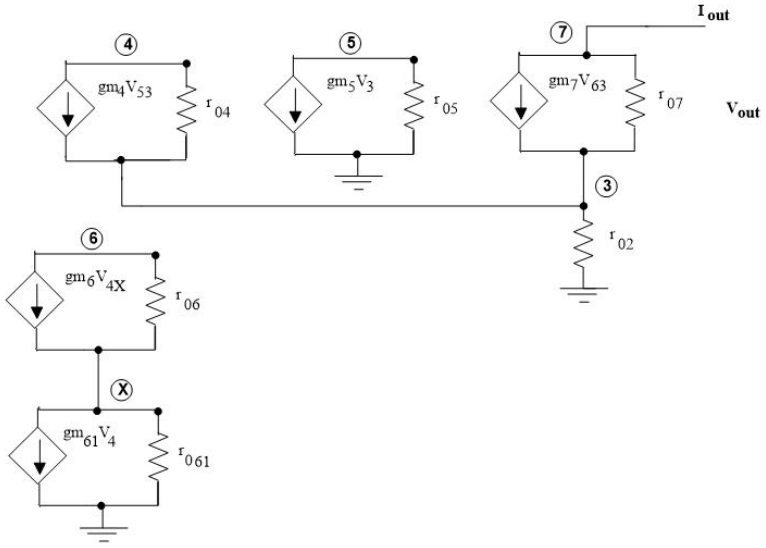

Figure 4. Small signal model to calculate output resistance.

resultant increase in the value of transconductance increases the output resistance in range of giga ohms.

2.2 Small signal analysis

The small signal is carried in terms of input and output resistances where the MOSFETs used is assumed to be working in saturation region.

2.2.1 Input resistance

The small-signal circuit for calculating the input resistance ($R_{in,prop.}$) of the proposed current mirror is shown in Fig. 3. At node 1

$$-g_{m3}V_2 + \frac{V_1 - V_2}{r_{03}} + \frac{V_1}{R_1} = 0 \tag{3}$$

Since $g_m r_0 \gg 1$ for saturation mode MOSFET

$$V_1 = g_{m3}(R_1 // r_{03})V_2 \tag{4}$$

At node 2

$$-g_{m31}V_{in} + \frac{V_2 - V_{in}}{r_{31}} = -\frac{V_1}{R_1} \tag{5}$$

At input node

$$i_{in} - g_{m31}V_{in} + \frac{V_2 - V_{in}}{r_{31}} = g_{m1}V_1 + \frac{V_{in}}{r_{01}} \tag{6}$$

From Eqs. 2, 3, and 4

$$\begin{aligned} i_{in} - g_{m31}V_{in} + \frac{r_{31}\left(-g_{m31}V_{in} + \frac{V_1}{R_1}\right) - V_{in}}{r_{31}} \\ = g_{m1}g_{m3}(R_1 // r_{03})r_{31}\left(-g_{m31}V_{in} + \frac{V_1}{R_1}\right) + \frac{V_{in}}{r_{01}} \end{aligned} \tag{7}$$

Assuming $R_1 \approx \infty$

$$\begin{aligned} R_{in,prop} &= \frac{V_{in}}{i_{in}} \\ &= \frac{1}{g_{m1}(g_{m3,qfg}r_{03,qfg})(g_{m31}r_{31}) + 2g_{m31} + \frac{1}{r_{01}}} \end{aligned} \tag{8}$$

From Eq. 6 it can be observed the input resistance gets reduced much lower compared to conventional FVF structure which is clearly visible in the result section.

2.2.2 Output resistance

The small-signal circuit for calculating the output resistance ($R_{out,prop}$) of proposed current mirror is shown in Fig. 4. Here

$$i_{out} = g_{m7}V_{63} + \frac{V_{out} - V_3}{r_{07}} \tag{9}$$

$$V_3 = i_{out}r_{02} \tag{10}$$

and

$$V_5 = -(g_{m6}r_{06})(g_{m4}r_{04})(1 + g_{m5}r_{05})(g_{m61}r_{061})V_2 \tag{11}$$

Table 1. Designing a test based on variables.

MOS	W (nano meter)	L (nano meter)
M1, M2	25000	240
M3, M31, M4, M7, M9	5000	240
M5	1000	240
M6, M61	2000	240
Mp	240	240
V_{dd}=0.5 V, V_{ss}=-0.5 V, C_1=C_2=1 pf, IB_1=10 μA, IB_2-IB_4=30 μA		

Table 2. Results of proposed current mirror and comparison with existing designs.

Parameters	[13]	[14]	citeu15	[16]	[17]	[18]	conv. FVF SC CM	prop. QFG-SC FVF CM
Current range (μA)	1000	0-200	0-150	0-500	0-1000	0-1000	0-1000	0-1000
I_{bias} (μA)	500	—-	—-	65	65	65	65	65
Input resistance (Ω)	68.3	130	12.3K	170	0407	487	330	81.6
Output resistance (Ω)	10 G	9.5 G	—	750 K	50 G	3.06 G	22.4 G	112 G
-3db frequency (Hz)	402M	2.7G	624M	4.5G	2.1G	875M	2.7 G	2.8 G
Supply (V)	1	0.8	1.2	0.5	0.5	0.5	0.5	0.5
DC Power (μW)	110	79.33	99	140	156	160	162	170
Technology (μm)	0.18	0.18	1.18	0.18	0.18	0.18	0.18	0.18

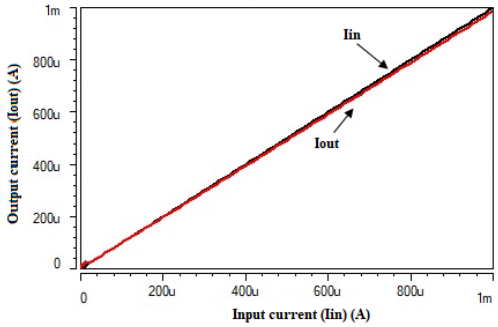

Figure 5. Transfer characteristics.

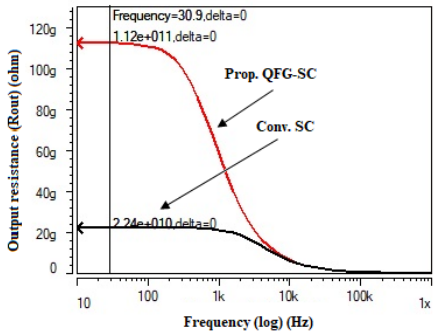

Figure 7. Output resistance plots.

From Eqs. 7, 8, and 9

$$\begin{aligned} R_{out,prop.} &= \frac{V_{out}}{i_{out}} \\ &= (r_{07} + r_{02}((g_{m7}r_{07})(g_{m6}r_{06}) \\ &\times (g_{m61}r_{061})(g_{m4}r_{04})(1 + g_{m5}r_{05}) \\ &+ (1 + g_{m7}r_{07}))) \end{aligned} \tag{12}$$

Since $g_m r_o \gg 1$

$$\begin{aligned} R_{out,prop.} &\approx r_{o2}(g_{m4}r_{04})(g_{m5}r_{05}) \\ &\times (g_{m6,qfg}r_{06,qfg})(g_{m61}r_{061})(g_{m7}r_{07}) \end{aligned} \tag{13}$$

As seen in Eq. 11, the QFG-SC structure introduces a multiple factor of ($g_{m,qfg}r_{0,qfg}$) in the output which results in resistance enhancement clearly visible in the result section.

3. Results and discussions

The proposed current mirror is designed and analyzed using the MOSFET models of 180 nanometer technology at a dual supply of $\pm$0.5 volt using Spice. The device dimension and other parameter assumed for analysis is listed in Table 1. The transfer characteristic is shown in Fig. 5, where observation can be made that the output current trajectory is almost same as input current and so overlapping can be seen. This shows the accuracy in current transfer which here is till 1000 micro amperes. Such a large dynamic range is useful in implementing linear circuits with wide range. Thus, high precision can be assured with the proposed method. The input current is swept from 0 to 1000 micro amperes in the step size of 10 micro amperes. The input compliance voltage required for its proper operation is also reduced due to the presence of FVF structure.

The key observation can be seen in the input resistance curve as shown in Fig. 6. Here the value obtained for proposed current mirror by using QFG-SC FVF is 81 ohms and when compared to use of conventional FVF at input, the value of input resistance is 330 ohms. Also, the value is much lower

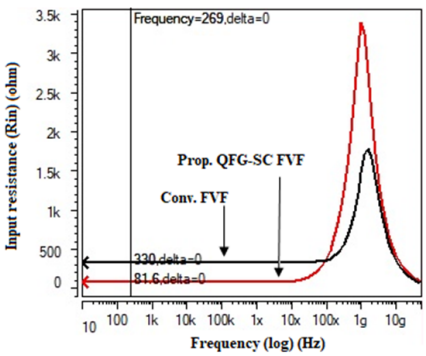

Figure 6. Input resistance plots.

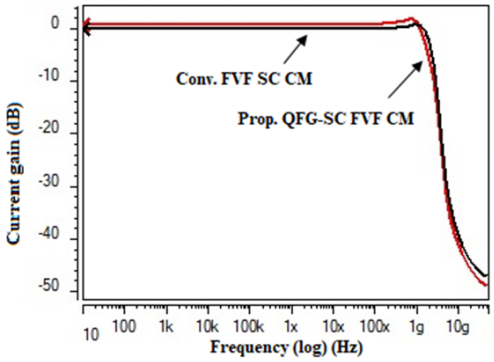

Figure 8. Frequency response.

than existing designs reported in literature as shown in the comparison table. This became possible due to the FVF stage & the modification carried through QFG-SC in the FVF stage. A similar advantage can be seen in the output resistance curve as shown in Fig. 7. The output resistance gets boosted to 112 giga ohms by using QFG-SC structure. If the inverting stage comprises of simple conventional SC, then obtained value of output resistance is 22.4 giga ohm which is much lesser than the proposed current mirror.
The bandwidth response is shown in Fig. 8. As can be observed the proposed QFG-SC FVF current mirror bandwidth and the conventional FVF SC current mirror is almost same. The bandwidth found for both is around 2.8 giga hertz. From the above graphs, it can be easily concluded that the proposed current mirror without sacrificing the bandwidth and significant power increase improves the input and output resistance satisfying low power design requirement. The complete result of proposed current mirror is summarized and compared with related recent designs is shown in Table 2.
Compared to prior arts it can be observed that the proposed design offers a wide dynamic range with low input resistance & significantly high output resistance at a giga hertz bandwidth.

4. Conclusion

A high-performance dual supply rail based low voltage FVF current mirror has been proposed. The contribution falls in terms of reduced input resistance without sacrificing other performance parameters. The technique adopted QFG in SC can be one of the promising solutions to enhance any circuit performance & FVF for making it to work in low supply. The enhancement seen is supported through mathematical analysis which satisfies the results as well. The current mirrors reduced input resistance in ohms & boosted output resistance in giga ohms at giga hertz bandwidth can be used in bio-amplifiers for better CMRR and PSRR of differential amplifier, to improve DC gain, in implantable communication modules as frequency synthesizers etc. So, using the proposed architecture a high-speed low power low power VLSI system can be realized.

Ethical Approval
This manuscript does not report on or involve the use of any animal or human data or tissue. So the ethical approval is not applicable.

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Authors Contributions
All authors have contributed equally to prepare the paper.

Availability of Data and Materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of Interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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