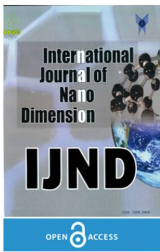

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Impact of nanometric buried Oxide layer on subthreshold swing and drain conductance of junctionless accumulation mode MOSFET for analog circuit applications

Supratim Datta[1], Arpan Deyasi[1*], Arighna Basak[2], Angsuman Sarkar[3]

[1]*Department of Electronics and Communication Engineering, RCC Institute of Information Technology, India.*
[2]*Department of Electronics and Communication Engineering, Brainware University, India.*
[3]*Department of ECE, Kalyani Government Engineering College, West Bengal, India.*

[*]**Corresponding author:** deyasiarpan@yahoo.co.in

REVIEW PAPER

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Abstract:

Drain conductance to drain current ratio is analytically investigated for junctionless accumulation mode MOSFET in presence of ultrathin buried oxide layer invoking the effect of conduction band tunnelling, within realistic range of dimensional configurations in nano regime. By taking into account the flatband voltage's influence and the image charge effect at the oxide-semiconductor interface, subthreshold swing is evaluated over practical range of applied bias. Comparative study reveals that 42% and 36.5% improvements are found with published literature for the conductance to current ratio, whereas reduction of corresponding subthreshold swing is 51% and 34% respectively, considering all the data are computed w.r.t reported value of drain current; for identical structural and electrical configurations. Accuracy of the analytical findings is verified against that of the TCAD software's numerical analysis. Result speaks in favour of the proposed candidate for amplifying low voltage signal in large scale along with suppression of leakage effect for analog amplifier applications.

Keywords: Buried oxide layer; Dielectric constant; Nano-dimension; Subthreshold swing

1. Introduction

The chronological development of MOS (Metal-Oxide-Semiconductor) architectures with growing complexity has been remained a fundamental driving force in creating new roadmap of nano-electronic [1, 2] devices during the last two decades, that revolutionised electronics industry. Owing to the benefits of lower power consumption [3], higher packing density and scalability; MOS transistors become enable to serve the purpose of diverse applications, simultaneously to be crammed into smaller chip area. However, detrimental effects because of the continuous shrinkage of device size leads to a variety of phenomena including gate tunnelling current (GTC) [4], the drain-induced barrier lowering (DIBL) effect [5], quantum effects [6], higher leakage current [7, 8], and increased power consumption [9]. Remedy to these ever-increasing problems is determined by unconventional architectures and novel material compositions.

Among the modern alternative device designs, Junctionless MOSFET (JL Metal-Oxide-Semiconductor-Field-Effect-Transistor) structures [10–12] have already exhibited potential solutions compared with traditional junction MOSFETs, due to the facts that it does not require abrupt source and drain connections, moreover, can maintain random dopant fluctuation without the need for trouble-some and expensive ultra-fast strengthening procedures. However, due to hindrance of carrier mobility, the structure depicts lower ON current and transconductance, which restricts its circuit applications. Problem is thereafter resolved using accumulation mode [13, 14] of operation

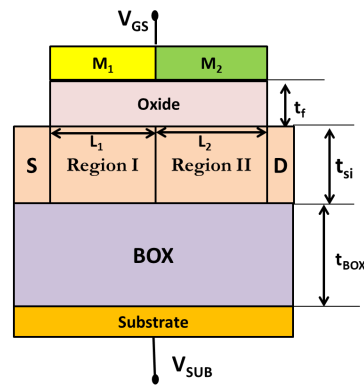

Figure 1. 2D view of JAM with buried oxide layer.

(JAM) with buried oxide layer as a viable option for future nanoscale device applications.

Buried-oxide (BOX) layer based MOSFET architectures [15, 16] have gained more recognition due to several benefits over conventional bulk MOS devices designed in absence of that. The BOX layer serves as an insulator in BOX-based MOS device, keeping the transistor channel apart from the substrate and limiting the penetration of the electric field into the substrate. As a result, reliability improves and the possibility of HCEs, which can lead to device degradation, decreases. The decreased parasitic junction capacitance, better transconductance, and regulated subthreshold swing of BOX-based MOS devices are added advantages. The BOX layer offers a consistent doping profile and lowers SCEs, improving electrical performance of the device.

In the present work, differential conductance to drain current ratio is computed as a function of applied voltage considering buried oxide layer, and subthreshold swing is also evaluated to qualitatively study the effect of leakage current. All the dimensional variations, involving thickness of buried oxide layer, dielectric thickness, doping density, and vertical voltage is set within practical range of interest. Results obtained are compared with previous findings, and therefore, effect of buried oxide layer is evaluated. Detailed analytical modelling is presented in the next few sections along with proposed device structure, and results are summarized with conclusions.

2. Device Structure

According to the recent study, Wagaj *et al* . developed a structure of dual material gate SOI junctionless transistor [17]. In addition, accumulation mode condition provides an additional degree of freedom to optimize subthreshold swings and drain conductance. Therefore, as per references and incorporated the advantage of the accumulation mode condition on the structure, JAM MOSFET with buried oxide layer is proposed in this manuscript and Fig. 1 represents 2-D schematics of JAM MOSFET with buried oxide layer. Workfunctions of 4.8 eV and 4.6 eV are used to make the gate materials, which helps to sub-divided the device in two regions, region-I and region-II respectively with lengths L_1 and L_2. All key regions, source, drain, and substrate; are equally doped with the concentration of 10^{21} m^{-3}. Substrate thickness (t_{Si}) is 10 nm whereas oxide layer thickness (t_f) is 5 nm. In addition to that, as per reference [17–20] a detailed structural parameter is presented in Table 1.

3. Analytical Modelling

2D Poisson's equation for JAM with buried oxide layer can be expressed as

$$\frac{\partial^2\phi(x,y)}{dx^2}+\frac{\partial^2\phi(x,y)}{dy^2}=\frac{qN_D}{\varepsilon_{si}}$$

for

$$0 \le x \le L \quad ,0 \le y \le t_{si} \tag{1}$$

Table 1. Various device parameters and their specifications.

Device parameters	JAM MOSFET
Gate length	60 nm
Front oxide thickness (t_f)	5 nm
Back oxide (BOX) thickness (t_{BOX})	50 nm
Silicon Thickness (t_{Si})	10 nm
Work function of M_1	4.8 ev (Au)
Work function of M_2	4.6 ev (Mo)
Doping concentration	10^{21} m^{-3}

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where ND indicates as density of doping, ε_{si} indicates as channel's permittivity, q indicates as charge of electrons For computing surface potential in the x-dependent regions, namely region-I and region-II, parabolic approximation is used in the following form

$$\phi_I(x,y) = \phi_S I(x) + C_{I1}(x)y + C_{I2}(x)y^2$$

for

$$\leq x \leq L_1 \quad ,0 \leq y \leq t_{si} \tag{2}$$

$$\phi_{II}(x,y) = \phi_{SII}(x) + C_{II1}(x)y + C_{II2}(x)y^2$$

for

$$0 \leq x \leq L_1 + L_2 \quad ,0 \leq y \leq t_{si} \tag{3}$$

The distribution of electric flux at front side of gate 1 and gate 2 are written as

$$\left.\frac{\partial \phi_1(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi s_1(x) - V_{GS_1}}{t_f} \quad \text{for gate1} \tag{4}$$

$$\left.\frac{\partial \phi_1(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi s_2(x) - V_{GS_2}}{t_f} \quad \text{for gate2} \tag{5}$$

where t_f indicates as gate-oxide thickness and εox indicates as gate-oxide permittivity

$$V_{GS_1} = V_{GS} - V_{FB_1}$$
$$V_{GS_2} = V_{GS} - V_{FB_2}$$

V_{GS} indicates as gate voltage and V_{FB_1},V_{FB_2} indicates as flat band voltages for gate1 and gate2. The distribution of electric flux at bottom side of gate1 and gate2 are written as

$$\left.\frac{\partial \phi_1(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{SUB1} - \phi_B(x)}{t_{BOX}} \quad \text{for gate1} \tag{6}$$

$$\left.\frac{\partial \phi_2(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{SUB2} - \phi_B(x)}{t_{BOX}} \quad \text{for gate2} \tag{7}$$

where t_{BOX} indicates as thickness of buried-oxide

$$V_{SUB1} = V_{SUB} - V_{FB,b}$$

V_{SUB} indicates as substrate's voltage and $V_{FB,b}$ indicates as flat band voltage for bottom gates. Continuous potential distributions are obtained near gate1 and gate2. Therefore,

$$\phi_I(L_1,0) = \phi_{II}(L_1,0) \tag{8}$$

Moreover, continuous electric field is obtained at junction of gate1 and gate2

$$\frac{\partial \phi_1(x,y)}{dx}|_{x=L_1} = \frac{\partial \phi_2(x,y)}{dx}|_{x=L_1} \tag{9}$$

Near source distribution of potential is described as

$$\phi_I(0,0) = \phi_{sI}(0) = V_{bi} \tag{10}$$

Near drain side, distribution of potential is described as

$$\phi_{II}(L_1+L_2,0) = \phi_{sII}(L_1+L_2) = V_{bi} + V_{ds} \tag{11}$$

where, V_{bi} indicates as built in potential and written as

$$V_{bi} = \frac{KT}{q} \log_e \frac{N_D}{n_i^2} \tag{12}$$

From Eqs. 2, 4 and 6 we get

$$\phi_I(x,y) = \phi_{sI}(x) + C_{I1}(x)y + C_{I2}(x)y^2$$

$$\implies \frac{\partial \phi_I(x,y)}{dy}|_{y=0} = 0 + C_{I1}(x) + 2C_{I2}(x)y$$

where $\quad C_{I1}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{sI}(x) - V_{GS1}}{t_f} \in$
Again

$$\phi_{sI}(x) + C_{I1}(x)t_{si} + C_{I2}(x)t_{si} + CZ_{I2}(x)t_{si}^2 = \phi_B(x)$$

Differentiating,

$$C_{I1}(x) + 2C_{I2}(x)t_{si} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{SUB1} - \phi_B(x)}{t_{BOX}}$$

where $\quad C_{I2} = C_b \left(\frac{V_{SUB1} - \phi_{B(x)}}{t_{BOX}}\right), \quad C_{BOX} = \frac{\varepsilon_{ox}}{t_{BOX}}$

Moreover, for gate2 regions

$$\phi_{sII}(x) + C_{II1}(x)t_{si} + C_{II2}(x)t_{si}^2 = \phi_{B_{(x)}}$$

where,

$$C_{II1} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{sII}(x) - V_{GS2}}{t_f}$$

$$C_{II2} = \frac{V_{SUB1} + V_{GS1}\left(\frac{C_f}{C_b} + \frac{C_f}{C_{si}}\right) - \phi_{sI}(x)\left[1 + \frac{C_f}{C_b} + \frac{C_f}{C_{si}}\right]}{t_{si}^2\left(1 + 2\frac{C_{si}}{C_b}\right)}$$

$$C_{BOX} = \frac{\varepsilon_{ox}}{t_{BOX}}$$

$$C_{si} = \frac{\varepsilon_{si}}{t_{si}}$$

Therefore after solution, obtain potential distribution of the structure.

$$\frac{d^2\phi_{sI}(x)}{dx^2} - \alpha\phi_{sI}(x) = \beta_1 \tag{13}$$

$$\frac{d^2\phi_{sII}(x)}{dx^2} - \alpha\phi_{sII}(x) = \beta_2 \tag{14}$$

where,

$$\alpha = \frac{2(1 + \frac{C_f}{C_{BOX}} + \frac{C_f}{C_{si}})}{t_{si}^2(1 + 2\frac{C_{si}}{C_{BOX}})}$$

$$\beta_1 = \frac{-qN_D}{\varepsilon_{si}} - 2V_{GS1}\left[\frac{\frac{C_f}{C_{BOX}} + \frac{C_f}{C_{si}}}{t_{si}^2\left(1 + 2\frac{C_{si}}{C_{BOX}}\right)}\right] - 2V_{SUB1}\left[\frac{1}{t_{si}^2\left(1 + 2\frac{C_{si}}{C_{BOX}}\right)}\right]$$

$$\beta_2 = \frac{-qN_D}{\varepsilon_{si}} - 2V_{GS2}\left[\frac{\frac{C_f}{C_{BOX}} + \frac{C_f}{C_{si}}}{t_{si}^2\left(1 + 2\frac{C_{si}}{C_{BOX}}\right)}\right]$$

$$-2V_{SUB1}\left[\frac{1}{t_{si}^2\left(1+2\frac{C_{si}}{C_{BOX}}\right)}\right]$$

The potential distributions are expressed as

$$\phi_{sI}(x) = A\exp(\alpha x) + B\exp(-\alpha x) - \frac{\beta_1}{\alpha} \quad (15)$$

$$\phi_{s2}(x) = C\exp(\alpha(x-L_1)) + D\exp(\alpha(x-L_1)) - \frac{\beta_2}{\alpha} \quad (16)$$

where $\eta_1 = \sqrt{\alpha}$

$$\eta_2 = \sqrt{-\alpha}$$

$$\gamma_1 = -\frac{\beta_1}{\alpha} = \frac{\frac{-qN_D}{\varepsilon_{si}} - 2V_{GS1}^1\left[\frac{\frac{C_f}{C_{BOX}}+\frac{C_f}{C_{si}}}{t_{si}^2\left(1+2\frac{C_{si}}{C_{BOX}}\right)}\right] - 2V_{SUB1}\left[\frac{1}{t_{si}^2\left(1+2\frac{C_{si}}{C_{BOX}}\right)}\right]}{\frac{2\left(1+\frac{C_f}{C_{BOX}}+\frac{C_f}{C_{si}}\right)}{t_{si}^2\left(1+2\frac{C_{si}}{C_{BOX}}\right)}}$$

$$\gamma_2 = -\frac{\beta_2}{\alpha} = \frac{\frac{-qN_D}{\varepsilon_{si}} - 2V_{GS2}\left[\frac{\frac{C_f}{C_{BOX}}+\frac{C_f}{C_{si}}}{t_{si}^2\left(1+2\frac{C_{si}}{C_{BOX}}\right)}\right] - 2V_{SUB1}\left[\frac{1}{t_{si}^2\left(1+2\frac{C_{si}}{C_{BOX}}\right)}\right]}{\frac{2\left(1+\frac{C_f}{C_{BOX}}+\frac{C_f}{C_{si}}\right)}{t_{si}^2\left(1+2\frac{C_{si}}{C_{BOX}}\right)}}$$

Moreover the electric field distribution are expressed as

$$E_1(x) = \frac{d\phi_1(x,y)}{dx}\Big|_{y=0} = \frac{d\phi_{s_1}(x)}{dx} = A\alpha\exp(\alpha x) - B\alpha\exp(-\alpha x) \quad (17)$$

$$E_2(x) = \frac{d\phi_2(x,y)}{dx}\Big|_{y=0} = \frac{d\phi_{s_2}(x)}{dx} = C\alpha\exp(\alpha(x-L_1)) - D\alpha\exp(-\alpha(x-L_1)) \quad (18)$$

Using the boundary condition we obtained the values of A, B, C, D

$$A = \frac{(V_{bi}-\gamma_2+V_{DS})\exp(-\alpha(L_1+L_2))}{1-\exp(-2\alpha(L_1+L_2))} - \frac{\exp(-\alpha(L_1+L_2))(V_{bi}-\gamma_1)\times\exp(-\alpha(L_1+L_2))}{1-\exp(-2\alpha(L_1+L_2))} - \frac{(\gamma_1-\gamma_2)\cosh(\alpha L_2)\times\exp(-\alpha(L_1+L_2))}{1-\exp(-2\alpha(L_1+L_2))}$$

$$B = \frac{(V_{bi}-\gamma_1)}{1-\exp(-2\alpha(L_1+L_2))} - \frac{(V_{bi}-\gamma_2+V_{DS})\exp(-\alpha(L_1+L_2))}{1-\exp(-2\alpha(L_1+L_2))} + \frac{(\gamma_1-\gamma_2)\cosh(\alpha L_2)\exp(-\alpha(L_1+L_2))}{1-\exp(-2\alpha(L_1+L_2))}$$

$$C = A\exp(\alpha L_1) + \frac{\gamma_1-\gamma_2}{2}$$

$$D = B\exp(\alpha L_1) + \frac{\gamma_1-\gamma_2}{2}$$

When two metal gates with differing work functions are present on a semiconductor in this form, the metal gate with the larger work function alone determines the surface potential minimum. Consequently, the minimum potential may be determined as

$$\phi_s(Z_{\min}) = 2\sqrt{AB} - \frac{\beta_1}{\alpha} \quad (19)$$

which is minimum at

$$Z_{min} = \frac{1}{2\sqrt{\alpha}}\ln\left(\frac{B}{A}\right)_{\min}$$

$$= \frac{\tau}{2}\ln\left(\frac{\Upsilon1+\Upsilon2}{\Upsilon3-\Upsilon4-\Upsilon2}\right)$$

in which

$$\Upsilon1 = (V_{bi}-\gamma_1) - (V_{bi}-\gamma_2+V_{DS})\exp(-\alpha(L_1+L_2));$$
$$\Upsilon2 = (\gamma_1-\gamma_2)\cosh(\alpha L_2)\exp(-\alpha(L_1+L_2));$$
$$\Upsilon3 = (V_{bi}-\gamma_2+V_{DS})\exp(-\alpha(L_1+L_2));$$
$$\Upsilon4 = (V_{bi}-\gamma_1)\exp(-\alpha(L_1+L_2));$$

where

$$\tau = \frac{1}{\sqrt{\alpha}} = \frac{t_{si}\sqrt{\left(1+2\frac{C_{si}}{C_{BOX}}\right)}}{\sqrt{2}\sqrt{\left(1+\frac{C_f}{C_{BOX}}+\frac{C_f}{C_{si}}\right)}}$$

$$\phi_s(Z_{\min}) = \left[\frac{\sqrt{\zeta^2-\xi^2}}{\Lambda+\Xi}\right]$$

in which

$$\zeta = (V_{bi}-\gamma_2+V_{DS})\exp(-\alpha(L_1+L_2))$$

and

$$\xi = (\gamma_1-\gamma_2)\cosh(\alpha L_2) - (\gamma_1-\gamma_2)\cosh(\alpha L_2))\exp(-\alpha(L_1+L_2)$$

and

$$\Lambda = \frac{1}{2}(1-\exp(-2\alpha(L_1+L_2))) - \frac{qN_D}{s_{si}\alpha}$$

and

$$\Xi = V_{GS}^1\left(\frac{\frac{C_f}{V_{BOX}}+\frac{C_f}{C_{si}}}{t_{si}^2(1+2\frac{C_{si}}{C_{BOX}})}\right) + V_{SUB}^1\left(\frac{1}{t_{si}^2(1+2\frac{C_{si}}{C_{BOX}})}\right) \quad (20)$$

Therefore TGF can be calculated as

$$\frac{g_m}{I_d} = \frac{q}{KT}\left(\frac{\partial\phi_s(Z_{\min})}{\partial V_{GS}}\right) \quad (21)$$

$$\frac{\partial\phi_s(Z_{\min})}{\partial V_{GS}} = \frac{1}{[2\sqrt{AB}\frac{1}{2}[1-\exp(-2\alpha L_1-2\alpha L_2)]]} [-(V_{bi}-\gamma_2+V_{DS}\exp(\alpha(L_1+L_2))/ -(\gamma_1-\gamma_2)\cosh(\alpha L_2)\exp(\alpha(L_1+L_2)) \times(\exp(\alpha(L_1+L_2))-1)]+1 \quad (22)$$

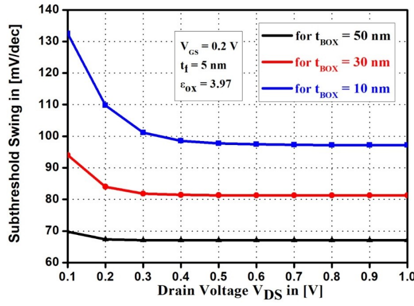

Figure 2. Subthreshold Swing variations of JAM MOSFET with buried oxide layer structure for various t_{BOX}.

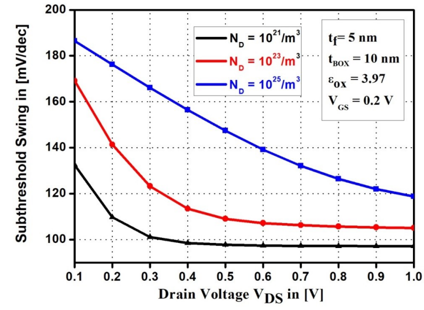

Figure 4. Subthreshold Swing variations of JAM MOSFET with buried oxide layer structure for various N_D

$$
\begin{aligned}
\frac{g_m}{I_d} = &\frac{q}{KT}\Big\{\frac{1}{[2\sqrt{AB}\frac{1}{2}[1-\exp(-2\alpha L_1-2\alpha L_2)]]} \\
&[-(V_{bi}-\gamma_2+V_{DS}\exp(\alpha(L_1+L_2))/ \\
&-(\gamma_1-\gamma_2)\cosh(\alpha L_2)\exp(\alpha(L_1+L_2)) \\
&\times(\exp(\alpha(L_1+L_2))-1)]+1\Big\}
\end{aligned} \tag{23}
$$

Moreover, the drain conductance-to-drain current ratio (g_{DS}/I_D) is given by,

$$
\frac{g_m}{I_d} = \frac{q}{KT}\Big(\frac{\partial\phi_s(Z_{\min})}{\partial V_{GS}}\Big) \tag{24}
$$

Differentiating (25) with respect to VDS, we get

$$
\frac{\partial\phi_s(Z_{\min})}{\partial V_{DS}} = \frac{1}{R}\times\frac{1}{2\sqrt{\{M\}-\{N\}^2}\times\{[Q]-2[P]\}}
$$

in which

$$
\begin{aligned}
R =& 0.5(1-\exp(-2\alpha L_1-2\alpha L_2)) \\
&\text{and} \\
M =& (V_{bi}-\gamma_2+V_{DS})^2\times(\exp(-\alpha L_1-\alpha L_2))^2 \\
&\text{and} \\
N =& \gamma_1\cosh\alpha L_2-\gamma_2\cosh\alpha L_2 \\
&-\gamma_1\cosh(\alpha L_2)\exp(-\alpha L_1-\alpha L_2) \\
&+\gamma_2\cosh(\alpha L_2)\exp(-\alpha L_1-\alpha L_2) \\
&\text{and} \\
Q =& (\exp(-\alpha L_1-\alpha L_2))^2\times(Vbi-\gamma_2+1)^2 \\
&\text{and} \\
P =& \gamma_1\cosh\alpha L_2-\gamma_2\cosh\alpha L_2 \\
&-\gamma_1\cosh(\alpha L_2)\exp(-\alpha L_1-\alpha L_2) \\
&+\gamma_2\cosh(\alpha L_2)\exp(-\alpha L_1-\alpha L_2)
\end{aligned} \tag{25}
$$

Substituting Eq. 26 in Eq. 25, the drain-conductance-to-drain current ratio for JAM MOSFET is obtained as

$$
\frac{g_{DS}}{I_{gs}} = \frac{q}{KT}\Big\{\frac{1}{R}\times\frac{1}{2\sqrt{\{M\}-\{N\}^2}\times\{[Q]-2[P]\}}\Big\}
$$

in which

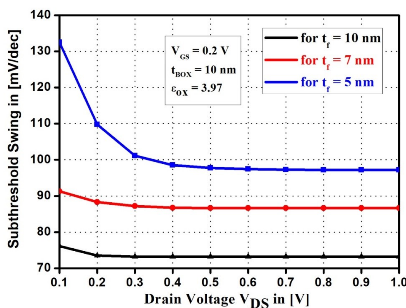

Figure 3. Subthreshold Swing variations of JAM MOSFET with buried oxide layer structure for various t_f.

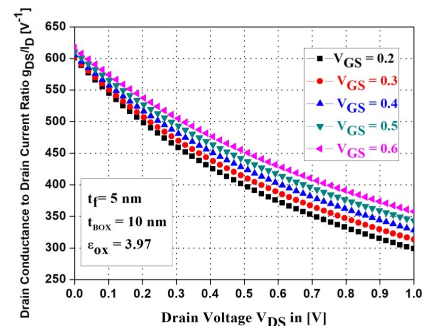

Figure 5. Drain-conductance-to-drain-current-ratio variations of JAM with buried oxide layer structure for various V_{GS}.

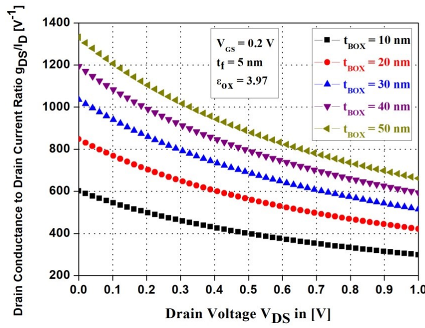

Figure 6. Drain-conductance-to-drain-current-ratio variations of JAM with buried oxide layer structure for various t_{BOX}.

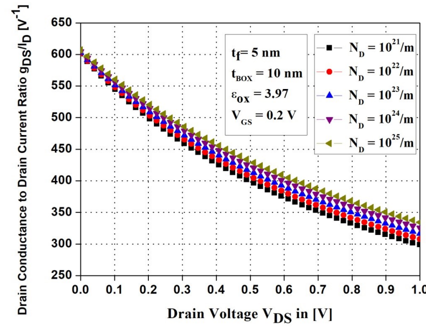

Figure 8. Drain-conductance-to-drain-current-ratio variations of JAM with buried oxide layer structure for various N_D.

$$
\begin{aligned}
R =& 0.5(1-\exp(-2\alpha L_1 - 2\alpha L_2)) \\
&\text{and} \\
M =& (V_{bi} - \gamma_2 + V_{DS})^2 \times (\exp(-\alpha L_1 - \alpha L_2))^2 \\
&\text{and} \\
N =& \gamma_1 \cosh \alpha L_2 - \gamma_2 \cosh \alpha L_2 \\
&- \gamma_1 \cosh(\alpha L_2) \exp(-\alpha L_1 - \alpha L_2) \\
&+ \gamma_2 \cosh(\alpha L_2) \exp(-\alpha L_1 - \alpha L_2) \\
&\text{and} \\
Q =& (\exp(-\alpha L_1 - \alpha L_2))^2 \times (Vbi - \gamma_2 + 1)^2 \\
&\text{and} \\
P =& \gamma_1 \cosh \alpha L_2 - \gamma_2 \cosh \alpha L_2 \\
&- \gamma_1 \cosh(\alpha L_2) \exp(-\alpha L_1 - \alpha L_2) \\
&+ \gamma_2 \cosh(\alpha L_2) \exp(-\alpha L_1 - \alpha L_2) \qquad (26)
\end{aligned}
$$

4. Result and Discussion

Based on the analytical modelling described in the above section, both subthreshold swing and normalized drain conductance are computed and plotted as functions of applied horizontal bias. Figures 2 and 3 analyze changes in subthreshold swing (SS) of JAM MOSFET with buried oxide layer structure with respect to V_{DS} for various t_f and t_{BOX} respectively. Both figures illustrates that the structure exhibits higher values of sub-threshold swing for 50 nm thickness of buried-oxide layer and 10 nm of thickness of gate dielectrics at lower values of V_{DS}.

Additionally, variations of subthreshold swing for various values of N_D are analyses with respect V_{DS} in (figure 4). Better SS is obtained for lower doping concentrations (N_D $=10^{21}/m^3$) for this structure at lower ranges of V_{DS}.

Drain-conductance-to-drain-current-ratio, g_{DS}/I_D is indeed an important parameter in MOSFET design. It is a measure of the conductance of the MOSFET channel between the drain and the source terminals, normalized by the drain current. The g_{DS}/I_D ratio is often used to indicate the mode of operation of the MOSFET and its performance in terms of switching speed and power efficiency. A high g_{DS}/I_D, is generally desirable for applications that require high power efficiency and high gain performance, such as power amplifiers, RF transmitters, and switching power supplies. In power amplifiers and RF transmitters, a high g_{DS}/I_D allows for better power efficiency and higher gain performance, which are critical for transmitting signals over long distances. In switching power supplies, a high g_{DS}/I_D allows for faster switching speeds and higher power efficiency, which are important for regulating power consumption in electronic devices.

Therefore, a high g_{DS}/I_D is generally desirable for ap-

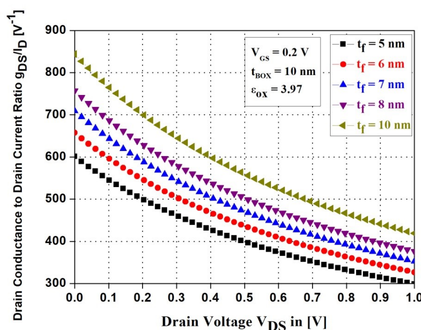

Figure 7. Drain-conductance-to-drain-current-ratio variations of JAM with buried oxide layer structure for various t_f.

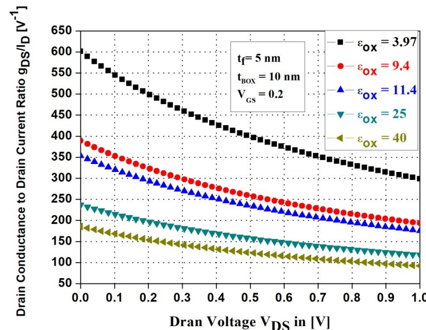

Figure 9. Drain-conductance-to-drain-current-ratio variations of JAM with buried oxide layer structure for various ε_{ox}.

Table 2. Drain Conductance variation with applied bias

Drain Voltage	Drain Conductance (g_{DS}) × 10^{-4} (A/V)		
(V)	[17]	[18]	Present work
0.00	5.3	5.5	8.2178
0.03	5.1	4.9	8.2168
0.06	4.8	4.5	8.2159
0.10	4.2	4	8.2149
0.13	3.7	3.4	8.2139
0.16	3.4	2.8	8.2130
0.20	2.3	1.8	8.2120
0.23	2	1.2	8.2111
0.26	1.6	1	8.2101
0.30	0.9	0.5	8.2091
0.33	0.7	0.4	8.2082
0.36	0.5	0.3	8.2072
0.40	0.3	0.1	8.2063
0.43	0.2	0.1	8.2053
0.46	0.1	0.1	8.2043
0.50	0.1	0.1	8.2034

Table 3. Drain conductance to drain current ratio with applied bias

Drain Voltage	Drain conductance to drain current ratio		
[VDS] (V)	[17]	[18]	Present work
0	600.9104	657.3751	1036.2
0.03	588.7547	644.0702	1015.2
0.06	565.8614	619.0131	975.7
0.1	544.6818	595.8328	939.2
0.13	534.6756	584.8816	922
0.16	515.727	564.1442	889.3
0.2	498.0756	544.827	858.9
0.23	489.6954	535.6561	844.4
0.26	473.7533	518.2104	816.9
0.3	458.8166	501.8652	791.2
0.33	451.6959	494.0733	778.9
0.36	438.0977	479.1934	755.4
0.4	425.2943	465.1836	733.4
0.43	419.1691	458.4815	722.8
0.46	407.4334	445.6404	702.6
0.5	396.3369	433.499	683.4

Table 4. Subthreshold swing variation with applied bias.

Drain Voltage	Subthreshold Swing (mV/dec)		
[VDS] (V)	[17]	[18]	Present work
0.1	167.821416	152.250597	76.11636
0.2	158.585292	127.2573	73.51818
0.3	149.541885	110.952297	73.21818
0.4	140.833062	102.098097	73.21818
0.5	132.668469	98.149203	73.21818
0.6	125.278938	96.471603	73.21818
0.7	118.912239	95.638797	73.21818
0.8	113.752584	95.145903	73.21818
0.9	109.813761	94.8186	73.21818
1	106.935885	94.586103	73.21818

plications that require high power efficiency and high gain performance, such as power amplifiers, RF transmitters, and switching power supplies.
Figure 5 exhibits g_{DS}/I_D of the structure with respect to V_{DS} for different V_{GS}. This figure indicates that higher g_{DS}/I_D is achieved for low values of V_{DS}. Moreover, it is observed that higher value of g_{DS}/I_D exhibits for increasing V_{GS}. Therefore, lower value of V_{DS} is suitable for better performance. Variations of g_{DS}/I_D of this structure for values of t_{BOX} and t_f are analyses with respect to V_{DS} in Fig. 6 and Fig. 7 . Both figures indicates that the structure exhibits higher values of Drain-conductance-to-drain-current-ratio for 50 nm thickness of buried-oxide layer and 10 nm of thickness of gate dielectrics at lower values of V_{DS}. A higher value of Drain-conductance-to-drain-current-ratio is used for high gain performance. There, for this purpose t_{BOX} = 50 nm and t_f = 10 nm are appropriate in structure
Additionally, variations of Drain-conductance-to-drain-current-ratio for various values of N_D are analyses with respect V_{DS} in Figure 8 . A higher value of Drain-conductance-to-drain-current-ratio is obtained for higher doping concentrations for this structure at lower values of V_{DS}.
Figure 9 analyses variation of Drain-conductance-to-drain-current-ratio of this structure with respect to V_{DS} for values of different gate dielectric. This figure indicates that higher Drain-conductance-to-drain-current-ratio is obtained for lower values of gate dielectric i.e. at ε_{ox} = 3.97 (SiO_2).
A brief comparative analysis is carried out for drain conductance based on the simulation, which are presented in tabular form in Table 2 . Subsequently, conductance to current ratio is compared in Table 3 and subthreshold swing in Table 4 .

5. Conclusion

A comparative investigation shows that the buried oxide layer in the current structure results in a 51% drop in subthreshold swing and a 42% improvement in drain conductance to current ratio at moderate drain bias. The subthreshold swing's magnitude is extremely near to the optimum limit, yet the simulation's size and external parameters are kept within a workable range, as shown by earlier published research as well. TCAD software is used to verify these at the same time. Because of the device's continuous subthreshold swing over the whole bias spectrum, the estimated dimensional optimisation set is designed to use it for analogue amplifier applications where the applied bias may be tuned from a low to a moderate range.

Ethical Approval
This manuscript does not report on or involve the use of any animal or human data or tissue. So the ethical approval is not applicable.

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Availability of Data and Materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of Interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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