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ORIGINAL ARTICLE

Simulation for a low-energy ternary multiplier cell based on Graphene nanoribbon field-effect transistor

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Abstract

The multiplier circuit is considered to be a significant component of larger circuits, such as the arithmetic and logic unit (ALU), and it is crucial to enhance its energy efficiency. This objective can be easily achieved by utilizing graphene nanoribbon field-effect transistor (GNRFET) devices and adopting ternary logic. Ternary circuit designs demonstrate superior energy efficiency and occupy less space compared to binary ones. The adjustability of the threshold voltage (V_{th}) in GNRFET devices is directly influenced by the width of the graphene nanoribbon (GNR). This offers significant advantages for ternary circuit designs. This paper presents a 24-transistor low-energy GNRFET-based single-trit ternary multiplier. Our proposed design incorporates an enhanced voltage division technique to achieve logic '1' while minimizing power consumption. The primary design approach employed in our design involves the utilization of unary operators and specialized transistor configurations to reduce the number of transistors and shorten the critical path. We used the Hewlett simulation program with integrated circuit emphasis (HSPICE) and GNRFET technology with a 32-nm channel length operating at 0.9 V and 300˚ K to evaluate the efficiency of our circuit. We then compared it with similar existing ternary multiplier circuits. The suggested circuit displays favorable delay and power consumption characteristics and ranks as the second most optimal design in terms of energy efficiency. Furthermore, it improves the energy-delay-product by at least 2.80%.

Keywords: *Delay; Digital Circuit; Graphene Nanoribbon Field-Effect Transistor (GNRFET); Low-Energy; Multiplier; Ternary Logic.*

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INTRODUCTION

The advent of semiconductor device miniaturization has significantly propelled the evolution of the electronics industry. Its primary goal is to improve the speed, affordability, power efficiency, and overall effectiveness of transistors [1]. According to the predictions made by researcher Gordon Moore, the number of transistors on a chip doubles every two years [2]. Complementary metal-oxide-semiconductor (CMOS) devices have become the foundation of very-large-scale-integrated (VLSI) circuits due to transistor downsizing, and they have continuously been scaled down to less than 32 nanometers [1]. However, this continuous size reduction has led to detrimental challenges such as short-channel issues, decreased threshold voltage (V_{th}), increased leakage power, degraded on-to-off currents ratio (I_{on}/I_{off}), boron or other light atoms diffusion through an ultrathin gate dielectric film, sample surface morphology, and degradation of the gate oxide, resulting in a decline in Si transistor performance [3-7]. Consequently, researchers have started to examine and evaluate potential alternatives to Si material.

Graphene is a single layer of graphite with a hexagonal atomic lattice. This unique atomic structure of graphene leads to the absence of an energy gap between its conducting and valence bands, thus giving it metallic properties. Due to its exceptional mobility, high carrier velocity for

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fast switching, and efficient thermal conductivity, graphene has attracted significant attention in the field of nanoelectronics [8, 9].

With the advent of graphene technology, there have been substantial advancements in using graphene as a channel material in transistors. However, the absence of an energy gap in graphene results in transistors constructed with it displaying significantly low I_{on}/I_{off} [3]. While this may not pose a significant concern for analog circuits, it presents a considerable challenge for digital applications [10]. One potential solution to this issue involves creating an energy gap by forming one-dimensional graphene nanoribbons (GNRs). Theoretical calculations and experimental evidence suggest that the energy gap of GNRs is directly related to their width, and reducing the width to less than 10 nanometers is crucial for achieving satisfactory transistor performance at room temperature [8].

Based on the edge configuration, GNRs can be categorized into two distinct types: 1) Armchair-edged GNR (AGNR) and 2) Zigzag-edged GNR (ZGNR), as depicted in Fig.1 [4].

The GNRFET is a type of transistor that incorporates GNR as the channel material. There are two classifications of GNRFET: The Schottky barrier (SB) and the metal-oxide-semiconductor (MOS) types. The present investigation exclusively employs the MOS variant due to its commendable attributes including a high I_{on}/I_{off} ratio, superior overall performance, and the low electrical resistance connections at source and drain terminals [8]. This particular transistor not only showcases superior scalability in comparison to CNTFETs, but also overcomes the challenges associated with chirality [3, 11]. Unlike cylindrical carbon nanotubes, GNRFETs can be synthesized in situ through a silicon-compatible process, thereby eliminating the issues related to misalignment encountered in CNTFETs [8]. GNRFETs exhibit low heat dissipation, offer higher carrier mobility, possess a large current-carrying capability, and demonstrate thermal stability. The graphene component contributes to these remarkable properties, making GNRFETs lightweight, robust, with a high switching speed and excellent thermal conductivity [1].

The incorporation of nanotechnology components in conjunction with multi-valued logic (MVL) holds significant potential for enhancing modern VLSI designs [1]. MVL design offers the capability to increase value and data transferability, making it a viable alternative to traditional binary logic-driven design [12]. Among the various forms of MVL designs, the integration of ternary logic has demonstrated success in reducing both the area and initial connectivity complexity [13]. Furthermore, ternary functions exhibit superior speed compared to numerous serial and parallel arithmetic computations. For efficiency optimization, ternary circuits are commonly employed in binary logic integrated circuits [14]. Ternary systems are represented using two methodologies: a balanced approach ('1', '0', '-1') corresponding to (V_{DD}, 0, -V_{DD}), and an unbalanced approach ('2', '1', '0') corresponding to (V_{DD}, V_{DD}/2, 0) [13].

In the realm of designing MVL gates, a new approach involves utilizing GNRFET transistors. This technique takes advantage of a unique property of GNRFETs, where the V_{th} can be finely tuned by adjusting the width of the GNR and determining the appropriate number of dimer lines, N [3, 15]. The ability to precisely adjust the V_{th}, combined with the superior efficiency and lower power consumption of GNRFETs compared to CNTFET and metal-oxide-semiconductor field-effect transistor (MOSFET) devices, makes them highly suitable for future circuit applications [16].

Optimal multipliers hold significant importance in advanced digital processing systems as they serve as crucial components. Therefore, the ability to provide an optimal multiplier is regarded as a valuable advantage for the digital computing system [16]. Recently, different topologies of multiplier circuits designed and implemented using ternary-capable CNTFETs and GNRFETs have been proposed in the literature [5, 16-24]. The main drawback of the designs presented in [16-19, 22-24] is the use of two supplies, V_{DD} and V_{DD}/2, which increases circuit complexity and somewhat contradicts the primary purpose of MVL design. The design available in [21] consumes a high amount of power due to the conventional voltage division technique used in this circuit. An improved technique for voltage division to obtain logic '1' is used in [5, 20] to reduce power consumption; however, these designs employ 34 and 38 transistors, respectively. In this regard, we propose an energy-efficient multiplier circuit using GNRFET devices and ternary logic. The proposed circuit is designed and implemented using 24 transistors. Moreover, it reduces delay

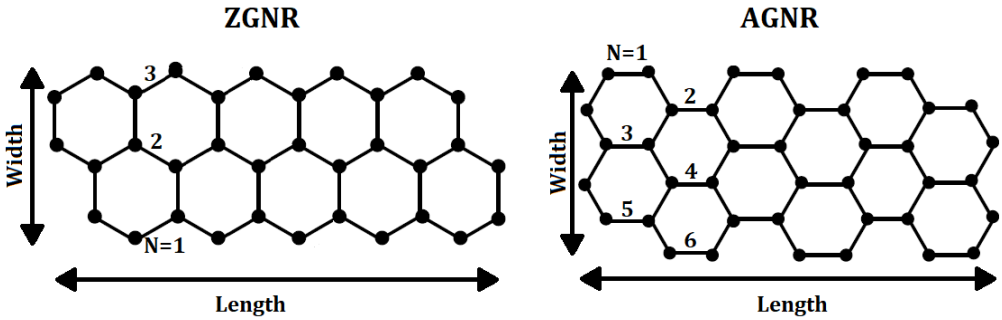

Fig. 1. Two distinct types of GNR; AGNR and ZGNR [4].

by shortening the critical path through special transistor arrangements and reduces power consumption by employing an improved version of the voltage division circuit to obtain logic '1'. The use of unary operators further enhances the performance of our design.

MATERIALS AND METHODS

Graphene Nanoribbon

As previously stated, graphene nanoribbon (GNR) exists in two distinct edge-shape variations, namely Zigzag GNR (ZGNR) and armchair GNR (AGNR). ZGNRs exhibit metallic properties, while AGNRs can display either metallic or semiconducting characteristics [8]. The width of AGNRs can be determined by calculating the dimer lines designated as N, using Eq. (1) [8].

$$W_{ch} = W_{AGNR} = 0.123 \times 10^{-9} \times (N-1) \quad (1)$$

The energy gap value in AGNRs is dependent on the parameter N. In the case of $N = 3p$ and $N = 3p+1$ (where p is a positive integer larger than 2), AGNRs display a finite energy gap value and demonstrate semiconductor characteristics. Conversely, for $N = 3p+2$, the energy gap value becomes extremely small, causing AGNRs to exhibit behavior akin to that of metals [9].

Graphene Nanoribbon Field-Effect Transistor; Device and Structure

The metal-oxide-semiconductor-type graphene nanoribbon field-effect transistor (MOS-GNRFET) employs armchair graphene nanoribbons (AGNRs) with n-i-n or p-i-p doping in its drain, channel, and source regions. Impurities are intentionally introduced to the source and drain terminals to establish a connection with the channel and create an energy barrier within the channel. By incorporating impurities, either acceptor or donor types, the MOS-GNRFET can be classified as n-type or p-type. In the n-type MOS-GNRFET, the predominant current is attributed to the transfer of electrons, whereas in the p-type MOS-GNRFET, it is due to the transfer of holes.

Fig. 2 depicts the configuration of a graphene nanoribbon field-effect transistor (GNRFET). The distance between AGNRs remains constant at a value of $2W_{sp}$. The gate, situated amidst the source/drain terminals, comprises heavily doped graphene nanoribbon (GNR) segments with a doping fraction of (f_{dop}) [8]. The doped areas, known as reservoirs, are characterized by a length equivalent to L_{res}, while the channel represents the intrinsic segment. The gate length is L_{gate}, and the gate dielectric material has a thickness denoted as T_{ox} [8]. The gate width, calculated using Eq. 2, is referred to as W_{gate}. In this equation, N_{AGNR} signifies the number of AGNRs located within the channel region [8].

$$W_{gate} = (W_{ch} + 2W_{sp}) \times n_{ribbon} \quad (2)$$

Multiple-Valued Logic

In the context of multiple-valued logic (MVL) systems, the adoption of ternary logic has gained significant popularity due to its simplicity and effectiveness. To implement this logic, diverse threshold voltage (V_{th}) values can be obtained by using graphene nanoribbons (GNR) with different widths. In the unbalanced-mode ternary logic, there are three logic levels represented by the symbols '0', '1', and '2', which correspond to voltage values 0, $V_{DD}/2$, and V_{DD}, respectively. Within ternary logic, three distinct types of logic inverters have been defined: negative ternary inverter (NTI), standard ternary inverter (STI), and positive ternary inverter (PTI). Table 1 presents the output values of ternary inverters [2].

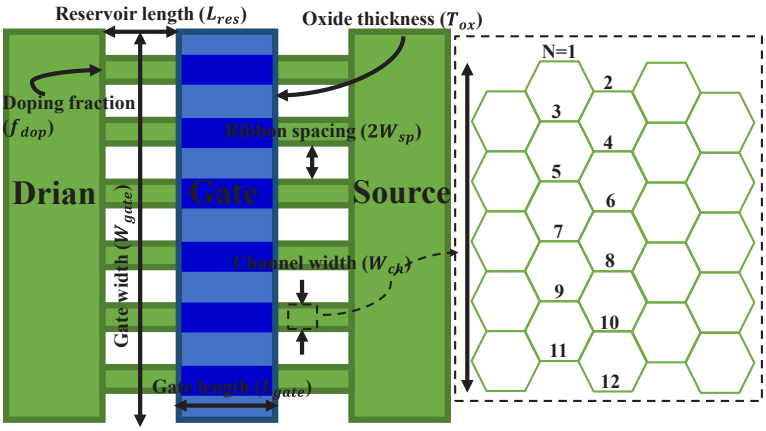

Fig. 2. An illustration of the MOS-GNRFET device [25].

Table 1. The outputs of three different types of the ternary inverters.

Input	Outputs		
F	NTI	PTI	STI
	F_N	F_P	$\bar{F}$
0	2	2	2
1	0	2	1
2	0	0	0

The determination of the V_{th} is a crucial aspect in ternary digital designs. While the V_{th} formula for carbo nanotube field-effect transistor (CNTFET) and metal-oxide-semiconductor field-effect transistor (MOSFET) is already established, there is currently no explicit expression available to evaluate the V_{th} values of MOS-GNRFET transistors based on the Hewlett simulation program with integrated circuit emphasis (HSPICE) parameters [3]. The conventional methodology is employed to obtain the V_{th} values. According to the definition, the V_{th} is obtained by plotting the current-voltage (*I-V*) curve. A significant gate-voltage (V_G) and a low source-drain voltage (V_{DS}) are applied to the n-type MOS-GNRFET transistor, and the slope of the *I-V* curve at the point where it intersects with the V_G axis determines the V_{th} [3]. The V_{th} remains constant for both n- and p-types MOS-GNRFET transistors [3]. In accordance with [25], the absolute values of the V_{th} for a 32-nm channel MOS-GNRFET device at V_{DD} = 0.9 V are 0.6 V and 0.24 V for dimer values N = 7 and 9, respectively.

The diagrams depicted in Figs. 3(a), 3(b), and 3(c) exhibit instances of MOS-GNRFET-based NTI, PTI, and STI circuit implementations, respectively. [25], which are utilized in the creation of the suggested multiplier circuit design. The working of these circuits is as follows:

In Fig 3(a), when *F* is '0', T1 and T2 are turned on and off, respectively. Then, F_N becomes '2'. When *F* becomes '1' or '2', T1 and T2 are off and on, respectively, connecting F_N to ground ('0').

In fig 3(b), when *F* is '0' or '1', T1 is switched on and T2 is disabled. Then, F_P will be equal to '2'. When *F* becomes '2', T1 and T2 are switched off and on, respectively, forcing F_P to zero potential (logic '0').

In Fig 3(c), when *F* is '0', T1 and T3 are switched on and T2 and T6 are disabled, which makes $\bar{F}$ equal to '2'. When *F* becomes '1', T3 and T6 are switched on, T1 and T2 are off, and T4 and T5 act as a diode-connected load. This makes $\bar{F}$ to be placed at an intermediate voltage level, i.e. '1'. Finally, when *F* is equal to '2', T2 and T6 are switched on and T1 and T3 are off, which makes $\bar{F}$ equal to '0'.

Proposed GNRFET-based Single-Trit Ternary Multiplier Cell

A single-trit ternary multiplier (TMUL) is a circuit that takes two inputs, *A* and *B*, and produces two outputs called *Carry* and *Product*. Its purpose is to perform multiplication operations on ternary

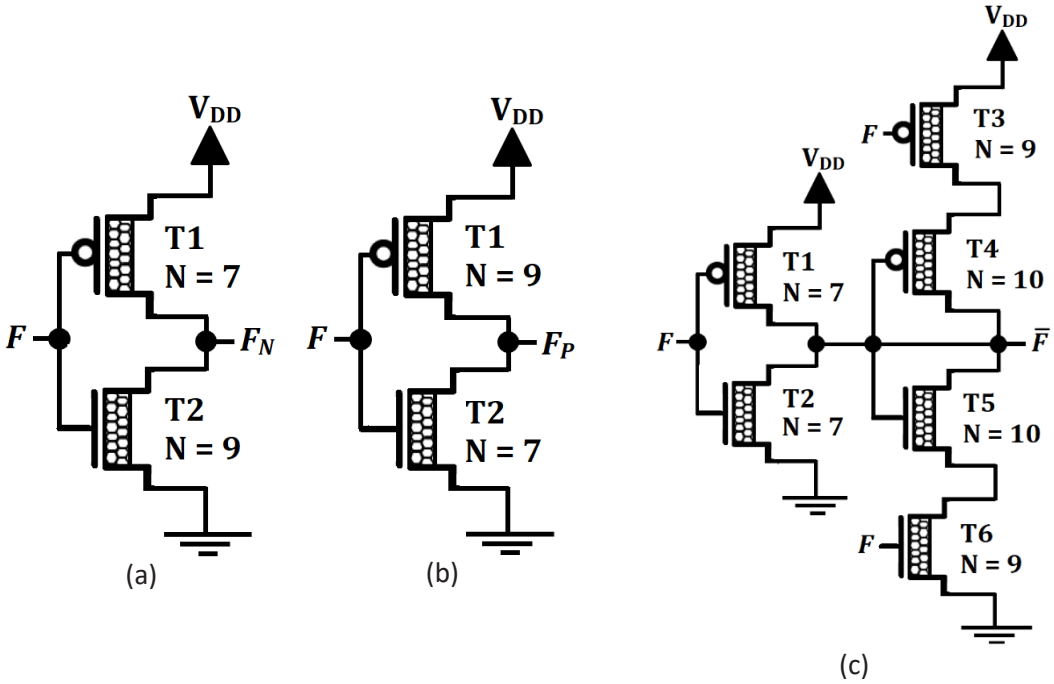

Fig. 3. GNRFET-based design of (a) NTI, (b) PTI, and (c) STI [26].

Table 2. The truth table of the single-trite TMUL cell.

Product			
A/*B*	*B* (0)	*B* (1)	*B* (2)
A (0)	0	0	0
A (1)	0	1	2
A (2)	0	2	1
Carry			
A/*B*	*B* (0)	*B* (1)	*B* (2)
A (0)	0	0	0
A (1)	0	0	0
A (2)	0	0	1

inputs. In Table 2, you can find the truth table for the single-trit TMUL cell. From this table, it can be observed that *Carry* is '1' for the first eight combinations of inputs and is '1' only when both *A* and *B* are '2'. On the other hand, *Product* is '0' when either *A* or *B*, or both, are '0'. It becomes '1' when both *A* and *B* are '2' or '1', and it becomes '2' when one input (*A* or *B*) is '1' and the other one is '2'. Based on these conditions, we have designed and implemented the proposed single-trit TMUL cell using MOS-GNRFETs.

Fig. 4 depicts the schematic diagram of the proposed single-trit TMUL cell based on MOS-GNRFETs. This circuit utilizes 24 MOS-GNRFETs in its design. The circuit operates according to the following principles.

For *Carry* output circuit, depicted in Fig. 4(a), we can state:

· When *A* = '0' or '1', A_p becomes '2', which turns on T1. This makes *Carry* low ('0').

· When *B* = '0' or '1', B_p becomes '2', which turns on T2. This makes *Carry* low ('0').

· When *A* = *B* = '2', A_p and B_p become '0', which turns on T3-T6. In this situation, T4 and T5 act as resistors for performing a voltage division. Finally, *Carry* becomes '1'. The on-state n-type transistor (T4) in the pull-up network and the on-state p-type transistor (T5) in the pull-down network are unable to pass strong logic '2' and '0', respectively, resulting in I_{on} reduction and power saving.

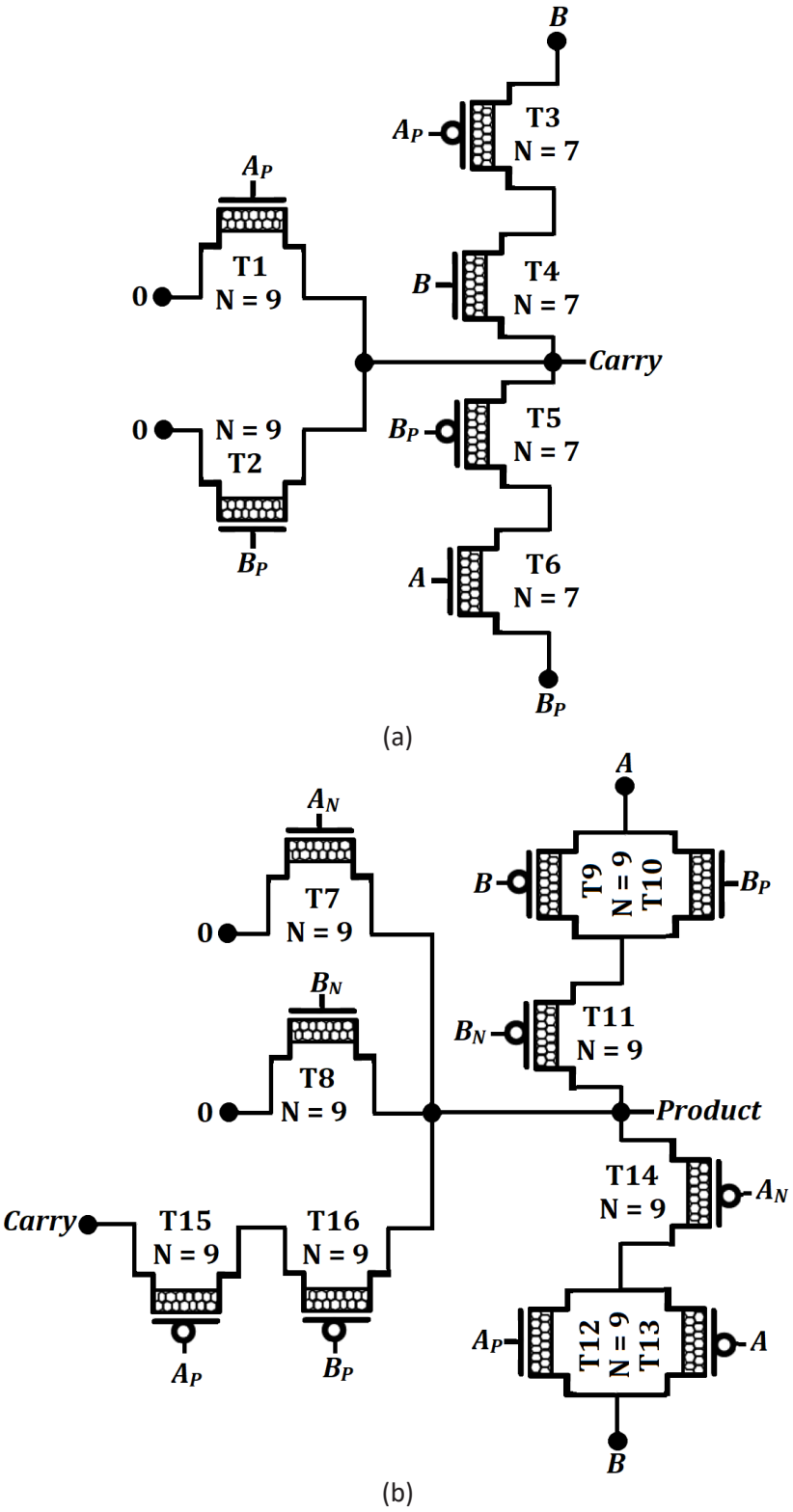

Fig. 4. GNRFET-based design of the proposed TMUL cell. (a) *Carry* and (b) *Product*.

For *Product* output circuit, depicted in Fig. 4(b), we can state:

· When A = '0', A_N becomes '2', which turns on T7. This makes *Product* low ('0').

· When B = '0', B_N becomes '2', which turns on T8. This makes *Product* low ('0').

· When B = '1', B_N and B_P become '0' and '2', respectively, which turns on T9-T11. This transmits A to *Product* to have the same logical values.

· When A = '1', A_N and A_P become '0' and '2', respectively, which turns on T12-T14. This transmits B to *Product* to have the same logical values.

· When A = B = '2', A_P and B_P become '0', which turns on T15-T16. This transmits *Carry* to *Product* to have the same logical value.

Simulation Program

The work utilizes the Hewlett simulation program with integrated circuit emphasis (HSPICE) software to simulate the proposed TMUL and investigated circuits. HSPICE is electronic design automation (EDA) software developed by Synopsys, Inc., a prominent industry player. Synopsys specializes in offering a diverse range of software tools and solutions for electronic system design, verification, and manufacturing processes [26].

HSPICE is widely used for simulating and analyzing electronic circuits. Its main focus is on simulating and evaluating integrated circuits, including analog, digital, and mixed-signal configurations. By using HSPICE, designers can accurately model and simulate circuit behavior, considering important factors such as voltage levels, current flow, and timing characteristics. This software tool covers various circuit parameters, including resistors, capacitors, inductors, transistors, and other components. Through simulations conducted with HSPICE, designers can evaluate the functionality and performance of their integrated circuit designs before fabrication [26].

In addition to its simulation capabilities, HSPICE provides features for detailed analysis, optimization, and detection of potential issues or flaws in circuit designs. It has a user-friendly interface and supports the industry-standard simulation program with integrated circuit emphasis (SPICE) netlist format.

Regarding modeling capabilities, HSPICE incorporates different circuit models to accurately replicate the behavior of integrated circuits. These models include transistor-level representations, such as the widely used Berkeley Short-Channel IGFET Model (BSIM) for simulating the behavior of metal-oxide-semiconductor field-effect transistor (MOSFET) components [26].

RESULTS AND DISCUSSIONS

Simulation-Setup

The suggested metal-oxide-semiconductor-type graphene nanoribbon field-effect transistor (MOS-GNRFET)-based single-trit ternary multiplier (TMUL) cell (G-TMUL) is simulated using the Synopsis Hewlett simulation program with integrated circuit emphasis (HSPICE) software. The MOS-GNRFET SPICE model presented in [8] is utilized for the implementation of the proposed TMUL and other investigated TMUL circuits. This model enables the development of precise and circuit-compatible MOS-GNRFET devices. Additionally, it incorporates a comprehensive transcapacitance electronic circuit to achieve high performance. Table 3 presents the characteristics of the technology model employed for these

Table 3. key characteristics of the MOS-GNRFET technology model [8].

Parameter	Description	Value
V_{DD}	Supply	0.9 V
Temp.	Temperature	300 ķelvin
L_{gate}	Gate Length	32 nm
T_{ox}	Gate Oxide Thickness	1 nm
N	GNR Dimer line	7 and 9
$2W_{sp}$	Gap between two GNRs	2 nm
n_{ribbon}	GNR count	3
K_{gate}	Permittivity (HfO_2)	4
f_{dop}	Doping fractions	0.001
P_r	Line-edge-roughness %	0

simulations.

To ensure a fair comparison, the proposed G-TMUL was evaluated against other TMUL circuits based on carbon nanotube field-effect transistors (CNTFETs) or GNRFETs that have been reported in the literature [5, 16-18, 20, 21]. These comparison TMUL circuits were re-simulated under identical conditions, including a 0.9 V supply voltage, a temperature of 300˚ K, 20 ps fall time, 20 ps rise time, a frequency of 1 GHz, and a fan-out of four ternary inverters (FO4) as output loads. Moreover, the chirality vectors or dimer lines numbers used for the comparison TMUL circuits were consistent with those mentioned in their corresponding original proposals [5, 16-18, 20, 21].

The key performance parameters considered include propagation delay, average power consumption, power-delay-product (PDP), energy-delay-product (EDP), and component count. The worst-case delay is calculated for different output transitions of the available outputs. Power consumption is measured using random input patterns at an operating frequency of 1 GHz. PDP is obtained by multiplying the average power consumption and the maximum propagation delay, serving as a trade-off factor for overall performance evaluation. EDP, on the other hand, is obtained by multiplying PDP and the maximum propagation delay, providing another metric for assessing the overall performance of the design.

Proposed Design's Efficiency Investigation

Fig. 5 displays the output of the recommended G-TMUL when operated at a supply voltage of 0.9 V, temperature of 300˚ K, 20 ps fall time, and 20 ps rise time, a frequency of 1 GHz, and an FO4 as output load. The graph illustrates that the proposed design functions effectively without any flaws. Through simulation, the delay, power consumption, and PDP have been computed, resulting in values of 24.7 ps, 0.17 µW, and 4.20 aJ, respectively.

Assessing the impact of process, voltage, and temperature (PVT) fluctuations on very large-scale integration (VLSI) circuits is crucial as it determines their level of sensitivity and helps identify the optimal configuration for specific purposes [27]. Hence, it is important to evaluate the performance of the proposed TMUL design under varying PVT conditions to understand its behavior in such scenarios. The variables to be changed encompass supply voltage (V_{DD}), temperature, output load, oxide thickness (T_{ox}), and channel length (L_{ch}).

To examine the influence of varying V_{DD} on the performance metrics of the suggested design, the simulations have been replicated for three distinct V_{DD} values: 0.8, 0.9, and 1 V. The variation of delay, power, and PDP with V_{DD} is depicted in Fig. 6. As the V_{DD} is raised in MOS-GNRFET-based circuits, it is expected that the power consumption would increase while the delay would decrease. This

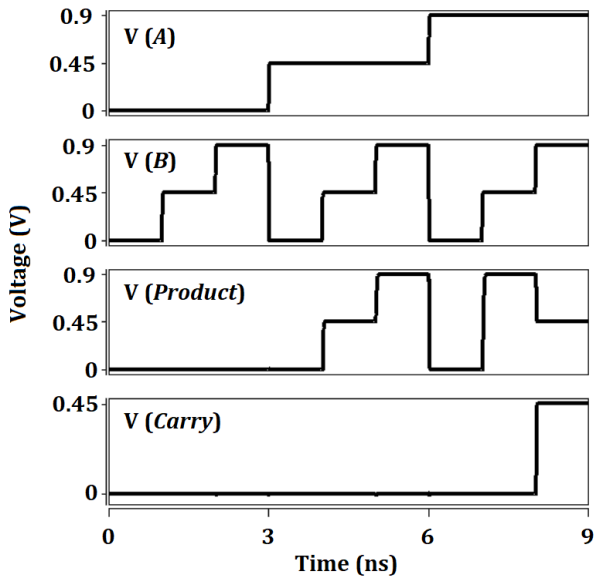

Fig. 5. Output of the proposed G-TMUL at V_{DD} = 0.9 V, temperature of 300˚ K, 20 ps fall time, 20 ps rise time, a frequency of 1 GHz, and an FO4 as output load.

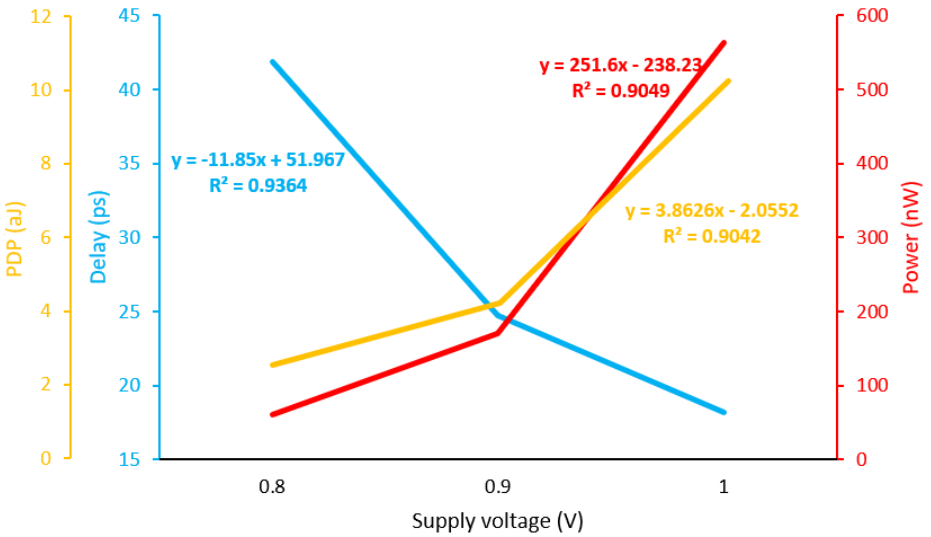

Fig. 6. Effect of V_{DD} variation on the performance of G-TMUL circuit (delay, power, and PDP).

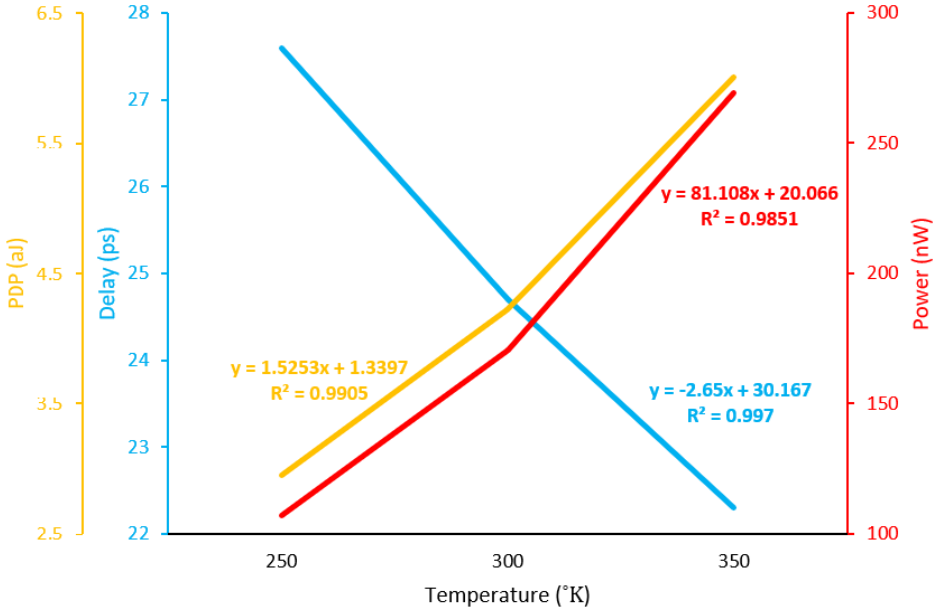

Fig. 7. Effect of temperature change on the performance G-TMUL circuit (delay, power, and PDP).

phenomenon can be observed in the designs. The increase in power consumption is attributed to the augmented dynamic power, which exhibits a square relationship with the V_{DD}. On the other hand, the delay reduces owing to the amplified drain current, facilitating faster node charging and discharging, resulting in expedited switching and reduced delay. The proposed design exhibits an enhancement in the overall performance metric, namely PDP, when the V_{DD} is increased. Consequently, it is commonly recommended to minimize V_{DD} as a means to reduce PDP or energy consumption. Each of the curves represented in Fig. 6 displays a linear function (y = ax ± by) accompanied by a correlation coefficient (R^2). It is noteworthy that 93.64%, 90.49%, and 90.42% of the variation in the delay, power consumption, and PDP values is accounted for by the V_{DD} values, respectively.

The TMUL circuit under investigation is subjected to simulations at three distinct temperature settings: 250 ˚K, 300 ˚K, and 350 ˚K.

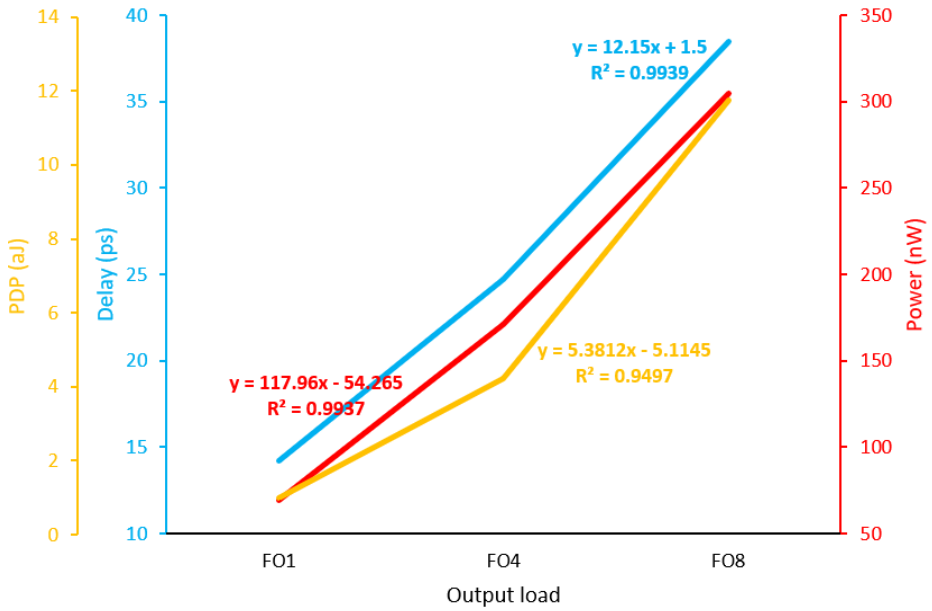

Fig. 8. Effect of output load variation on the performance G-TMUL circuit (delay, power, and PDP).

The purpose of these simulations is to examine how alterations in temperature affect the efficiency of the proposed design. Fig. 7 illustrates the relationship between temperature changes and the corresponding variations in delay, power consumption, and PDP. It is worth noting that as the temperature increases, thermally generated electrons are introduced into the conducting channel of the MOS-GNRFET. Consequently, the rise in temperature leads to a reduction in delay and an increase in power consumption within the design. However, the PDP exhibits an upward trend with increasing temperatures. Based on the R^2 values shown for each curve in Fig. 7, it can be concluded that 99.7%, 98.51%, and 99.05% of the variation in the delay, power consumption, and PDP values can be explained by the temperature values, respectively.

The performance of the suggested TMUL circuit is assessed with three different output loads: FO1, FO4, and FO8. In Fig. 8, the variation in delay, power consumption, and PDP of the proposed G-TMUL cell is shown in relation to changes in the output load. As the output load increases, all performance metrics of the design also increase. This is because increasing the output load capacitance will cause a slower rise and fall time for the output signal. This is because the increased capacitance will require more time to charge and discharge, resulting in a slower transition between logic levels. Additionally, increasing the load capacitance can also increase power consumption and reduce switching speed. For instance, when FO8 is used as the load, the delay, power consumption, and PDP become 1.56, 1.79, and 2.78 times higher, respectively, compared to the FO4 output load. Based on the R^2 values for each curve depicted in Fig. 8, it can be deduced that 99.39%, 99.37%, and 94.97% of the variance in the delay, power consumption, and PDP values, respectively, can be accounted for by the associated temperature values.

Fig. 9 demonstrates the impact of changes in oxide thickness (T_{ox}) on the efficiency of our design. As T_{ox} increases, the on-current (I_{on}) of the transistor decreases [4]. Consequently, this results in an increase in delay, as portrayed in Fig. 9. Hence, there exists a direct correlation between the rise in T_{ox} and the subsequent increase in delay. Thicker oxide layers possess greater capacitance and enhanced resistance. Consequently, this leads to a reduction in leakage current, thereby improving the power efficiency of the transistor. As a result, as depicted in Fig. 9, power consumption decreases with an increase in T_{ox}. However, the power-delay product (PDP) will increase with a rise in T_{ox}, as illustrated in Fig. 9. Based on the R^2 values for each curve depicted in Fig. 9, it can be deduced that 99.73%, 97.79%, and 97.15% of the variance in the delay, power consumption, and

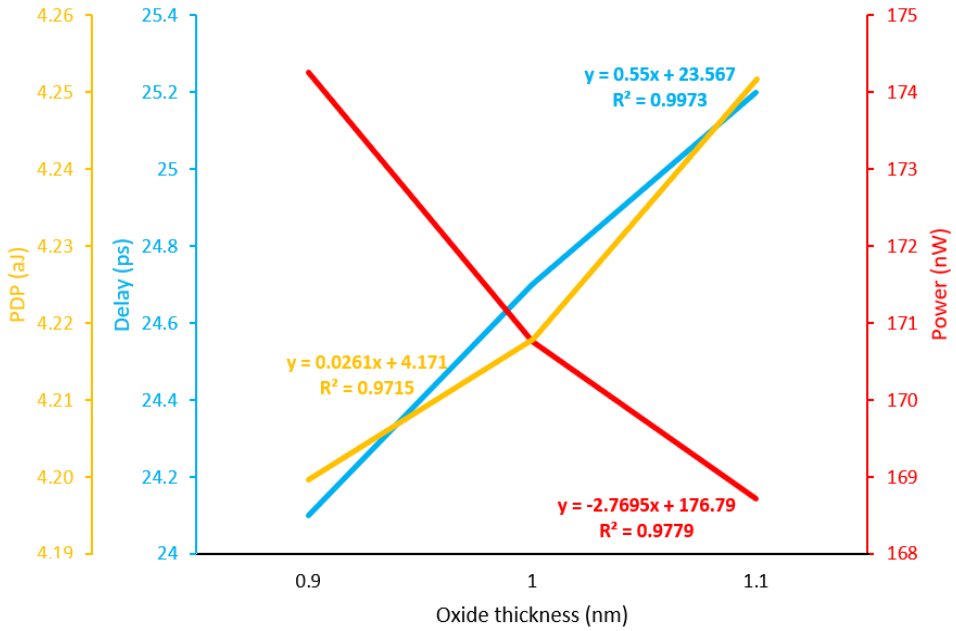

Fig. 9. Effect of T_{ox} change on the performance G-TMUL circuit (delay, power, and PDP).

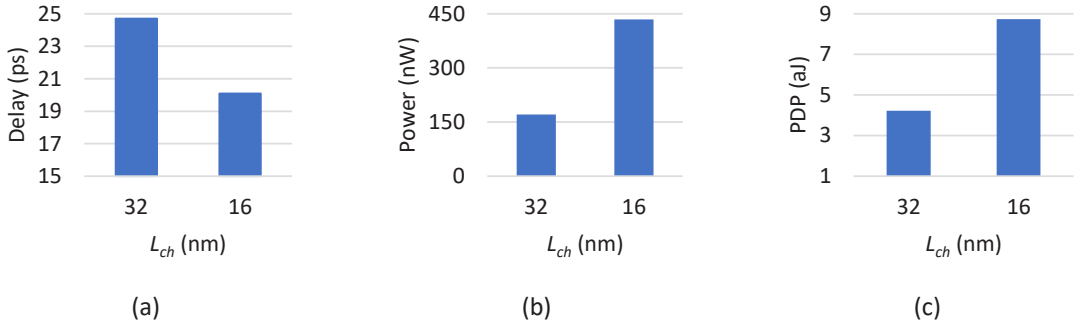

Fig. 10. Effect of L_{ch} change on the performance G-TMUL circuit. (a) delay, (b) power, and (c) PDP.

PDP values, respectively, can be accounted for by the associated temperature values.

Fig. 10 showcases the influence of channel length (L_{ch}). As L_{ch} decreases, the gate capacitance also decreases [18], resulting in a reduction in delay, as indicated in Fig. 10(a). Alternatively, as demonstrated in figs. 10(b) and (c), the proposed design exhibits higher power and energy consumption at smaller L_{ch} values.

PERFORMANCE COMPARISON

To gain a more comprehensive understanding of the advantages of our design, various feature metrics including published year, technology node, transistor technology, number of supply voltages, and transistor count are compared to recently published CNTFET- or GNRFET TMUL circuits. This thorough comparison can be found in Table 4. From a careful examination of Table 4, it is evident that all the analyzed TMUL circuits have been designed and implemented utilizing the 32-nm process node. Notably, the designs in [21], employ CNTFET technology, while the proposed circuit and the designs in and [18] utilize GNRFET technology. The design approach employed for the design in [21] is a combination of ternary multiplexer and unary operators. This is design employs voltage division technique to get logic '1'. In [5], the design utilizes a ternary multiplexer to generate the *Carry* output. Additionally, a combination of numerous transmission gates (TGs), either alone or connected in series, is employed as switching

Table 4. A feature comparison between the proposed G-TMUL and existing TMUL circuits.

TMUL Designs	Published year	Process node	Transistor type	No. of Transistors	No. of supply voltages
[21]	2016	32 nm	CNTFET	26	1
[5]	2017	32 nm	CNTFET	34	1
[20]	2020	32 nm	CNTFET	38	1
[17]	2023	32 nm	CNTFET	23	2
[18]	2023	32 nm	GNRFET	26	2
[16]	2023	32 nm	GNRFET	22	2
Proposed	2024	32 nm	GNRFET	24	1

Table 5. A performance comparison between the proposed G-TMUL and existing TMUL circuits at V_{DD} = 0.9 V.

Designs	Delay (ps)	Power (μW)	PDP (aJ)	EDP (E-28 Js)
[21]	20.4	35.34	720.97	147.08
[20]	17	3.18	54.11	9.20
[5]	17.3	2.14	37.01	6.40
[17]	19.4	1.93	37.44	7.26
[18]	26.7	0.15	4.01	1.07
[16]	27.7	0.17	4.71	1.30
Prop. G-TMUL	24.7	0.17	4.20	1.04

access to generate the *Product* output. To achieve logic '1' in this design, a voltage division is provided at the output node. Authors in [20] have used a new approach to design a TMUL circuit, which is based on a combination of unary operators, TG, pass transistors, and a modified version of voltage division technique. The TMUL designs presented in [17] have used a power supply voltage of $V_{DD}/2$ to get directly logic '1'. This eliminates any connections between high to low levels of voltage during the circuit operation, thereby, improving power/energy efficiency. The main design approach considered for these designs is to combine unary operators, pass transistors, and TGs. The proposed TMUL circuit benefits from the use of an improved version of voltage division technique and the use of pass transistor and TGs, along with acceptable transistor count. It is concluded from Table 4 that the proposed TMUL circuit reduces transistor count by 7.69%, 29.41%, 36.84%, and 7.69% compared to the designs presented in [21], respectively, and only employs one and two additional transistors in comparison with the designs proposed in [17], respectively.

The performance metrics of the proposed TMUL circuit, including delay, power, PDP and EDP, are compared to recently published CNTFET- or GNRFET TMUL circuits. This thorough comparison can be found in Table 5. As indicated in Table 5, CNTFET-based designs exhibit lower delay compared to GNRFET-based designs due to their higher on current (I_{on}). However, they do not demonstrate high power efficiency. Additional information regarding this can be found in [18]. The CNTFET-based TMUL circuit presented in [21] consumes the highest amount of power due to the presence of multiple direct paths from high to low voltage levels. This occurs as a result of voltage division required to achieve logic '1'. The use of a ternary multiplexer in this design to generate *Carry* and *Product* outputs leads to increased delay compared to the CNTFET designs mentioned in [5, 17, 20]. The CNTFET TMULs designed and presented in [5, 20] employ an improved version of the voltage division technique to reduce power consumption. While these circuits have comparable delay, the design in [5] consumes a lower amount of power than [20], due to its lower transistor count. In the CNTFET-based TMUL circuit proposed in [17], the logic '1' is acquired directly from the supply voltage $V_{DD}/2$ component. This eliminates any current flowing from high to low voltages, resulting in power savings. Therefore, the design in [17] exhibits lower power consumption

compared to [5, 20, 21]. However, it has higher delay than those of [5, 20] due to its longer critical path. The use of the $V_{DD}/2$ component also increases the complexity of this circuit.

Among the GNRFET-based TMUL circuits, the proposed design exhibits the lowest delay as its critical path is shorter than [16, 18]. The designs presented in [16, 18] employ a dual-V_{DD} technique to improve power efficiency, whereas our proposed design utilizes the voltage division technique to obtain logic '1'. This is why the proposed design consumes more power than [18] but is comparable to [16]. However, compared to [16, 18], our suggested G-TMUL circuit has lower complexity.

From Table 5, it can be observed that the PDP of the proposed design is reduced by 99.42%, 92.24%, 88.65%, 88.78%, and 10.83% compared to the designs in [21], respectively. Furthermore, our suggested G-TMUL cell improves EDP by 99.29%, 88.70%, 83.75%, 85.67%, and 20% when compared to the designs in [21], respectively.

Although our design exhibits 1.05 times higher PDP compared to the design in [18], the suggested circuit offers a 2.80% improvement in EDP, along with a 7.69% reduction in transistor count and low complexity.

CONCLUSION

This paper presents a ternary multiplier circuit based on metal-oxide-semiconductor-type graphene nanoribbon field-effect transistor (MOS-GNRFET) technology, which offers a high level of energy efficiency. The proposed circuit is designed using unary operators, carefully configured transistors, and an improved voltage division technique to achieve logic '1'. The simulations were conducted using the Hewlett simulation program with integrated circuit emphasis (HSPICE) software, featuring 32-nm MOS-GNRFET technology with a supply voltage of 0.9 V and a temperature of 300˚ K. The simulation results demonstrate that the proposed design exhibits lower delay and comparable power consumption compared to previous MOS-GNRFET-based designs. However, when compared to existing designs based on carbon nanotube field-effect transistors (CNTFET), our design shows higher delay but significantly lower power consumption. In terms of energy consumption, the proposed design is ranked as the second-best design.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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