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ORIGINAL ARTICLE

Novel robust quantum-dot cellular automata (QCA) full adder in the one-dimensional clock

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Abstract

Quantum-dot cellular automata technology has emerged as an alternative for complementary metal oxide semiconductor technology in very-large-scale integration (VLSI) circuits. The basis and structure of QCA technology are different from CMOS technology, and it is necessary to redesign the existing circuits based on the characteristics of QCA technology. In this paper, first, five-input and three-input majority gates are proposed with the ability to work in the one-dimensional clock. Then a full adder based on the proposed majority gates in the one-dimensional clock was designed with 0.75 clock cycle latency. As a consequence of the location of the circuit's inputs & outputs, this full adder can easily be converted to a multi-bit adder. This paper introduces a four-bit adder utilizing the same method, endeavoring to design the circuit compliant with the inherent features of QCA technology and prove that the proposed circuit can be constructed. For design as well as manufacturing process simplicity, a general framework for design (in one-dimensional clock) is also hereby proposed. Proposed designs are confirmed by QCADesigner, a well-known QCA layout design and verification tool, and QCADesigner-E for power analysis.

Keywords: *Five-Input Majority Gate; Full Adder; Majority; QCA; QCA Designer E; RCA Adder; 1-d Clocking; 4-bit adder.*

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INTRODUCTION

As transistors shrink in size and reach physical limits, the need for alternative technology for transistors is increased. QCA is an alternative technology for transistor-based circuits. QCA technology, capable of clocking in the terahertz range, can also transmit data without transmitting current [1-2]. In addition to its silicon-based structure, it also can implement molecularly and magnetically [3-4]. Due to the capabilities of QCA technology in digital circuits and the fundamental differences between this technology and transistor-based technology, it is essential to design a suitable circuit with this technology. One of the basic blocks in VLSI is the full adder, and the optimal design for a full adder can increase the efficiency and speed of the circuit. Many full adders have been proposed. In most of these designs, the designer's goal has been to reduce latency and the number of used cells [5-8]. While attention to clock schematic and suitable inputs and outputs, placement was less considered in previous papers. The full adder proposed in [9] has a low circuit area, but the inputs are in different layers, making it difficult to use in a larger circuit. Also, the clock design method is unsuitable for the one-dimensional clock. The full adder proposed in [10] has suitable inputs and outputs placement, but clock arrangement is undisciplined and unsuitable for use in the one-dimensional clock. The full adder (introduced in [11]), even though

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capable of becoming a subtractor, complicates the achievement of a multi-bit adder or larger design due to the poor location of the inputs and, moreover, lacks the ability for implantation in a one-dimensional clock. However, the full adders (introduced in [12-13]) have fewer cells and less occupied area but do not have the possibility to achieve inputs and outputs in the same layer. They furthermore do not have implantation capability in a one-dimensional clock.

First, this paper introduced a three-input and five-input majority gate capable of working in the one-dimensional clock. Next, utilizing the five-input majority gate, a full adder capable of working in the one-dimensional clock was provided. The following is a four-bit RCAadder capable of working in the one-dimensional clock. Section 3 describes the simulation and the results, and the next is devoted to the conclusion.

MATERIALS AND METHODS

Each QCA cell consists of 4 quantum dots and 2 electrons. The arrangement of the electrons inside the cell's dot creates two states, one of which, as p = + 1, represents the value of the logical one shown in Fig. 1 (a), and the other case is considered p = -1 and Fig. 1 (b) represents a logical zero. QCA wire is made by placing the cells next to each other, as shown in Fig. 1 (c). Since the electron does not move between cells, the state of each cell is determined by the adjacent cell. The state of each cell is affected by the coulombic force between the electrons; therefore, no current is transmitted during data transfer between cells.

In this paper, the four-phase clock method is used. The four-phase clock consists of four modes: switch, hold, release and relax. Each mode and barrier potential change are shown in Fig. 2. This clock model ensures the propagation of information in the correct direction in the circuit [14].

The clock is applied to the cells by wires with the electromagnetic field. The QCA cells are instantiated in a bed that can be referred to as the QCA bed. This QCA bed rests on a surface consisting of several clock wires, as shown in Fig.

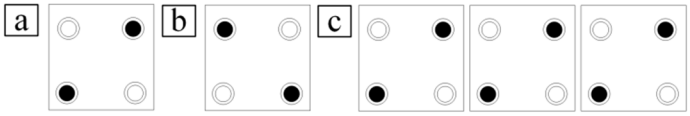

Fig. 1. a) p=+1, b) cell with p=-1, c) QCA wire.

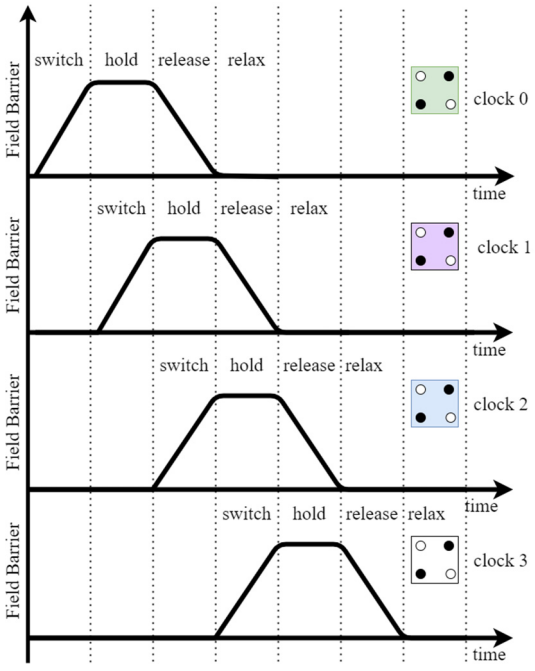

Fig.2. Four-phase clock.

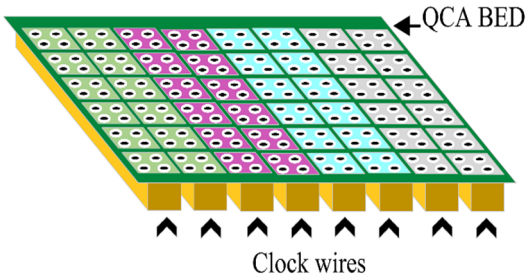

Fig. 3. QCA bed and clock wire.

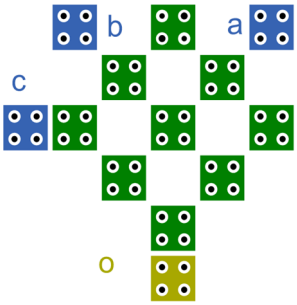

Fig. 4. Proposed three-input Majority Gate.

3. Clock wires are placed perpendicular to the clock path. If we consider the course of the wires in the direction of X Cartesian coordinates, Y will be the path of the clock in the circuit, and Z will be the direction of the field

The arrangement of clock wires and how to apply the field has different methods that can be generally divided into two categories: The one-dimensional clock and the two-dimensional clock [15]. Two-dimensional clock require more complex control circuits and are more challenging to implement than one-dimensional clock. The two-dimensional clock requires more coordination between the clock wire and the QCA bed, and the manufacturing process is more complicated [15-16]. In contrast, one-dimensional clock is less complicated. This paper is based on one-dimensional clock. The equal width of each clock floor prevents additional complexity in the fabrication process and even allows the production of the cell and clock wire layers separately. This paper considers the following principles for the cell layer, which aims to integrate and simplify the manufacturing process.

1. The width of all clock areas(in the entire circuit is equal.
2. When the layer changes, the clock should not change.
3. The width of each clock area is six cells.

QCA based five-input majority gate

In general, due to its wide application, the majority gate is one of the most critical gates in designing QCA-based circuits [17]. Among the previous design topics in the design of the majority gate that has received less attention and focus is the need to change the clock in the standard three-input majority gate. The introduced majority gate only requires clock change at the output (and not at the input). This makes it easier to use and less complicated to design the rest of the circuit. The proposed majority gate design is in such a manner as to enable utilization in the one-dimensional clock system, as well as the conditions alluded to in the previous section. The proposed three-input majority gate layout is shown in Fig. 4, and the equation of the three-input majority gate is:

$$M\left(A,B,C\right)=\bar{A}BC+A\bar{B}C+AB\bar{C}+ABC \quad (1)$$

In Fig. 4, “a, b, c” are input cells, and “o” is the output cell.

Fig. 5 displays the aforementioned five-input majority gate (only requiring output clock change & not needed during input). In general, the three-input majority gate can easily be constructed by

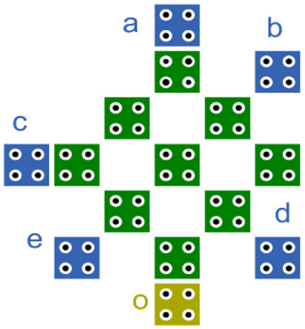

Fig. 5. Proposed five-input Majority Gate.

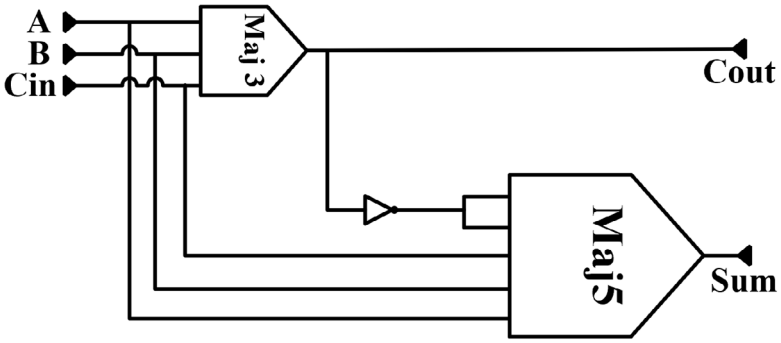

Fig. 6. Proposed full adder schematic.

a five-input majority gate and applying a fixed input. But this case is not required in the five-input majority gate, and they become a three-input majority gate simply by removing two inputs. The proposed structure is observable in Fig. 4. It should be stipulated that the output cell clock in fig. 5 is 0.25 clock more than the input clock. The equation of the five-input majority is:

$$M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (2)$$

In **Fig.**, "a, b, c, d, e" is input cells, and "o" is the output cell.

Proposed QCA one-bit full adder

Because of the widespread use of this block in computational circuits [14], and optimally designed full adder is quite helpful in the optimal design of a large unit such as a multi-bit adder or multiplier [18]. This block has three inputs and two outputs. The equation of the proposed full adder for sum and carry out are:

$$C_{out} = maj(A,B,C_{in}) \quad (3)$$

$$Sum = maj\left(A,B,C_{in},\overline{C_{out}},\overline{C_{out}}\right) \quad (4)$$

In (3), (4)," A, B" are input bits, and "*C-in*" is input carry. And "sum" is the sum of 3 inputs and "C_{out}" is output carry. Fig.6 shows schematic of proposed full adder.

The proposed full adder is based on the one-dimensional clock and has mentioned the situation of each clock floor. As shown in Fig.7 (a), layer one is used for the main gates, and Fig.7 (b) shows layer two used as VIA for layer one with layer three connecting. Fig.7 (c) shows layer three used for crossover and connecting cells that can not connect to each other in layer one. All inputs and outputs are in layer one and accessible. In Fig. 7 (a), "a, b, Cin" are input cells "sum, Cout" are the output cells of the proposed full adder

Proposed 4-bit Full adder

In light of the fact that it is introduced in the one-bit full adder design, the inputs and outputs of the circuit are arranged in such a way that the circuit inputs are on one side, the circuit outputs are on the other side, and hence, simply by correctly connecting several full adders, can make

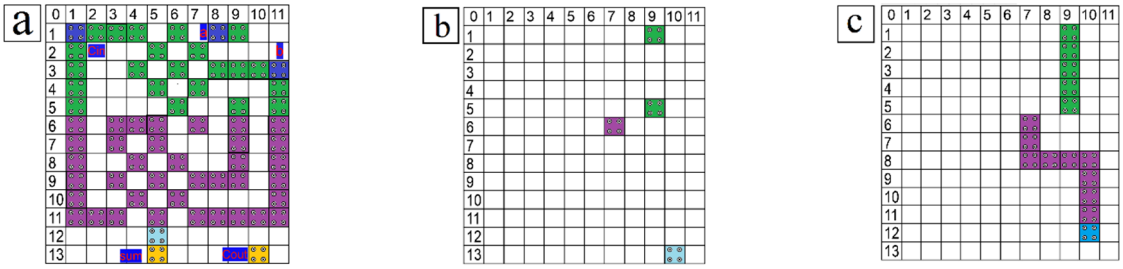

Fig. 7. proposed full-adder design a) Layer 1 b) Layer 2 c) Layer3.

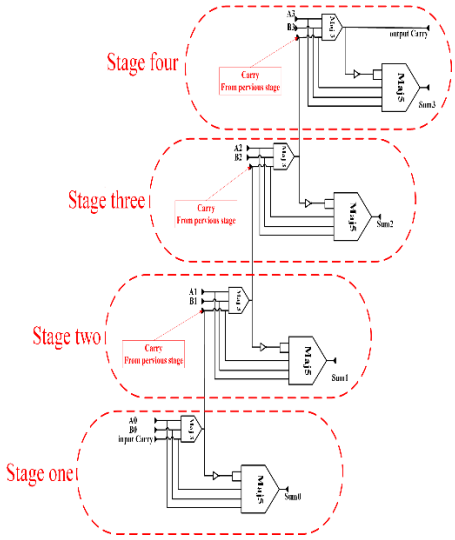

Fig. 8. 4-bit Full adder schematic.

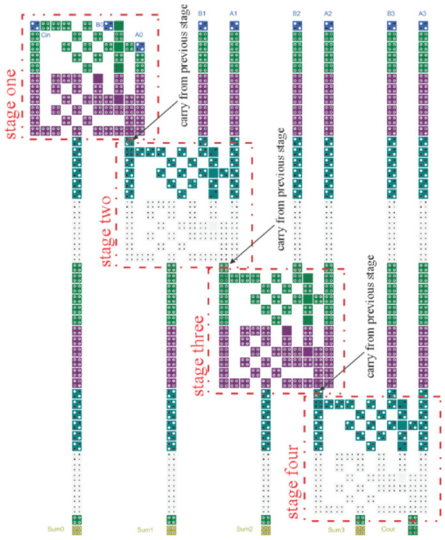

Fig. 9. Proposed QCA RCA 4-bit Full adder cells design.

a multi-bit adder. The schematics and design of the introduced 4-bit adder cells that can work in one-dimensional clock are shown in Fig. 8. The carry output of each stage is connected to the next stage's carry input. Cells after the sum output cell are for clock syncing, which is neglected in many papers but is necessary for a real adder. Fig. 9 shows the layout of the proposed 4-bit adder. The proposed 4-bit adder consists of 555 cells and 0.75 µm2 Occupied area where many cells and areas are used for syncing outputs and inputs to each other. This tip was neglected in many papers to reduce cell and area, causing the circuit to be unusable. In the proposed design, all raised items are considered. The proposed 4-bit adder has two clock cycles latency. Inputs cells of the proposed 4-bit adder placed above the circuit and outputs cells placed below the circuit are shown in Fig. 9.

RESULTS AND DISCUSSION

Simulation results

Simulation of proposed designs and performance accuracy has been performed in well-known QCADesigner 2.0.3 software with coherence vector simulation engine and setting listed in Table 1 [19]. The introduced one-bit full adder has only 0.75 Clock latency, and the comparison of this full adder with other full adders is demonstrated in Table 2. In terms of latency, the introduced full adder, in spite of the use of a one-dimensional clock, has an acceptable latency compared to other designs. Most paper's power analysis is undertaken via the QCAPro software [20]. While QCAPro uses version 1.4 of QCADesigner software, it supports only one cell layer. This makes its findings not sufficiently accurate for comparison purposes. In this paper,

Table 1. QCADesigner coherence vector engine setting.

Temperature	1.0 K
Relaxation Time	1.0e-15 s
Time Step	1.0e-16
Total Simulation Time	7.0e-11s
Clock High	9.8e-22 j
Clock Low	3.8e-23 j
Clock Shift	0
Clock Amplitude Factor	2.0
Radius of Effect	80.0 nm
Relative Permittivity	12.9
Layer Separation	11.5 nm

Table 2. Comparison results of full-adders design whit prior works.

Design source	No. of Cells	Area(μm^2)	Latency(clock cycle)	Crossover type	1D Clocking Scheme	Total energy dissipation	Quantum cost
[23]	26	0.02	0.5	Coplanar	NO	2.23e-2 eV	0.01
[24]	41	0.03	1	Coplanar	NO	3.0e-2 eV	0.03
[25]	59	0.043	1	Multilayer	NO	2.16e-2 eV	0.043
[26]	93	0.09	1.25	Multilayer	NO	3.52e-2 eV	0.1125
[11]	28	0.02	0.5	Coplanar	NO	2.31e-2 eV	0.01
[27]	48	0.02	0.5	Coplanar	NO	1.11e-2 eV	0.01
Proposed	80	0.06	0.75	Multilayer	YES	2.06e-2 eV	0.045

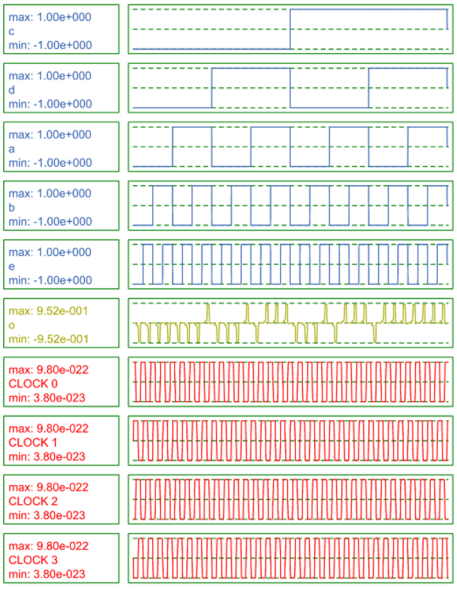

Fig. 10. Proposed five-input Majority Gate simulation results.

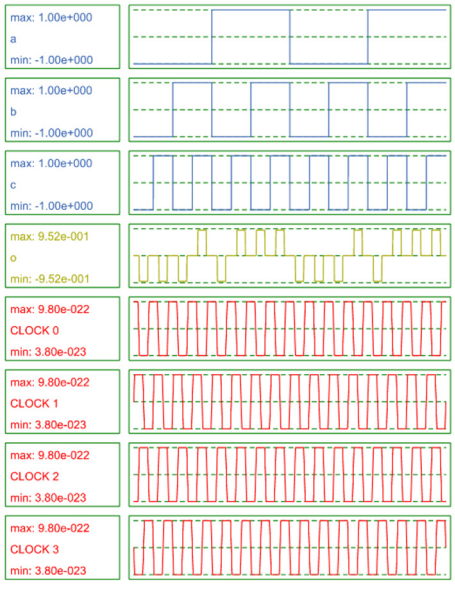

Fig. 11. Proposed three-input Majority Gate simulation results.

the QCAdesigner-E software (Version 2.2), which supports the multi-layer structure, is used for power analysis [21]. The findings can be seen in Table 2. Simulation results of the proposed three-input majority gate and five-input majority gate are depicted in Fig. 10 and Fig. 11, showing their correct function.

The quantum cost is the trade-off between the delay and complexity equivalent to the multiplication of total area and latency [22]. The proposed full adder simulation result is depicted in Fig. 12, and the first correct output appears after the 0.75 clock cycle. Fig. 13 shows the proposed 4-bit adder, and the first correct output appears

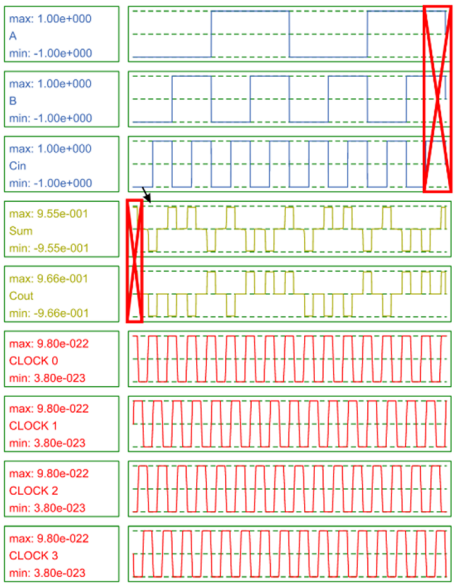

Fig. 12. Full adder simulation result.

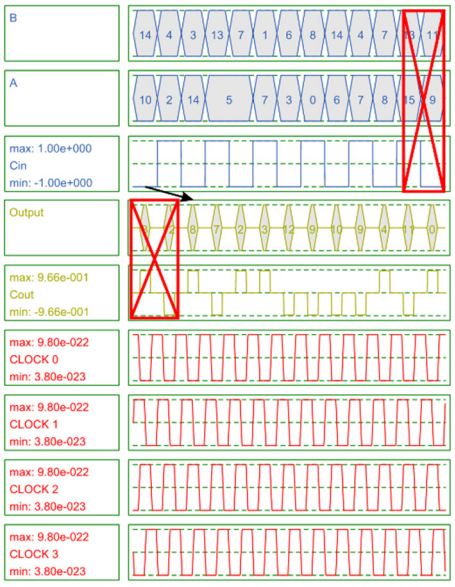

Fig. 13. proposed 4-bit full adder result.

Table 3. Comparison results of 4-bit adder design whit prior works.

Design source	No. of Cells	Area(μm^2)	Latency(clock cycle)	Crossover type	1D Clocking Scheme	Quantum cost
[28]	269	0.37	3.5	Coplanar	NO	1.295
[29]	651	1.2	17	Coplanar	NO	20.4
[30]	339	0.254	7	Multilayer	NO	1.778
[31]	125	0.17	5	Coplanar	NO	0.85
[32]	1435	1.21	5	Coplanar	NO	6.05
[33]	237	0.24	6	Multilayer	NO	1.44
[10]	308	0.29	2	Multilayer	NO	0.58
Proposed	555	0.75	2.25	Multilayer	YES	1.5

after two clock cycle latency.

Even though the presented design utilizes a one-dimensional clock, as far as latency, it is comparable to other proposed schemes wherein inputs & outputs can be accessed. In Table 2, the proposed full adder is compared in detail with the other prior proposed designs. Table 3 shows the comparison of the proposed 4-bit adder with prior designs. The number of cells and the occupied area within the circuit proposed in this paper are not optimal or the best compared to other papers. This is a consequence of the usability and easy-to-construct nature of the circuit, as well as the utilization of a one-dimensional clock. Quantum cost and latency can compete with the circuits that assume the full adder as a functional block. In certain papers, to reduce the noted instances, a block is utilized while ignoring the fact that the block must be able to be used in the remainder of the circuit. This lack of attention causes serious challenges in large-scale designs and even renders these blocks unusable.

The proposed designs concerning proper and orderly design will not have most of these challenges in the production process and also will be a good product candidate.

CONCLUSION

This paper proposes a five-input majority gate and a three-input majority gate that does not need to change the clock at the input cell and can work in the one-dimensional clock. Then, this paper proposes a one-bit full adder capable of working in the one-dimensional clock that was designed with the proposed majority gates, which has only 0.75 clock cycle latency and suitable inputs and outputs arrangements that give them the multi-bit extensibility feature. The proposed designs concerning proper and orderly design will not have most of these challenges in the production

process and also will be a good product candidate. The Advantage of the proposed design is that it is designed according to the properties of the one-dimensional clock to make the construction process simple.

CONFLICTS OF INTEREST

The authors do not have any conflicts of interest.

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