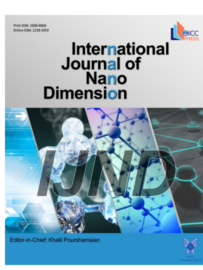

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Improvement of digital and analog/RF performances of stacked gate oxide JLTFET using heterostructure and lightly doped drain

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Original Research

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Abstract:
In this paper, a novel heterostructure stacked gate oxide junctionless tunnel field effect transistor (HS-SGO-JLTFET) with a lightly doped drain (LDD) region is proposed. The low band gap material (InAs) in the source region generates a stronger electric field in the source-channel junction, thereby increasing the ON current to 1.8×10^{-4} A/μm. Conversely, the lightly doped drain region near the channel end mitigates the electric field in the channel-drain junction, reducing the ambipolar current to 1.26×10^{-15} A/μm. Furthermore, the performance of the proposed device is analyzed with respect to analog/RF parameters. In this regard, the LDD-HS-SGO-JLTFET exhibits a smaller gate-to-drain capacitance (C_{gd}) of 0.14 fF, a larger transconductance (g_m) of 840 μs, a higher cutoff frequency (f_T) of 271 GHz, a bigger gain bandwidth product (GBWP) of 112 GHz, and a lower transit time (τ) of 6.55×10^{-13} s compared to the SGO-JLTFET. These improvements demonstrate that the proposed device is highly suitable for low-power and high-frequency applications.

Keywords: Ambipolar current; Heterostructure; Junctionless tunnel field effect transistor; Lightly doped drain; ON current; Stacked gate oxide

1. Introduction

According to Moore's Law, the IC industry doubles the number of devices on a chip every 24 months. Reducing transistor size is essential to fit more components on a chip. MOSFET scaling poses many challenges like short channel effects (SCEs), random dopant fluctuations, drain-induced barrier lowering (DIBL), high subthreshold swing (SS), and large OFF current (I_{OFF}). Low power consumption requires supply voltage scaling and low subthreshold swing. The SS of MOSFET is constrained to 60 mV/dec at lower technology nodes, making it unable to provide a high switching speed for low-power applications. To address the aforementioned challenges, researchers have recommended the tunneling field effect transistor (TFET) for substituting the MOSFET due to steeper SS, lower I_{OFF}, and more overcoming of short channel effects (SCEs). The advantages of TFET make it suitable for applications with high energy efficiency and low power dissipation [1–10]. The current transfer mechanism in TFET is based on band-to-band tunneling (BTBT), while the injection of carriers in MOSFET is through thermionic emission on the barrier [9–13]. Although TFETs provide many advantages, they face problems such as low ON current and ambipolar conduction [14–16]. Researchers have reported many approaches to raise the ON current (I_{ON}), including double gate architecture with high-k dielectric gate [17], strain engineering [18], n^+ pocket [19, 20], low band gap material at the source region [21, 22], L-shaped gate TFET [23], and U-shaped gate TFET [24]. Moreover, several techniques such as hetero gate dielectric [25, 26], gate-drain underlap [27], drain doping engineering [28–32], and drain dielectric pocket [33–35] are proposed to reduce the ambipolar current (I_{amb}).
As device dimensions are reduced to below 100 nm, fabrication complexity is a major challenge for such a technology node. To overcome this problem, junctionless TFETs (JLTFETs) have been introduced, which have a simpler fabrication process. In JLTFETs, the doping type of the source, channel, and drain regions is the same. They do not require the formation of a steep p-n junction. The P-I-N structure is induced using the charge plasma method, where metal gates

with appropriate work functions are placed over the source and channel regions. The polar gate (PG) and the control gate (CG) are utilized to implement the BTBT principle in JLTFETs. In n-channel JLTFETs, the PG, which has a higher work function, is positioned above the source region. This configuration is intended to create a P^+ source region. The CG, which is located in the middle and has a lower work function than the PG, can create an intrinsic channel region. A similar configuration is considered for P-channel JLTFETs, although different work functions are used for the PG and CG [36–39]. For JLTFETs, several ideas such as dual material gate [40–43], band gap engineering [44–47], metal implant at source/channel junction [48–50], stacked gate oxide [51, 52], and p^+ pocket [45, 53] have been proposed to boost the I_{ON}. Several techniques also show that Iamb can be reduced by gate material engineering [54], Gaussian doping [55], and gate overlap engineering [56].

In this paper, a new heterostructure stacked gate oxide JLTFET (HS-SGO-JLTFET) is proposed with a lightly doped drain (LDD). The reduction of gate oxide thickness leads to increased leakage at the gate oxide-silicon interface, which negatively affects device performance. This problem is overcome by using a high-k material (HfO_2) in addition to the thin SiO_2 layer. The stacked gate oxide (SiO_2/HfO_2) reduces the leakage current at the gate-channel interface. The high-k gate dielectric (HfO2) increases band bending, leading to more I_{ON} and steeper SS. The low-k dielectric layer (SiO_2) also prevents lattice mismatch between channel and HfO_2 dielectric. In addition, the band gap engineering is accomplished by applying lower band gap InAs in the source region and higher band gap Si in the channel and drain regions. Using the low band gap material (InAs) in the source region reduces the tunneling barrier width in the source-channel junction and consequently enhances the I_{ON}. The reason for selecting Si/InAs as the heterostructure is its simpler fabrication method compared to other hetero material-based structures. Moreover, a lightly doped drain (LDD) region is included near the channel end, which widens the tunneling barrier at the channel-drain junction, thereby reducing the Iamb. The LDD idea has been previously suggested in Refs. [31, 32], but its effect on JLTFET has not yet been reported. In this work, this idea is introduced for the first time in heterostructures-based SGO-JLTFET. The main objective of this paper is to illustrate the effect of combining LDD with a heterostructure on the electrical characteristics and analog/RF parameters of the SGO-JLTFET.

The rest of this paper is organized as follows: In section 2, the device structure and simulation setup are elaborated. In section 3, the simulation results in terms of DC characteristics and RF performance are discussed. Finally, the conclusion is summarized in section 4.

2. Materials and methods

Figure 1 (a-c) illustrates the schematic view of the SGO-JLTFET, HS-SGO-JLTFET, and LDD-HS-SGO-JLTFET, respectively. Initially, the SGO-JLTFET is designed as a silicon-based structure with a (SiO+HfO) stack. Then, the HS-SGO-JLTFET is constructed by substituting Si with InAs in the source region. Finally, the LDD-HS-SGO-JLTFET is created by applying a lightly doped drain (LDD) region adjacent to the channel end. The physical consequences of Si/InAs-based devices (HS-SGO-JLTFET and LDD-HS-SGO-JLTFET) are compared with Si-based SGO-JLTFET to demonstrate the amelioration in the performance parameters.

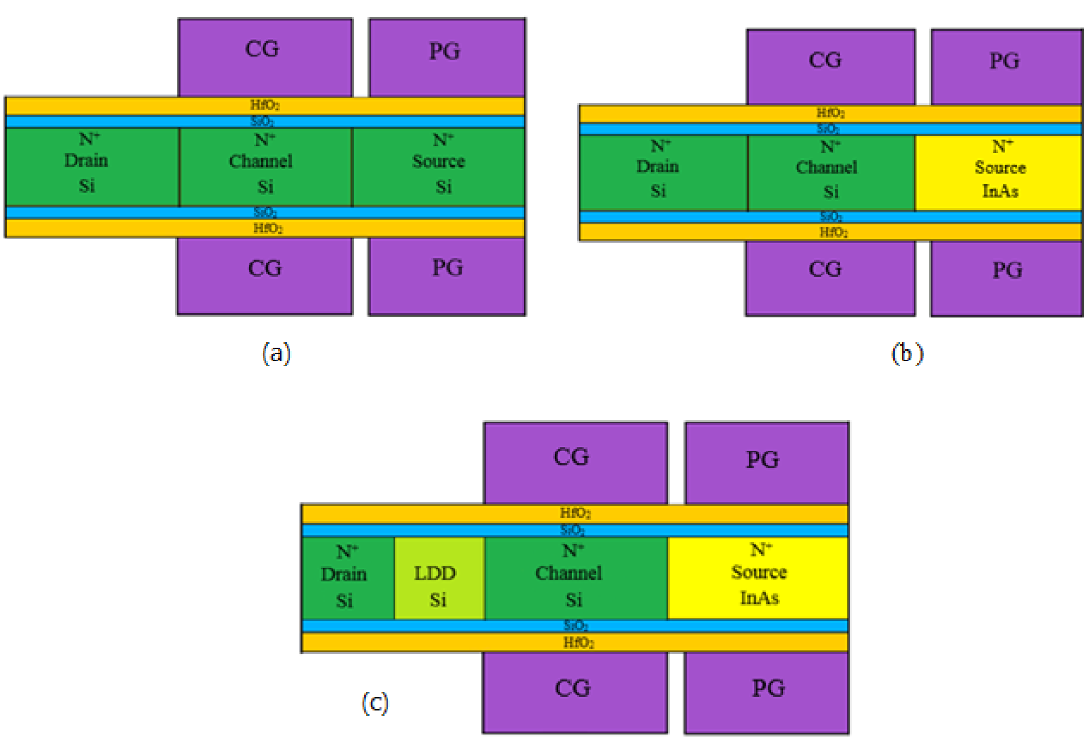

Figure 1. Cross-sectional view of (a) SGO-JLTFET (b) HS-SGO-JLTFET, (c) LDD-HS-SGO-JLTFET.

All three device structures are N-type JL-TFETs and consist of a polar gate (PG) and a control gate (CG). A spacer with a length of 2 nm separates the PG and CG. The work function of the PG is set to 5.9 eV to convert the N^+ source into a P^+ source, while the CG work function is set to 4.3 eV to convert the N^+ channel into an intrinsic channel. Platinum (Pt) and aluminum (Al) are considered as the PG and CG materials, respectively. A heavy N-type doping concentration of 1×10^{19} cm^{-3} is applied to the source, channel, and drain regions. In the LDD-HS-SGO-JLTFET, the doping concentration of the lightly doped drain (LDD) is assumed to be 1×10^{17} cm^{-3}. Additional design parameters are detailed in Table 1.

Table 1. Design parameters for three devices.

Parameters	Value
Source Length	20 nm
Drain Length	20 nm
Channel Length	20 nm
LDD Length	10 nm
Body Thickness	5 nm
SiO_2 Thickness	0.8 nm
HfO_2 Thickness	1.2 nm

All simulations in this study are performed using the Silvaco ATLAS simulator [57]. To provide an in-depth analysis of the device physics, the non-local BTBT model is employed to calculate the tunneling rate at the junctions. The band gap narrowing model is used to account for the effects of heavy channel doping. Minority carrier recombination effects are incorporated using the Shockley-Read-Hall recombination model, and the Lombardi CVT mobility model is utilized to capture the influences of doping, electric field, and temperature. The trap-assisted tunneling model is used to include interface trap effects, and the quantum confinement model is applied due to the body thickness being less than 10 nm [54].
The non-local BTBT model is calibrated using the experimental work reported in [58]. The I_{DS}-V_{GS} curve is plotted based on the same data as in [58], demonstrating strong agreement with the published fabrication-based results, as shown in figure 2. This alignment confirms the accuracy of our simulation setup.
Fig. 3 depicts the main fabrication steps of the LDD-HS-SGO-JLTFET, which are explained as follows:

- a) The Si drain region is doped using a combination of low- and high-energy implants [59].
- b) The source region is recessed into the silicon substrate using an etching process.
- c) The InAs layer is deposited via epitaxial growth [45].
- d) The SiO_2 and HfO_2 gate oxides are deposited using the atomic layer deposition (ALD) technique. The ALD method allows for thickness control at the angstrom level, making it easy to deposit a 0.8 nm SiO_2 layer [60].

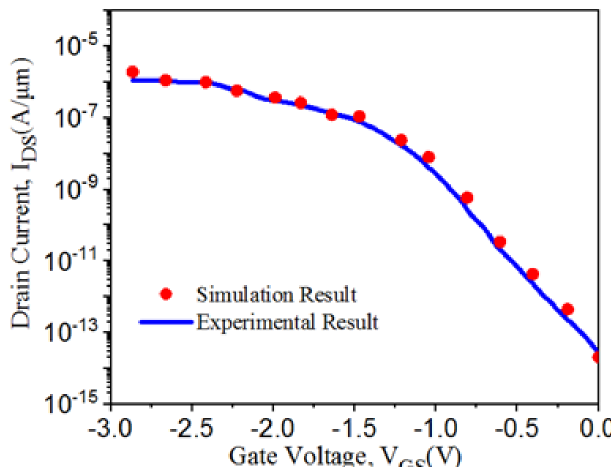

Figure 2. Calibration of I_{DS}-V_{GS} characteristics using experimental work [58].

- e) Metal gates are deposited using electron beam lithography [42, 61].

3. Results and discussion

3.1 DC performance

This section examines the influence of the heterostructure (HS) and lightly doped drain (LDD) region on the DC performance of the stacked gate oxide JLTFET.
Figures 4 (a) and b illustrate the energy band diagrams for the three devices in the ON and ambipolar states, respectively. As shown in figure 4 (a), the tunneling barrier width of the HS-SGO-JLTFET and LDD-HS-SGO-JLTFET is narrower compared to the SGO-JLTFET. This reduction in barrier width arises from the utilization of the narrow band gap material (InAs) in the source region. The presence of Si/InAs hetero material at the source-channel junction causes the conduction band to be pulled down so that the conduction band minimum occurs at the source-channel interface. Because of this, the tunneling barrier width is diminished. Consequently, a higher number of electrons tunnel from the source to the channel, resulting in an increased I_{ON}. Additionally, figure 4 (a) demonstrates that the lightly doped drain region near the channel end does not influence the tunneling width at the source-channel interface. It can also be observed from figure 4 (b) that the LDD-HS-SGO-JLTFET exhibits a wider tunneling barrier at the drain-channel interface compared to the SGO-JLTFET and HS-SGO-JLTFET. This widening occurs because the inclusion of the LDD near the channel-drain junction expands the barrier width at the drain-channel interface, reducing the tunneling rate and ultimately suppressing ambipolar conduction.
Figure 5 represents the transfer characteristics of the three devices. It is evident that both the HS-SGO-JLTFET and LDD-HS-SGO-JLTFET achieve higher ON currents and steeper subthreshold swings (SS) than the SGO-JLTFET. These improvements are attributed to the incorporation of InAs, which has a narrower bandgap compared to silicon. The enhanced I_{ON} of heterostructure-based devices is

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(a)

(b)

(c)

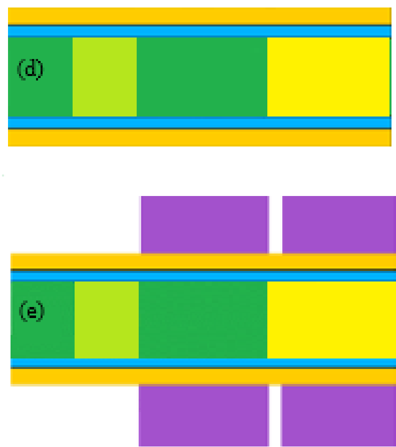

Figure 3. Manufacturing process of the LDD-HS-SGO-JLTFET.

achieved from the sudden band bending, which leads to a minimized conduction band at the source-channel junction. Moreover, the LDD-HS-SGO-JLTFET achieves the lowest I_{amb} among the three devices, owing to the presence of the lightly doped drain region. The inclusion of the LDD in the vicinity of the channel enlarges the tunneling width at the drain-channel junction and subsequently degrades the ambipolar current. Consequently, the LDD-HS-SGO-JLTFET demonstrates superior drain current performance relative to the other two devices.

In this study, threshold voltage (V_{th}) is determined using the constant current method. Here, V_{th} refers to the V_{GS} obtained from the transfer characteristics, where $I_{DS} = 2.89 \times 10^{-8}$ A/μm. The HS-SGO-JLTFET and LDD-HS-SGO-JLTFET have a smaller V_{th} than the SGO-JLTFET, as seen in figure 5. This means that Si/InAs based-devices require less voltage to turn on compared to the Si-based device.

The carrier concentrations of the three devices in the ON state are presented in figure 6. It is observed that the HS-SGO-JLTFET and LDD-HS-SGO-HJLTFET show a sharp upsurge in the electron concentration near the source-channel junction, while the SGO-JLT-FET demonstrates a steady increase in the electron concentration near the same junction. Using the Si/InAs heterostructure generates an N-doped pocket area below the gap between PG and CG. This formation increases the electron concentration of the region beneath the gap area. Due to this, the conduction band minimum is formed at the source-channel interface, which leads to a narrowing of the tunneling barrier width.

Figures 7 (a) and 7 (b) depicts the electric field distributions for the three devices in the ON and ambipolar states. As shown in figure 7 (a), the electric field peak at the source-channel junction is significantly higher for the HS-SGO-JLTFET and LDD-HS-SGO-JLTFET compared to the SGO-JLTFET. This elevated electric field in the source-channel junction implies a raised ON current for the Si/InAs heterostructure-based devices. The use of InAs with its narrower band gap than silicon induces an N-doped source region betwixt the two gates, which causes a fringing field near the source-channel interface. This event results in further bending of the energy bands and facilitates an increased tunneling current at the source-channel junction.

Figure 7 (b) demonstrates that the electric field in the channel-drain junction of the LDD-HS-SGO-JLTFET is lower than that of the other two devices. The attenuated

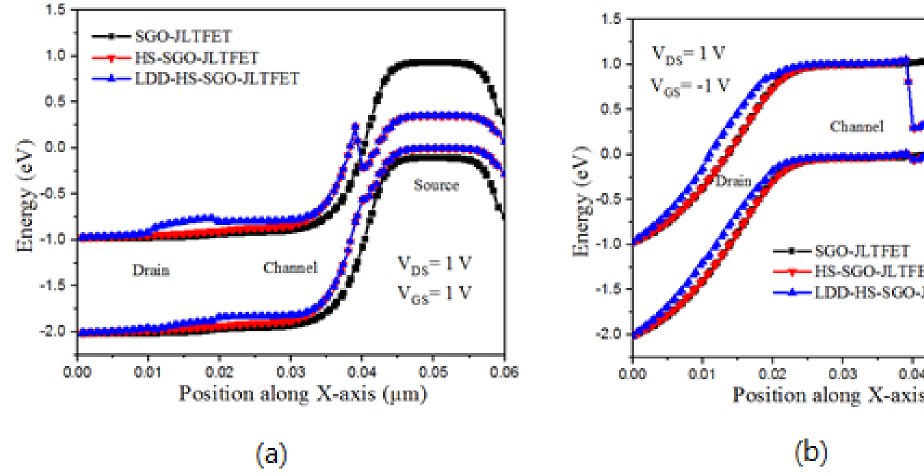

Figure 4. Relative investigation of energy band diagrams for all three devices in (a) ON state, (b) ambipolar state.

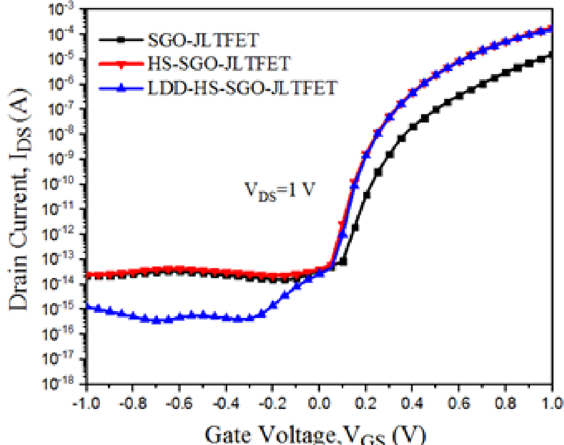

Figure 5. Relative investigation of transfer characteristics for all three devices.

electric field denotes a decrease in the slope of the energy bands at the drain/channel junction, which is attributed to the LDD's effectiveness in mitigating ambipolar conduction. The DC parameters of all three devices are listed in Table 2. Based on the table, the parameters of I_{ON}, I_{ON}/I_{OFF}, V_{th}, and SS of both Si/InAs-based devices (HS-SGO-JLTFET and LDD-HS-SGO-JLTFET) are improved compared to SGO-JLTFET. Furthermore, the smallest I_{amb} is obtained for the proposed device (LDD-HS-SGO-JLTFET).

3.2 Analog/RF performance

In this section, the analog/RF parameters of the proposed LDD-HS-SGO-JLTFET are investigated and its outcomes are compared with SGO-JLTFET and HS-SGO-JLTFET. Figure 8 (a) and 8 (b) illustrates the gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) of all three devices, respectively. Parasitic capacitances (C_{gs} and C_{gd}) play a key role in measuring the RF performance of the device. For an efficient device, the value of these capacitances should be small to avoid excessive power dissipation and slow switching speed. According to figure 8 (a), the value of C_{gs} is higher in HS-SGO-JLTFET and LDD-HS-SGO-JLTFET compared to SGO-JLTFET due to the strong

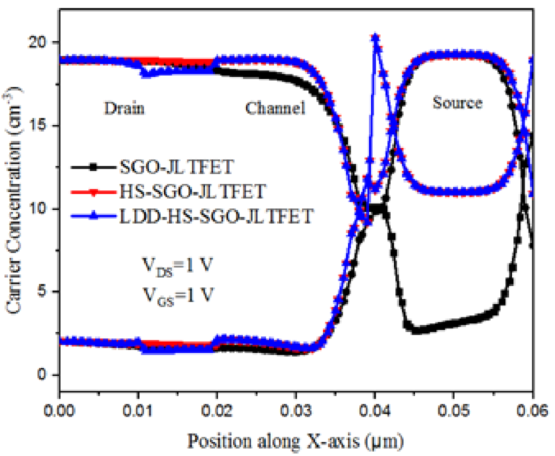

Figure 6. Relative analysis of carrier concentration for all three devices in ON state.

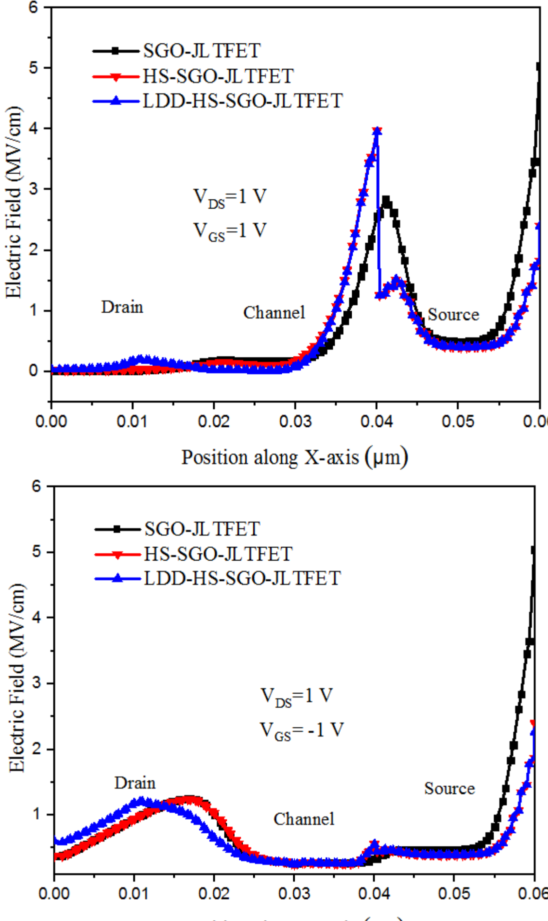

Figure 7. Relative analysis of electric field for all three devices in (a) ON state (b) ambipolar state.

coupling between gate and source. As can be observed from figure 8 (b), the C_{gd} of all three devices rises with increasing VGS, which is due to the formation of an inversion layer from drain to source. At higher gate bias, the LDD-HS-SGO-JLTFET has the lowest C_{gd}, due to employing the lightly doped drain. The C_{gd} value of LDD-HS-SGO-JLTFET is 0.14 fF at $V_{GS} = 1$ V.

Transconductance (g_m) is an important parameter for the design of RF circuits, which relates the input voltage across the device to the output current. To achieve high gain and large driving capability, g_m should be high. Mathematically it is written as [62]

$$g_m = (\frac{dI_{DS}}{dV_{GS}}) \tag{1}$$

Figure 9 illustrates the transconductance of all three devices under different gate-source voltages. As can be seen, the transconductance is enhanced with the increase of the gate voltage for all devices. It is also evident from figure 9 that band gap engineering in HS-SGO-JLTFET and LDD-HS-SGO-JLTFET results in a significant advancement in gm value. Furthermore, there is no difference between the g_m of these two devices. Because the application of LDD does not change the tunneling distance in the source-channel interface. The LDD-HS-SGO-JLTFET and HS-SGO-JLTFET have increased g_m of 840 μs, which is 8 times larger than

Table 2. DC Parameters of all three devices.

Parameters	SGO-JLTFET	HS-SGO-JLTFET	LDD-HS-SGO-JLTFET
I_{ON} (A/μm)	1.60×10^{-5}	1.80×10^{-4}	1.80×10^{-4}
I_{OFF} (A/μm)	3.66×10^{-14}	4.02×10^{-14}	2.66×10^{-14}
I_{ON}/I_{OFF}	0.44×10^{9}	0.45×10^{10}	0.68×10^{10}
I_{amb} (A/μm)	2.31×10^{-14}	2.31×10^{-14}	1.26×10^{-15}
V_{th} (V)	0.34	0.28	0.28
SS (mV/dec)	37	25	25

that of the SGO-JLTFET.
Another key parameter determining RF performance is the transconductance generation factor (TGF), which transforms the drain current (I_{DS}) into g_m and is formulated as [62]

$$TGF = (\frac{g_m}{I_{DS}}) \tag{2}$$

The variation of TGF versus V_{GS} for all three devices is shown in figure 10. The higher TGF for all three devices is achieved at lower V_{GS} due to the domination of g_m over I_{DS}. After reaching the maximum value, further increase in V_{GS} causes TGF degradation due to the domination of I_{DS} over g_m. It is also clear from figure 10 that Si/InAs-based devices (HS-SGO-JLTFET and LDD-HS-SGO-JLTFET) are provided more TGF value as compared with SGO-JLTFET at low gate bias. The highest TGF value for LDD-HS-SGO-JLTFET and HS-SGO-JLTFET is 4.73×10^{2} V^{-1}, which is 2.19 times higher than that of the SGO-JLTFET.

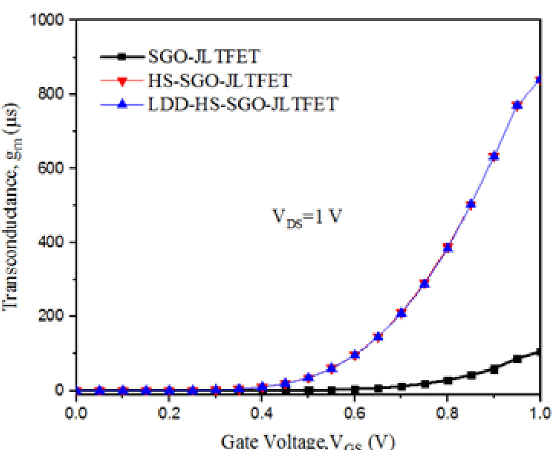

Figure 9. Comparative plot of transconductance for all three devices.

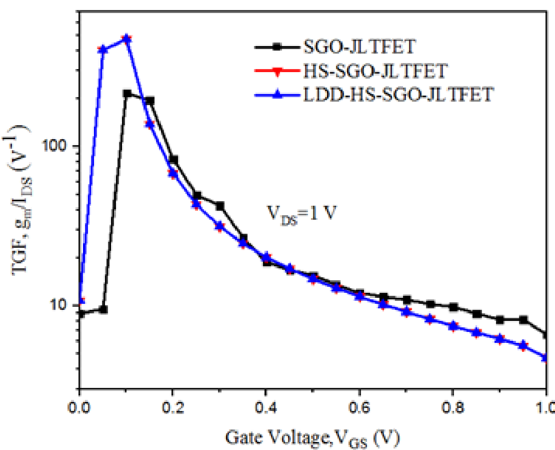

Figure 10. Comparative plot of transconductance generation factor for all three devices.

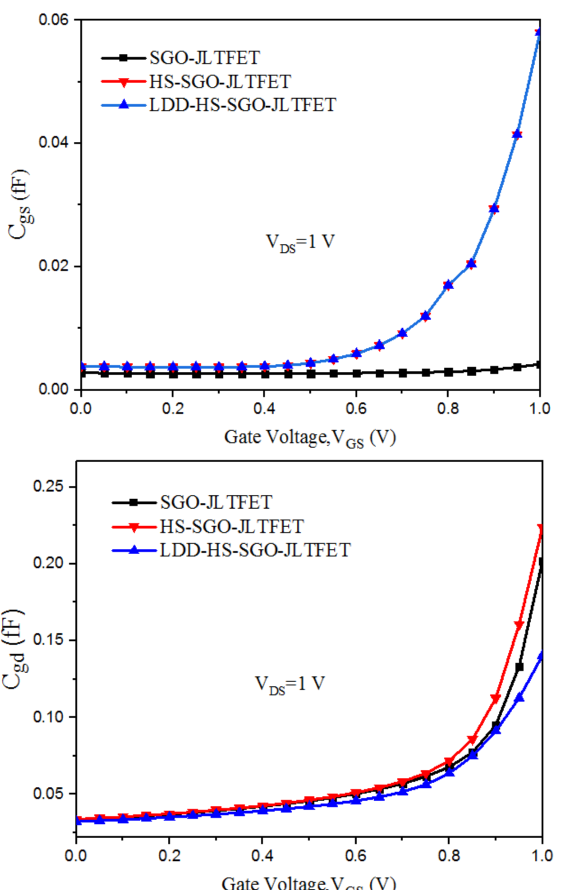

Figure 8. Relative examination of (a) gate-to-source capacitance (b) gate-to-drain capacitance for all three devices.

The cut-off frequency (f_T) is another critical parameter in determining the suitability of a device for RF applications. It can be defined as the frequency for which the short-circuit current gain achieves the unity value and is computed as [63]

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{3}$$

In figure 11 the variation of cut-off frequency is shown for the three devices. It is found from the figure that the f_T of the LDD-HS-SGO-JLTFET is higher than the other two devices. This is the result of the enhancement in g_m and degradation in C_{gd}, which is achieved due to the combination of Si/InAs heterostructure with LDD. The maximum f_T value

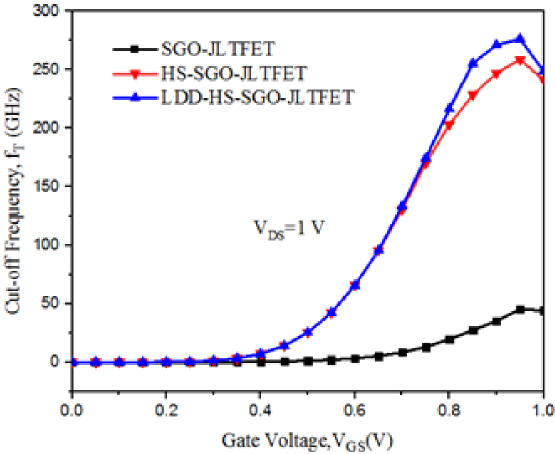

Figure 11. Comparative analysis of cut-off frequency for all three devices.

for SGO-JLTFET is 4.51×10^{10} Hz, whereas the maximum f_T value for HS-SGO-JLTFET and LDD-HS-SGO-JLTFET is 2.59×10^{11} Hz and 2.71×10^{11} Hz, respectively.
Another important parameter to consider when evaluating the high-frequency performance of the device is the gain bandwidth product (GBWP). It demonstrates how effectively the device can amplify signals across different frequencies. The GBWP for the DC gain of 10 can be calculated as [63]

$$\mathrm{GBWP} = \frac{g_m}{20\pi(C_{gd})} \tag{4}$$

Figure 12 exhibits the investigation of all three devices in terms of GBWP. First GBWP curve rises with increasing gate voltage and reaches its peak value. After that, the curve starts to decrease due to the increment of C_{gd} value. It is also observed that the LDD-HS-SGO-JLTFET has the highest GBWP value (1.12×10^{11} Hz), which is 1.2 and 10.87 times greater in comparision to HS-SGO-JLTFET and SGO-JLTFET. The superiority of the LDD-HS-SGO-JLTFET in terms of GBWP is due to increased g_m and lower C_{gd}.
Transit time (τ) is another significant parameter to evaluate the device for high-frequency operation, which is described as the time needed for carriers to travel from the source to the drain region and is determined as [54]

$$\tau = \frac{1}{2\pi f_T} \tag{5}$$

The τ characterizes the transfer speed of charge carriers, and a low τ indicates a faster response time and a higher operating speed of the device. Therefore, for a fast-switching transistor, this parameter should be low. The comparison of transit time for all three devices is shown in figure 13. As shown in the figure, HS-SGO-JLTFET and LDD-HS-SGO-JLTFET have similar τ up to 0.75 V, which is less than that of SGO-JLTFET. For $V_{GS} > 0.75$ V, the lowest value of τ is observed in the LDD-HS-SGO-JLTFET due to higher f_T. According to figure 13, the LDD-HS-SGO-JLTFET has the τ value of 6.55×10^{-13} s at $V_{GS} = 1$ V.
The comparison between the DC and analog/RF parameters of the proposed LDD-HS-SGO-JLTFET and recently reported JLTFETs [39, 41, 44, 45] is shown in Table 3. The table indicates that the proposed device performs better than other JLTFET devices in terms of I_{ON}, g_m, f_T, and GBWP. Consequently, it is a suitable candidate for low-power digital applications and analog/RF circuits.

4. Conclusion

This paper presents a new stacked gate oxide JLTFET that integrates a Si/InAs heterostructure and a lightly doped drain region. The use of the narrow band gap material (InAs) in the source region increases the band bending and reduces the tunneling width. As a result, a stronger electric field peak forms at the source-channel junction, leading to higher I_{ON} and steeper SS. Additionally, the lightly doped drain (LDD) adjacent to the channel weakens the electric field at the channel-drain junction, which reduces ambipolar current.
Furthermore, by examining the RF parameters, it is found that using band gap engineering along with LDD boosts f_T and GBWP due to larger g_m and smaller C_{gd}. Overall, the proposed device performs well for low-power and analog/RF applications.

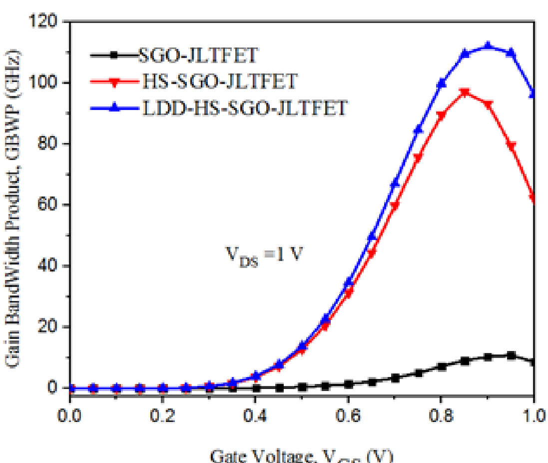

Figure 12. Comparative analysis of gain bandwidth product for all three devices.

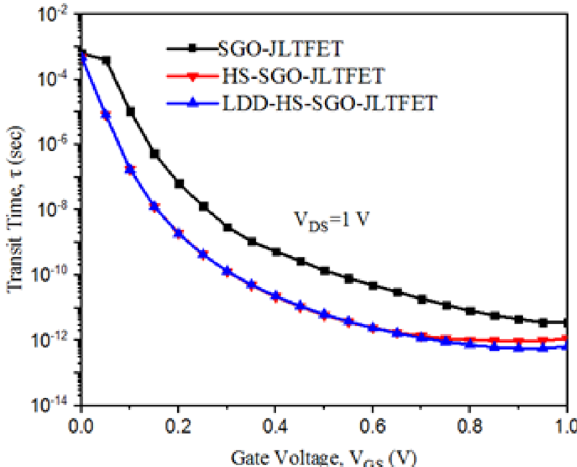

Figure 13. Comparative analysis of transit time for all three devices.

Table 3. Performance comparison of LDD-HS-SGO-JLTFET with recently reported JLTFET structures.

Structures	I_{ON} (A/μm)	SS (mV/dec)	g_m (μs)	f_T (GHz)	GBWP (GHz)
SNPJL-TFET [39]	5.43×10^{-5}	20	210	65.4	14.9
DMMG-HJLTFET [41]	1.01×10^{-5}	-	12.6	9.17	0.17
HJLTFET [44]	1.45×10^{-5}	-	55	-	50.6
Reported JLTFET [45]	1.80×10^{-4}	42.3	170	12	11/8
LDD-HS-SGO-JLTFET (Proposed Device)	1.80×10^{-4}	25	840	271	112

Authors contributions
Authors have contributed equally in preparing and writing the manuscript.

Availability of data and materials
The authors declare that the data supporting the findings of this study are available within the paper.

Conflict of interests
The authors assert that they do not have any identifiable conflicting financial interests or personal relationships that might be perceived to influence the work presented in this paper.

References

[1] J. Ajayan, D. Nirmal, S. Tayal, S. Bhattacharya, L. Arivazhagan, A. Fletcher, P. Murugapandiyan, and D. Ajitha. “Nanosheet field effect transistors-A next generation device to keep Moore’s law alive: An intensive study.”. *Microelectronics Journal*, 114:105141, 2021. DOI: https://doi.org/10.1016/j.mejo.2021.105141.

[2] V. Vashishtha and L. T. Clark. “Comparing bulk-Si FinFET and gate-all-around FETs for the 5 nm technology node.”. *Microelectronics Journal*, 107:104942, 2021. DOI: https://doi.org/10.1016/j.mejo.2020.104942.

[3] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov. “Performance comparison between pin tunneling transistors and conventional MOSFETs.”. *IEEE Trans Electron Devices*, 56(3):456–465, 2009. DOI: https://doi.org/10.1109/TED.2008.2011934.

[4] H. Lu and A. Seabaugh. “Tunnel field-effect transistors: State-of-the-art.”. *IEEE J. Electron Devices Soc.*, 2(4):44–49, 2014. DOI: https://doi.org/10.1109/JEDS.2014.2326622.

[5] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu. “Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/Dec.”. *IEEE Electron Device Lett.*, 28(8):743–745, 2007. DOI: https://doi.org/10.1109/LED.2007.901273.

[6] Q. Zhang, W. Zhao, and A. Seabaugh. “Low-subthreshold-swing tunnel transistors.”. *IEEE Electron Device Lett.*, 27(4):297–300, 2006. DOI: https://doi.org/10.1109/LED.2006.871855.

[7] B. Sadeghi, S. Ghammamy, Z. Gholipour, M. Ghorchibeigy, and A. A. Nia. “Gold/hydroxypropyl cellulose hybrid nanocomposite constructed with more complete coverage of gold nano-shell. ”. *Micro & Nano Letters.*, 6(4):209–213, 2011. DOI: https://doi.org/10.1049/mnl.2011.0036.

[8] M. S. Sadjadi, B. Sadeghi, and K. Zare. “Natural bond orbital (NBO) population analysis of cyclic thionylphosphazenes, [NSOX $(NPCl_2)_2$]; X= F(1),X= Cl(2).”. *Journal of Molecular Structure: THEOCHEM*, 817((1-3)):27–33, 2007. DOI: https://doi.org/10.1016/j.theochem.2007.04.015.

[9] A. C. Seabaugh and Q. Zhang. “Low-voltage tunnel transistors for beyond CMOS Logic.”. *Proc IEEE.*, 98(12):2095–2110, 2010. DOI: https://doi.org/10.1109/JPROC.2010.2070470.

[10] A. M. Ionescu and H. Riel. “Tunnel field-effect transistors as energy efficient electronic switches.”. *Nature*, 479((7373)):329–337, 2011. DOI: https://doi.org/10.1038/nature10679.

[11] T. Bentrcia, F. Djefal, H. Ferhati, and Z. Dibi. “A comparative study on scaling capabilities of Si and SiGe nanoscale double gate tunneling FETs.”. *Silicon*, 12(4):945–953, 2020. DOI: https://doi.org/10.1007/s12633-019-00190-w.

[12] C. K. Pandey, D. Das, R. K. Kadava, T. Ashok, P. AnilK, and R. G. Siva. “A review on emerging tunnel FET structures for high-speed and low-power circuit applications.”. *2023 IEEE Devices for Integr.Circuit (DevIC)*, pages 163–167, 2023. DOI: https://doi.org/10.1109/DevIC57758.2023.10134784.

[13] S. Agarwal, G. Klimeck, and M. Luisier. “Leakage-reduction design concepts for low-power vertical tunneling field-effect transistors.”. *IEEE Electron Device Lett.*, 31(6):621–623, 2010. DOI: https://doi.org/10.1109/LED.2010.2046011.

[14] U. E. Avci, D. H. Morris, and I. A. Young. “Tunnel field effect transistors: prospects and challenges.”. *IEEE J. Elect. Dev. Soc.*, 3 (3):88–95, 2015. DOI: https://doi.org/10.1109/JEDS.2015.2390591.

[15] A. Vladimirescu, A. Amara, and C. Anghel. “An analysis on the ambipolar current in Si double-gate tunnel FETs.”. *Solid-State Electron*, 70:67–72, 2012. DOI: https://doi.org/10.1016/j.sse.2011.11.009.

[16] M. J. Kumar and S. Janardhanan. “Doping-less tunnel field effect transistor: Design and investigation.”. *IEEE Trans Electron Devices*, 60(10):3285–3290, 2013. DOI: https://doi.org/10.1109/TED.2013.2276888.

[17] K. Boucart and A. M. Ionescu. “Double-gate tunnel FET with high-k gate dielectric.”. *IEEE Trans Electron Devices*, 54(7):1725–1733, 2007. DOI: https://doi.org/10.1109/TED.2007.899389.

[18] S. Saurabh and M. J. Kumar. “Impact of strain on drain current and threshold voltage of nanoscale double gate tunnel field effect transistor: Theoretical investigation and analysis.”. *Jpn. J. Appl. Phys.*, 48(6R):064503, 2009. DOI: https://doi.org/10.1143/JJAP.48.064503.

[19] D. B. Abdi and M. J. Kumar. “n-built N^+ pocket p-n-p-n tunnel field-effect transistor. ”. *IEEE Electron Device Lett.*, 35(12):1170–1172, 2014. DOI: https://doi.org/10.1109/LED.2014.2362926.

[20] W. Cao, C. J. Yao, G. F. Jiao, D. Huang, H. Y. Yu, and M. F. Li. “Improvement in reliability of tunneling field-effect transistor with p-n-i-n structure.”. *IEEE Trans Electron Devices*, 58(7):2122–2126, 2011. DOI: https://doi.org/10.1109/TED.2011.2144987.

[21] B. R. Raad, K. Nigam, D. Sharma, and P. N. Kondekar. “Performance investigation of bandgap, gate material work function and gate dielectric engineered TFET with device reliability improvement.”. *Superlattices Microstruct*, 94:138–146, 2016. DOI: https://doi.org/10.1016/j.spmi.2016.04.016.

[22] B. R. Raad, D. Sharma, K. Nigam, and P. Kondekar. "Physics-based simulation study of high-performance gallium arsenide phosphide-indium gallium arsenide tunnel field-effect transistor.". *IET Micro. Nano Let.*, 11(7):366–368, 2016.
DOI: https://doi.org/10.1049/mnl.2016.0050.

[23] Z. Yang. "Tunnel field-effect transistor with an L-shaped gate.". *IEEE Electron Device Lett.*, 37(7):839–842, 2016.
DOI: https://doi.org/10.1109/LED.2016.2574821.

[24] S. Chen, S. Wang, H. Liu, W. Li, Q. Wang, and X. Wang. "Symmetric U-shaped gate tunnel field-effect transistor.". *IEEE Trans Electron Devices*, 64(3):1343–1349, 2017.
DOI: https://doi.org/10.1109/TED.2017.2647809.

[25] W. Y. Choi and W. Lee. "Hetero-gate-dielectric tunneling field effect transistors. ". *IEEE Trans Electron Devices*, 57(9):2317–2319, 2010.
DOI: https://doi.org/10.1109/TED.2010.2052167.

[26] M. J. Lee and W. Y. Choi. "Effects of device geometry on hetero-gate-dielectric tunneling field-effect transistors.". *IEEE Electron Device Lett.*, 33(10):1459–1461, 2012.
DOI: https://doi.org/10.1109/LED.2012.2206790.

[27] J. Madan and R. Chaujar. "Gate drain underlapped-PNIN-GAA-TFET for comprehensively upgraded analog/RF performance.". *Superlattices Microstruct*, 102:17–26, 2017.
DOI: https://doi.org/10.1016/j.spmi.2016.12.034.

[28] M. Ebrahimnia, S. A. S. Ziabari, and A. Kiani-Sarkaleh. "A design of improved nanoscale U-Shaped TFET by energy band modification for high performance digital and analog/RF applications.". *International Journal of Nano Dimension*, 12(3):279–292, 2021.
DOI: https://doi.org/10.22034/IJND.2021.681127.

[29] A. Shaker, M. El Sabbagh, and M. M. El-Banna. "Influence of drain doping engineering on the ambipolar conduction and high-frequency performance of TFETs.". *IEEE Trans Elect. Dev.*, 64(9):3541–3547, 2017.
DOI: https://doi.org/10.1109/TED.2017.2724560.

[30] S. Sahoo, S. Dash, S. R. Routray, and G. P. Mishra. "Impact of drain doping engineering on ambipolar and high-frequency performance of ZHP line-TFET.". *Semicond.Sci. Technol*, 35(6):065003, 2020.
DOI: https://doi.org/10.1088/1361-6641/ab7ce7.

[31] S. Garg and S. Saurabh. "Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis.". *Superlattices Microstruct*, 113:261–270, 2018.
DOI: https://doi.org/10.1016/j.spmi.2017.11.002.

[32] C. Li, X. Zhao, Y. Zhuang, Z. Yan, J. Guo, and R. Han. "Optimization of L-shaped tunneling field-effect transistor for ambipolar current suppression and analog/RF performance enhancement.". *Superlattices Microstruct*, 115:154–167, 2018.
DOI: https://doi.org/10.1016/j.spmi.2018.01.025.

[33] C. K. Pandey, D. Dash, and S. Chaudhury. "Improvement in analog/RF performances of SOI TFET using dielectric pocket.". *Int. J. Electron*, 107(11):1844–1860, 2020.
DOI: https://doi.org/10.1080/00207217.2020.1756439.

[34] M. Ebrahimnia, S. A. Sedigh Ziabari, and A. Kiani-sarkaleh. "Influence analysis of dielectric pocket on ambipolar behavior and high-frequency performance of dual material gate oxide stack-double gate Nano-Scale TFET.". *J. Nanoanalysis*, 9(2):90–98, 2022.
DOI: https://doi.org/10.22034/jna.2022.1943631.1277.

[35] M. Ebrahimnia, S. A. S. Ziabari, and A. Kiani-sarkaleh. "Analytical modeling for a new structure of dielectric pocket-based dual material double gate TFET with gate oxide stack.". *Silicon*, 15(7):3215–3224, 2023.
DOI: https://doi.org/10.1007/s12633-022-02229-x.

[36] S. Basak, P. K. Asthana, Y. Goswami, and B. Ghosh. "Leakage current reduction in junctionless tunnel FET using a lightly doped source.". *Applied Physics A.*, 118:1527–1533, 2015.
DOI: https://doi.org/10.1007/s00339-014-8935-9.

[37] B. Ghosh and M. W. Akram. "Junctionless tunnel field effect transistor. ". *IEEE Electron Device Lett.*, 34(5):584–586, 2013.
DOI: https://doi.org/10.1109/LED.2013.2253752.

[38] S. Anand, S. I. Amin, and R. K. Sarin. "Performance analysis of charge plasma based dual electrode tunnel FET.". *Journal Semicond*, 37(5):054003, 2016.
DOI: https://doi.org/10.1088/1674-4926/37/5/054003.

[39] S. Hussain, N. Mustakim, M. Hasan, and J. K. Saha. "Performance enhancement of charge plasma-based junctionless TFET (JL-TFET) using stimulated n-pocket and heterogeneous gate dielectric.". *Nanotechnology*, 32(33):335206, 2021.
DOI: https://doi.org/10.1088/1361-6528/abec07.

[40] P. Bal, B. Ghosh, P. Mondal, M. W. Akram, and B. M. M. Tripathi. "Dual material gate junctionless tunnel field effect transistor.". *J Comput Electron*, 13:230–234, 2014.
DOI: https://doi.org/10.1007/s10825-013-0505-4.

[41] H. Xie, H. Liu, S. Wang, S. Chen, T. Han, and W. Li. "Improvement of electrical performance in heterostructure junctionless TFET based on dual material gate.". *Appl Sci.*, 10(1):126, 2019.
DOI: https://doi.org/10.3390/app10010126.

[42] S. Sharma and R. Chaujar. "Impact of tunnel gate process variations on analog/radio frequency (microwave) and small signal parameters of hetero-material tunneling interfaced charge plasma junctionless tunnel field effect transistor.". *Int J Circuit Theory Appl.*, 50(10): 3626–3641, 2022.
DOI: https://doi.org/10.1002/cta.3347.

[43] K. K. C. R. Koppolu. "The effect of a dual oxide-dual gate material and a sensitivity analysis on the performance of a junctionless tunnel FET.". *Silicon*, 1:11, 2024.
DOI: https://doi.org/10.1007/s12633-024-02964-3.

[44] S. Sharma and R. Chaujar. "RF, linearity and intermodulation distortion analysis with small-signal parameters extraction of tunable bandgap arsenide/antimonide tunneling interfaced JLTFET. ". *Microsyst Technol*, 28(12):2659–2667, 2022.
DOI: https://doi.org/10.1007/s00542-022-05273-0.

[45] A. Vanak, A. Amini, and S. H. Pishgar. "Improvements in reliability and RF performance of stacked gate JLTFET using p^+ pocket and heterostructure material.". *Silicon*, 15(9):4137–4147, 2023.
DOI: https://doi.org/10.1007/s12633-023-02330-9.

[46] K. Kumar, A. Kumar, V. Kumar, and S. C. Sharma. "Comparative investigation of band gap and gate metal engineered novel $Si_{0.2}Ge_{0.8}$/GaAs charge plasma-based JLTFET for improved electrical performance. ". *Silicon*, 15(11):4689–4702, 2023.
DOI: https://doi.org/10.1007/s12633-023-02387-6.

[47] K. Kumar, A. Kumar, and S. C. Sharma. "Electrical performance improvement of charge plasma-based junctionless TFET using novel coalescence of SiGe/GaAs and heterogeneous gate dielectric. ". *Applied Physics A.*, 129(1):23, 2023.
DOI: https://doi.org/10.1007/s00339-022-06309-y.

[48] S. Tirkey, D. Sharma, D. S. Yadav, and S. Yadav. "Analysis of a novel metal implant junctionless tunnel FET for better dc and analog/RF electrostatic parameters.". *IEEE Trans Electron Devices*, 64(9):3943–3950, 2017.
DOI: https://doi.org/10.1109/TED.2017.2730922.

[49] B. V. Chandan, K. Nigam, S. Tirkey, and D. Sharma. "Metal-strip approach on junctionless TFET in the presence of positive charge.". *Appl Phys A.*, 125:1–12, 2019.
DOI: https://doi.org/10.1007/s00339-019-2966-1.

[50] A. Vanak and A. Amini. "Use of metal strip in stacked gate oxide JLTFET improves device quality and single-event-transient effect.". *Materials Science and Engineering: B.*, 307:117526, 2024.
DOI: https://doi.org/10.1016/j.mseb.2024.117526.

[51] S. Kumar, E. Goel, K. Singh, B. Singh, P. K. Singh, K. Baral, and S. Jit. "2-D analytical modeling of the electrical characteristics of dual-material double-gate TFETs with a SiO2/HfO2 stacked gate-oxide structure.". *IEEE Trans Electron Devices*, 64(3):960–968, 2017.
DOI: https://doi.org/10.1109/TED.2017.2656630.

[52] K. Eyvazi and M. A. Karami. "A new junction-less tunnel field-effect transistor with a SiO_2/HfO_2 stacked gate oxide for DC performance improvement.". *2020 28th Iran. Conf. Electr. Eng. (ICEE)*, pages 1–4, 2020.
DOI: https://doi.org/10.1109/ICEE50131.2020.9260621.

[53] S. L. Tripathi, R. Patel, and V. K. Agrawal. "Low leakage pocket junction-less DGTFET with biosensing cavity region. ". *Turkish J Electr Eng Comput Sci.*, 27(4):2466–2474, 2019.
DOI: https://doi.org/10.3906/elk-1807-186.

[54] S. Tirkey, K. Nigam, S. Pandey, D. Sharma, and P. Kondekar. "Investigation of gate material engineering in junctionless TFET to overcome the trade-off between ambipolarity and RF/linearity metrics.". *Superlattices Microstruct*, 109:307–315, 2017.
DOI: https://doi.org/10.1016/j.spmi.2017.03.059.

[55] H. Aghandeh and S. A. S. Ziabari. "Gate engineered heterostructure junctionless TFET with Gaussian doping pro le for ambipolar suppression and electrical performance improvement.". *Superlattices Microstruct*, 111:103–114, 2017.
DOI: https://doi.org/10.1016/j.spmi.2017.06.018.

[56] K. Kumar, A. Kumar, V. Kumar, A. Jain, and S. C. Sharma. "Ambipolarity suppression of band gap and gate dielectric engineered novel $Si_{0.2}Ge_{0.8}$/GaAs JLTFET using gate overlap technique.". *Silicon*, 15 (18):7837–7854, 2023.
DOI: https://doi.org/10.1007/s12633-023-02624-y.

[57] "ATLAS device simulator.". *Silvaco Inc. Santa Clara*, 2018.

[58] Y. Zhao, C. Wu, and Q. Huang. "A novel tunnel FET design through adaptive bandgap engineering with constant sub-threshold slope over 5 decades of current and high I_{ON}/I_{OFF} ratio.". *IEEE Electron Device Lett.*, 38:540–543, 2017.
DOI: https://doi.org/10.1109/LED.2017.2679031.

[59] N. Bagga, N. Chauhan, S. Banchhor, D. Gupta, and S. Dasgupta. "Demonstraion of a novel tunnel FET with channel sandwiched by drain.". *Semicond. Sci. Technol*, 35(1):015008, 2019.
DOI: https://doi.org/10.1088/1361-6641/ab5434.

[60] R. W. Johnson, A. Hultqvist, and S. F. Bent. "A brief review of atomic layer deposition: from fundamentals to applications.". *Mater. Today.*, 17(5):236–246, 2014.
DOI: https://doi.org/10.1016/j.mattod.2014.04.026.

[61] K. Y. Na and Y. S. Kim. "Silicon complementary metal-oxide-semiconductor field-effect transistors with dual work function gate. ". *Japanese J Appl Physics*, 45(12R):9033, 2006.
DOI: https://doi.org/10.1143/JJAP.45.9033.

[62] P. K. Verma and S. K. Gupta. "An improved analog/RF and linearity performances with small-signal parameter extraction of virtually doped recessed source/drain dopingless junctionless transistor for radio-frequency applications.". *Silicon*, 13(5):1519–1539, 2021.
DOI: https://doi.org/10.1007/s12633-020-00518-x.

[63] K. Nigam, S. V. Singh, and P. Kwatra. "Investigation and design of stacked oxide polarity gate JLTFET in the presence of interface trap charges for analog/RF applications.". *Silicon*, 14:1–18, 2021.
DOI: https://doi.org/10.1007/s12633-021-01162-9.