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Digital and analog performance enhancement of nanotube heterojunctionless tunnel FET using core-shell gate technology

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Original Research

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Abstract:

This paper introduces a nanotube heterojunctionless tunneling field-effect transistor (NT-HJLTFET) that combines core-shell gate technology with a $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ heterojunction to enhance device performance. The NT-HJLTFET achieves an I_{ON}/I_{OFF} ratio of 9.84 × 10^{13}, an average subthreshold slope (SS) of 9.4 mV/dec, I_{ON} of 6.4 mA, transconductance (g_m) of 17.5 mS, and unit gain cutoff frequency (f_T) of 42.7 THz. These results represent a significant improvement in performance, including a nearly two orders of magnitude increase in I_{ON}, g_m, and f_T compared to silicon-based nanotube junctionless tunneling field-effect transistor (NT-JLTFET). The NT-HJLTFET also exhibits a five orders of magnitude enhancement in I_{ON}/I_{OFF} and a 76% improvement in SS. Additionally, the presence of defects is shown to decrease f_T, impacting the device's high-frequency response. These findings suggest that the NT-HJLTFET is a promising candidate for use in both digital and analog applications in integrated circuits.

Keywords: Heterojunction; TFET; Nonlocal BTBT; Transconductance; Work function

1. Introduction

Tunneling field-effect transistor (TFET) has attracted many researchers' attention due to the subthreshold slope (SS) of less than 60 mV/dec and low leakage current [1–6]. However, TFET has low ON-state current (I_{ON}) due to the band-to-band tunneling (BTBT) mechanism, which limits its application in integrated circuits [7]. Studies have proposed using materials with a narrow bandgap [8–11] as well as III-V materials with staggered/broken bandgaps to increase I_{ON} in TFET [9–16].

Various gate shapes have been proposed to improve TFET electrical characteristics, including double gate (DG), gate-all-around (GAA) and core/shell gates [9–16]. Nanowire gate-all-around TFET (NWGAA-TFET) have been proposed to reduce leakage current and improve subthreshold slope [17]. The electrostatic control of gate over the channel in NWGAA-TFET is more than that of DG-TFET. As a result, NWGAA-TFET has lower leakage current and better subthreshold slope compared to DG-TFET [18, 19]. Also, NWGAA-TFET has high integration for circuit functionality [13].

Low ON-state current is among the problems of silicon-based NWGAA-TFET [20, 21], for solving which the nanotube TFET has been proposed, which includes a core-shell gate [17, 22–24]. In nanotube TFETs, shell and core gates are used, respectively, as all-around and cylindrical, which increase I_{ON} compared to NWGAA-TFETs [13, 17, 22, 25, 26]. The existence of ultra-sharp doping concentration gradient at source/channel and drain/channel junctions is among the main problems of nanotube TFETs, which complicates its manufacturing process in the nanometer regime [17, 22].

The present study mainly aims to propose a nanotube TFET, which has acceptable electrical characteristics for digital and analog applications in integrated circuits and resolves the problems of doping concentration gradient at source/channel and drain/channel junctions. In this paper, it introduced the nanotube junctionless TFET (NT-JLTFET), a novel structure for the first time in this application. The

source-channel-drain doping in NT-JLTFET is of one type and level. The problems caused by the ultra-sharp doping concentration gradient at source/channel and drain/channel junctions are solved. Compared to the regular NT-TFET structure, NT-JLTFET has additional core-shell gates, called p-auxiliary, in the source region.

The simulation results indicate silicon-based NT-JLTFET has better *SS* and greater I_{ON} compared to NW-JLTFET with similar dimensions. It is suggested to use $Ga_{0.8}In_{0.2}As$ as the drain-channel material and $Ga_{0.85}In_{0.15}Sb$ as the source material to improve NT-JLTFET electrical characteristics. The motivation behind this work stems from the limitations of silicon-based NT-JLTFET, particularly their low ON-state current. To address these challenges, this study proposes the use of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ heterojunctions in NT-JLTFET, which offer a narrower and staggered bandgap, thereby enhancing the band-to-band tunneling (BTBT) mechanism and increasing I_{ON}. Additionally, the core-shell gate configuration is introduced to provide superior electrostatic control over the channel, further reducing the subthreshold slope (*SS*) and improving the I_{ON}/I_{OFF} ratio. This approach (NT-JLTFET) not only simplifies the fabrication process by eliminating the need for ultra-sharp doping profiles but also significantly enhances the electrical performance of the device. $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ NT-JLTFET is known as NT-HJLTFET.

The importance of structural parameters such as work function of shell gate (*WFS*), work function of core gate (*WFC*), doping (N_D), body thickness (T_b) and spacer width (W_{sio2}) between p-auxiliary (PG) and control gates (CG) in NT-HJLTFET performance is investigated. Although using $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ heterojunction improve NT-HJLTFET electrical characteristics, our simulation results show defects at $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ interface affects the subthreshold characteristics. The simulation results indicate average *SS*, ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) and I_{ON} of NT-HJLTFET structure are significantly improved compared to the recently proposed structures [15, 25, 27, 28]. Moreover, our investigations indicate NT-HJLTFET has a remarkable transconductance (g_m) and unity gain cutoff frequency (f_T). Therefore, the NT-HJLTFET is not only novel but also a strong candidate for future digital and analog applications in integrated circuits.

This paper is organized into four sections. Section II presents the device structure and simulation models. Section III provides the simulation results of NT-HJLTFET. Finally, Section IV presents the conclusion.

2. Materials and methods

Previous studies have shown that using a material with a larger bandgap in the drain-channel region compared to the source region can significantly reduce the ambipolarity behavior in Heterojunctionless TFET (HJLTFET) devices [8–12]. In this study, $Ga_XIn_{1-X}As$ was chosen for the drain-channel region and $Ga_YIn_{1-Y}Sb$ for the source region. The mole fraction of X was varied from 0 to 1 in increments of 0.05, while the mole fraction of Y was similarly adjusted, enabling a systematic evaluation of the optimal X and Y values. Simulation results showed that the best device performance in terms of I_{ON}/I_{OFF} ratio, *SS*, and threshold voltage (V_{th}) was achieved with X=0.8 and Y=0.85 [29, 30]. Therefore, $Ga_{0.8}In_{0.2}As$ was selected as the drain-channel material and $Ga_{0.85}In_{0.15}Sb$ as the source material to optimize the electrical characteristics of the NT-JLTFET.

Fig. 1a shows the three-dimensional structure of NW-JLTFET. Fig. 1b illustrates the three-dimensional schematic of NT-JLTFET with a silicon body. Fig. 1c indicates the three-dimensional schematic of NT-HJLTFET simulated in this paper. As illustrated in Fig. 1c, the NT-HJLTFET

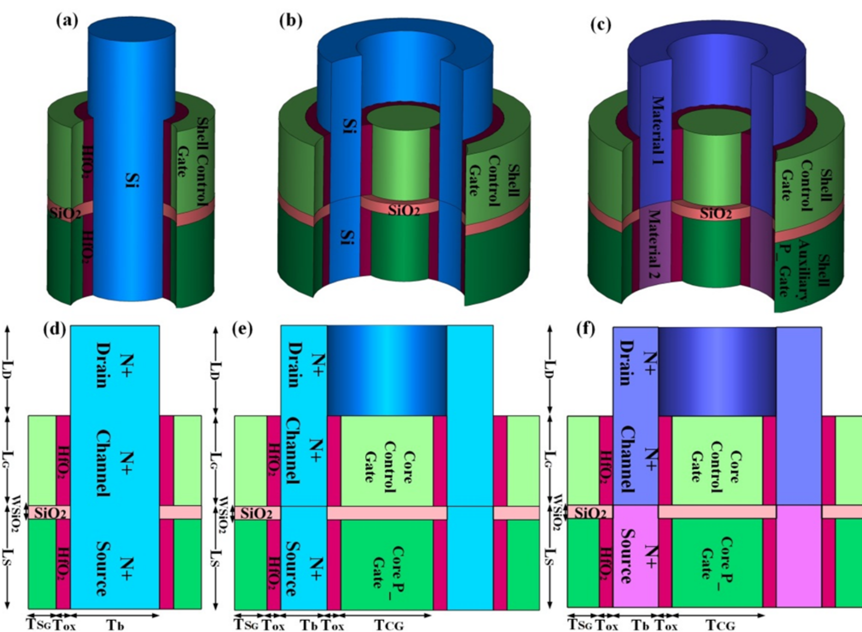


Figure 1. 3D Schematic of (a) NW-JLTFET, (b) NT-JLTFET, and (c) NT-HJLTFET. 2D schematic of (d) NW-JLTFET, (e) NT-JLTFET, and (f) NT-HJLTFET (not to scale).

Table 1. Structural parameters of NW-JLTFET, NT-JLTFET and NT-HJLTFET (related to structures of Fig.1).

Parameters	NW-JLTFET	NT-JLTFET	NT-HJLTFET NT-JLTFET
L_D, L_G, L_S (nm)	20	20	20
T_b (nm)	10	10	10
T_{CG} (nm)	-	25	25
T_{SG} (nm)	5	5	5
T_{OX} (nm)	2	2	2
WFC (eV)		4.3	4.3
WFS (eV)	4.3	4.3	4.3
WFPG (eV)	5.9	5.9	5.9
$N_D(cm^{-3})$	1×10^{19}	1×10^{19}	1×10^{18}
W_{SiO2} (nm)	2	2	2
Material1	Si	Si	$Ga_{0.85}In_{0.15}Sb$
Material2	Si	Si	$Ga_{0.8}In_{0.2}As$

structure utilizes $Ga_{0.8}In_{0.2}As$ in the drain-channel region (as the Materil1) and $Ga_{0.85}In_{0.15}Sb$ in the source region (as the Materil2), optimizing device performance.

Figs. 1d, 1e and 1f indicate two-dimensional cross-sections of the simulated devices. Table 1 presents the structural parameters of the simulated devices. To increase the electrostatic control of gate over the channel, gate-all-around and cylindrical gates were placed, respectively, in the shell and core of devices shown in Figs. 1b and 1c. The work function of p-auxiliary gate (*WFPG*) was chosen in a way that doping of source region changed from n- to p-type [31]. The work function of core-shell gates was chosen in a way that channel doping became intrinsic in the thermal equilibrium. Devices shown in Fig. 1 behave like a p-i-n diode in thermal equilibrium. *WFPG* was equal to 5.9 eV, obtained by considering Pt as the gate electrode [32]. The work function of core-shell gates was 4.3 eV, which could be obtained using molybdenum with nitrogen implant dose as the metal [32].

A numerical device simulator was employed to evaluate the performance of the proposed devices, incorporating a range of sophisticated models to ensure accuracy. The non-local band-to-band tunneling (non-local BTBT) model was chosen to capture the essential tunneling effects, which are critical for determining the electrical characteristics of the simulated devices [9]. The Hansch model was used to account for quantum confinement effects as well as defects at the oxide/semiconductor interface, providing a comprehensive view of the interface behavior [10]. Mobility dependence on vertical field, doping density, and temperature was calculated using the Lombardi model, ensuring that variations in mobility were accurately represented [10]. Additionally, to quantify leakage currents, the direct generation/recombination model and the Shockley-Read-Hall (SRH) recombination model were applied, providing a robust estimation of leakage under various conditions [9]. Due to the high doping concentration in the proposed devices, a band gap narrowing model was also implemented [9]. These models, chosen for their ability to accurately simulate the key physical phenomena, ensured that the simulation results were both reliable and reflective of the actual device behavior.

To show the simulation accuracy, an HJL-TFET with structural parameters reported in [12], consisting of GaAs material in both drain and channel regions and Ge material in the source region, was simulated. Fig. 2 compares our numerical simulations and the simulation reported in [12]. As could be observed, our numerical simulation results had an acceptable agreement with the simulation results reported in [12]. Therefore, the models used in the simulation in this study are accurate enough.

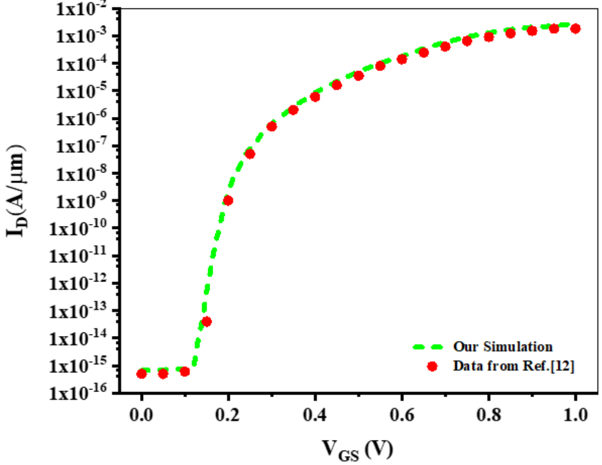


Figure 2. Calibration with the published result, $I_D - V_{GS}$ characteristics of 20 nm gate length HJL-TFET reported in Ref. [12].

3. Results and discussions

Fig. 3a compares ON-state energy band profiles of NW-JLTFET, NT-JLTFET, and NT-HJLTFET. As could be observed, the electron tunneling region width at the tunneling junction, i. e. , source/channel junction, of NT-JLTFET decreased compared to NW-JLTFET. The existence of core gate increased the control of gate over the tunneling junction and, then, reduced the tunneling width of NT-JLTFET compared to NW-JLTFET. Also, Fig. 3a illustrates total drain current is calculated along the whole circumference ($2\pi r$) of the device where r is the nanotube channel radius [13].

As indicated in Fig. 3b, I_{ON} (i. e. , drain current under bias conditions of V_{GS} = 1 V and V_{DS} = 1 V) of NT-JLTFET was equal to 4.46×10^{-5} A/2π4, which improved

Figure 3. (a) ON-state energy band profiles, (b) $I_D - V_{GS}$ characteristics, and (c) Off-state energy band profiles of NW-JLTFET, NT-JLTFET, and NT-HJLTFET devices. The ON-state profiles illustrate the tunneling junction behavior under bias conditions (V_{GS}=V_{DS}=1 V), while the off-state (V_{GS}=0 V and V_{DS}=1 V), profiles in (c) show the wide tunneling barriers that prevent electron flow in the off state. The $I_D - V_{GS}$ characteristics in (b) compare the current-voltage behavior.

by one order of magnitude compared to NW-JLTFET. As mentioned above, the core gate reduced electron tunneling width and, then, increased electron tunneling rate in NT-JLTFET compared to NW-JLTFET. Additionally using $Ga_{0.85}In_{0.15}Sb/Ga_{0.8}In_{0.2}$ as heterojunction at the tunneling junction reduced the tunneling width of NT-HJLTFET compared to NT-JLTFET, see inset of Fig. 3a. Fig. 3b compares $I_D - V_{GS}$ characteristic of the simulated devices. As a result, I_{ON} of NT-JLTFET was greater than that of NW-JLTFET. Table 2 compares electrical characteristics of NW-JLTFET, NT-JLTFET and NT-HJLTFET. In this study, V_{GS} at the drain current of 10^{-7} A/2πr was considered as the threshold voltage (V_{th}) [9]. Also, drain current under bias condition of V_{GS} = 0 V and V_{DS} = 1 V was considered as OFF-state current (I_{OFF}) [31]. The simulation results showed heterojunction increased electric field at the tunneling junction and, consequently, increased electron tunneling rate of NT-HJLTFET compared to NT-JLTFET. Accordingly, I_{ON} of NT-HJLTFET was almost two orders of magnitude greater than that of NT-JLTFET (Table 2). The average *SS* of NT-HJLTFET was 9.4 mV/dec which improved by 76% and 81% compared to NT-JLTFET and NW-JLTFET, respectively. V_{th} of NT-HJLTFET was 0.09 V, which reduced by 75% and 84% compared to NT-JLTFET and NW-JLTFET, respectively.

In addition to the ON-state energy band profiles, the OFF-state band structures of NT-HJLTFET, NT-JLTFET, and NW-JLTFET are crucial for understanding their low I_{OFF} characteristics. As shown in Fig. 3c, is, the band gap in the OFF-state ensures a wide tunneling barrier, effectively blocking electron tunneling from the source to the channel (see inside of Fig. 3c). This result in significantly lower leakage currents in NT-HJLTFET compared to NT-JLTFET and NW-JLTFET, further enhancing its I_{ON}/I_{OFF} ratio. The I_{ON}/I_{OFF} ratio of NT- HJLTFET was 9.84 × 10^{13}, which improved by about five orders of magnitude compared to NT-JLTFET and NW-JLTFET. Our investigations showed using $Ga_{0.85}In_{0.15}Sb/Ga_{0.8}In_{0.2}As$ heterojunction as well as core-shell gate greatly improved NT-HJLTFET electrical characteristics compared to other devices proposed in this study.

3.1 Importance of structural parameters on NT-HJLTFET performance

To investigate the importance of the work function of the control gate (*WFCG*) in NT-HJLTFET performance, both *WFC* and *WFS*are increased from 4.3 eV to 5 eV. The simulations results showed increasing *WFC*=*WFG* from 4.3 eV to 5 eV increased tunneling region width and, then, V_{th} became greater. As a result, I_{ON} decreased (Fig. 4). Also,

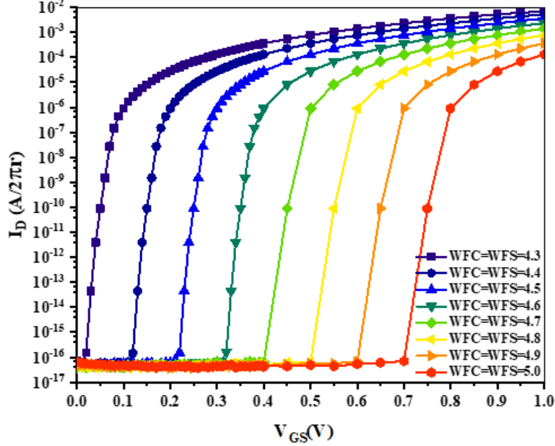


Figure 4. $I_D - V_{GS}$ characteristic of NT-HJLTFET considering changes of WFC=WFS at $WFPG$=5.7 eV.

Table 2. Electrical characteristics of NW-JLTFET, NT-JLTFET and NT-HJLTFET.

Design	I_{ON} (A/2πr)	I_{OFF}(A/2πr)	SS(mV/dec)	V_{th}(V)	I_{ON} / I_{OFF}
NW-JLTFET	4.82×10^{-6}	4.52×10^{-15}	50	0.55	1.07×10^{9}
NT-JLTFET	4.46×10^{-5}	3.5×10^{-14}	40	0.36	1.26×10^{9}
NT-HJLTFET	6.4×10^{-3}	6.3×10^{-17}	9.4	0.09	9.84×10^{13}

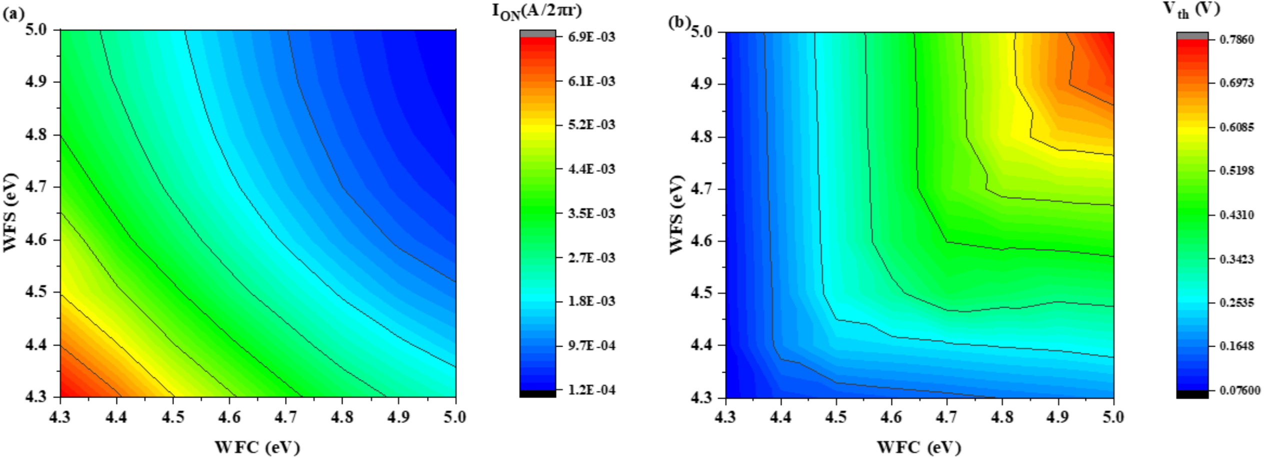


Figure 5. Two-dimensional matrix of changes: (a) I_{ON}, (b) V_{th} considering WFC and WFS changes form WFC=WFS=4.3 eV to WFC=WFS=5 eV.

the simulation results revealed drain current significantly increased at WFS=WFC < 4.3 eV under bias conditions of V_{GS}=0 V and V_{DS}=1 V and the device did not turn off afterward. Further, WFC increased from 4.3 eV to 5 eV with steps of 0.1 eV and WFSchanged from 4.3 eV to 5 eV per step of WFC. I_{ON} and V_{th} were extracted for different variations of WFC and WFS. Fig. 5a and Fig. 5b, respectively, show the two-dimensional matrix of I_{ON} changes and the two-dimensional matrix of V_{th} changes with changes in WFC and WFS.

Fig. 5a shows the highest and lowest I_{ON} values occur at $WFC = WFS$=4.3 eV and $WFC = WFS$=5 eV, respectively. Fig. 6a compares ON-state energy band profile at $WFC = WFS$=4.3 eV and $WFC = WFS$=5 eV. As could be observed, the tunneling region width at $WFC = WFS$=4.3 eV was less than that of $WFC = WFS$=5 eV. As a result, the electron tunneling rate at $WFC = WFS$=4.3 eV was greater than that of $WFC = WFS$=5 eV. Consequently, the electron density in the device channel at $WFC = WFS$=4.3 eV was greater than that of $WFC = WFS$=5 eV, see Fig. 6b. As a result, I_{ON} at $WFC = WFS$=4.3 eV was greater than that of $WFC = WFS$=5 eV.

As mentioned above, the tunneling region width at $WFS = WFC$=4.3 eV was less than that of $WFS = WFC$=5 eV. Therefore, the threshold voltage at $WFS = WFC$=4.3 eV was expected to be less than that of $WFS = WFC$=5 eV (Fig. 5b). Fig. 7a shows $I_D - V_{GS}$ characteristics at different V_{DS} values. As can be observed the device is turned on at V_{DS}=0.05 V, it shows that changes in I_{ON} were significant with increasing V_{DS}, while I_{OFF} changes could be ignored. Fig. 7b shows the $g_m = \partial I_D / \partial V_{GS}$ value of NT-HJLTFET at different V_{DS}. The maximum g_m (g_{mmax}) value was obtained as 17.5, 6.07, 0.093, and 0.012 mS at V_{DS} of 1, 0.5, 0.2 and 0.05 V, respectively. As could be observed, the g_m value was maximum for V_{DS}=0.5 V and V_{DS}=0.2 V at V_{GS}=0.65 and V_{GS}=0.4 V, respectively. Therefore, the NT-HJLTFET could be used at voltages less than 1 V. It can also be said that the NT-HJLTFET device is suitable for low power applications. Fig. 7b shows that the gm value decreased with reducing V_{DS}. In fact, the tunneling region width decreased in the ON state with increasing V_{DS} (Fig. 7c) and significantly increased I_{ON}. Consequently, g_m increased. The simulations results indicated tunneling region width was significant at V_{GS}=0 V and the importance of increasing V_{DS} from 0.05 V

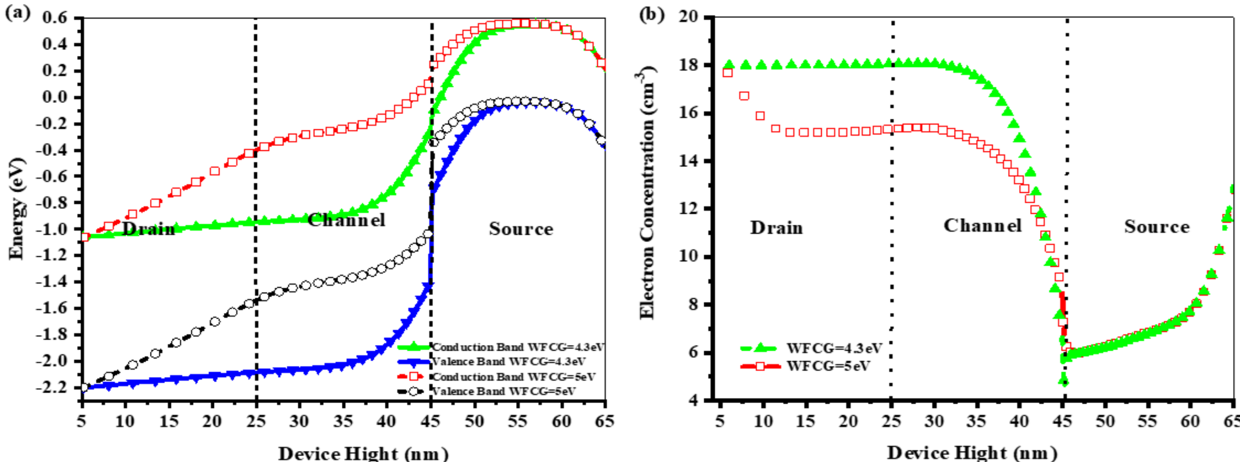


Figure 6. (a) Energy bands, (b) Electron density of NT-HJLTFET at WFS=WFC=4.3 eV and WFS=WFC=5 eV in the ON state (VGS=VDS=1 V).

Figure 7. (a) $I_G - V_{GS}$ characteristic, (b) g_m at different V_{DS} values, in different values of V_{DS} (c) comparing energy bands in the ON state at V_{DS}=1 V and V_{DS}=0.05 V of NT-HJLTFET with specifications stated in Table 1.

to 1 V in the tunneling region width could be ignored. As a result, I_{OFF} changes could be ignored with increasing V_{DS}. Fig. 8a shows $I_D - V_{GS}$ characteristic at different source-channel-drain doping values with the body thickness of 10 nm. I_{OFF} significantly increased with increasing N_D from 1×10^{18} to 1×10^{19}. The electron-hole density product increased in the simulated device channel with increasing N_D, see Fig. 8b. As a result, the channel resistance decreased and I_{OFF} increased, which was consistent with the results presented in [9]. Based on the simulations performed, in the ON state, the tunneling region width increased at N_D less than $1\times10_{18}$ and I_{ON} decreased. Fig. 8c shows $I_D - V_{GS}$ characteristic of NT-HJLTFET at different body thicknesses and N_D=1×10^{18}. The control of core and shell gates over the channel decreased with increasing body thickness. Therefore, I_{OFF} increased.

Our simulation results revealed NT-HJLTFET performance depended on the spacer width (W_{SiO2}) between PG and CG. In this study, W_{SiO2} changed from 2 nm to 6 nm to investigate the effect of W_{SiO2} on NT-HJLTFET performance. Fig. 9a shows $I_D - V_{GS}$ characteristic of NT-HJLTFET at different W_{SiO2} values. Inset of Fig. 9a displays the performance of the simulated devices in the above threshold region. The simulation results indicated the electric field at the tunneling junction at the source/channel interface decreased with increasing W_{SiO2}. As a result, the electron tunneling rate decreased in the ON state and, then, I_{ON} decreased. This was reflected by the threshold voltage shift

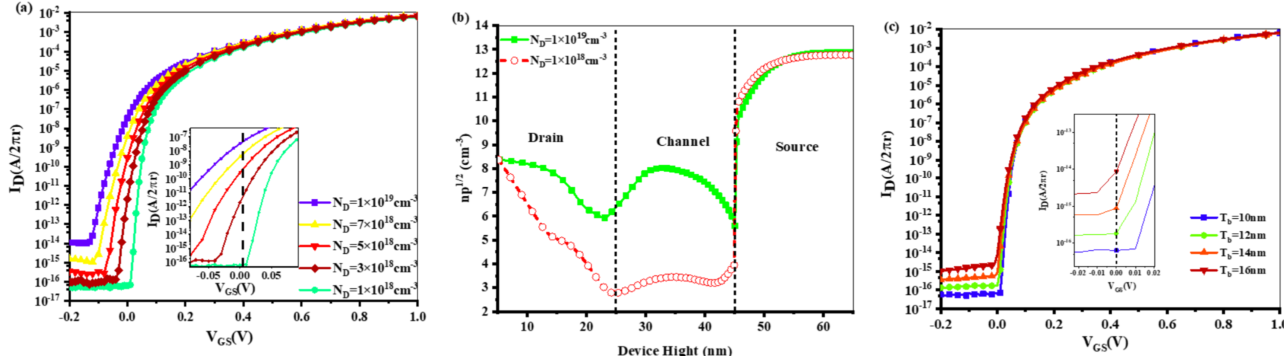


Figure 8. (a) $I_D - V_{GS}$ characteristic for various N_D values at a fixed T_b of 10 nm, (b) Vertical profile of $np^{1/2}$ taken across NT-HJLTFET with T_b=10 nm, for N_D=1×10^{18} (cm^{-3}) and N_D=1×10^{19} (cm^{-3}) (c) $I_D - V_{GS}$ characteristic for different T_b with N_D=1×10^{18} (cm^{-3}).

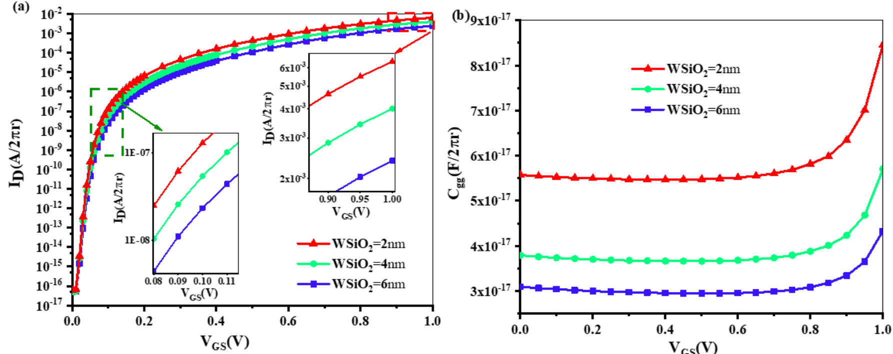


Figure 9. . (a) $I_D - V_{GS}$ characteristic, and (b) Cgg of NT-HJLTFET at three different values of W_{SiO2}.

Table 3. Intrinsic gate delay (τ), I_{ON}, and C_{gg} in different W_{SiO2} for NT-HJLTFET.

W_{SiO2}	I_{ON} (mA/2πr)	C_{gg} (fF/2πr)	Delay(τ) (fS)
2 nm	6.4	0.08	13
4 nm	4.0	0.05	14
6 nm	2.4	0.04	17

to greater values, see inset of Fig. 9a. Based on the simulations, I_{ON} has been decreased by 62% with change of W_{SiO2} from 2 nm to 6 nm.

Intrinsic gate delay, $\tau = C_{gg}V_{DD}/I_{ON}$, is one of the most important parameters of device performance in digital applications. C_{gg} is the total gate-to-gate capacitance, I_{ON} is the ON-state current and V_{DD} is the supply voltage [9].

C_{gg} plays an important role in determining τ of a transistor. Fig. 9b shows C_{gg} as a function of V_{GS} for NT-HJLTFET at different W_{SiO2} values. To calculate C_{gg}, it was assumed that $V_{DS} = V_{DD}$=1 V and control gate voltage was swept between 0 V and 1 V at 1 MHz [9]. The simulation results revealed gate-source capacitance decreased with increasing W_{SiO2}. As a result, C_{gg} reduced. Table 3 compares τ, I_{ON} and C_{gg} values under bias conditions of $V_{GS} = V_{DS}$=1 V. As expected, I_{ON} and C_{gg} decreased with increasing W_{SiO2}. I_{ON} and C_{gg} compete in determining τ. The results presented in Table 3 show in determining τ, I_{ON} reduction prevailed over C_{gg} reduction with increasing W_{SiO2}. Thus, τ increased with increasing W_{SiO2}.

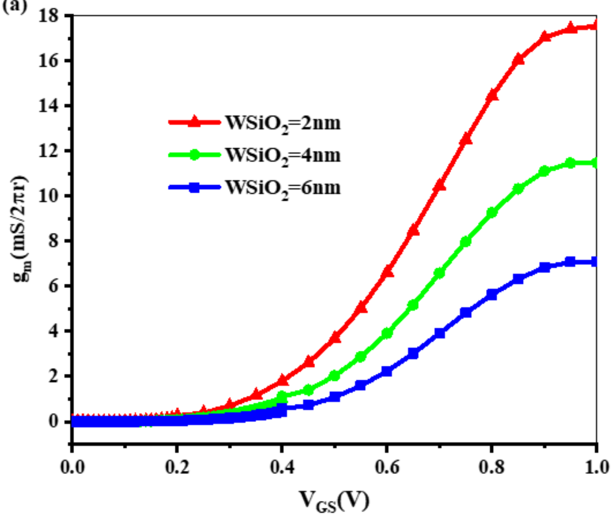
Fig. 10a shows g_m of NT-HJLTFET at different W_{SiO2} values. As could be observed, g_m decreased due to the decreased electron tunneling rate with increasing W_{SiO2}. Fig. 10b compares the unity gain cutoff frequency ($f_T = g_m/2\pi C_{gg}$) of NT-HJLTFET at different W_{SiO2} values, f_T=42.7 THz was obtained at V_{GS}=0.9 V and W_{SiO2}=2 nm, which improved by about 35% compared to W_{SiO2}=6 nm. The improvement of g_m at W_{SiO2}=2 nm in NT-HJLTFET compared to W_{SiO2}=6 nm improved f_T. The improvement of f_T at W_{SiO2}=2 nm compared to W_{SiO2}=4 nm could be ignored. It should be noted that although gm at W_{SiO2}=2 nm was larger than that at W_{SiO2}=4 nm, C_{gg} at W_{SiO2}=4 nm was smaller than that at W_{SiO2}=2 nm. As a result, the improvement of gm at W_{SiO2}=2 nm compared to W_{SiO2}=4 nm was compensated by increasing C_{gg}, and the improvement of f_T could be neglected. Considering that g_m=17 mS and f_T=42.7 THz at W_{SiO2}=2 nm, NT-HJLTFET could be an acceptable candidate for analog applications. It should be noted that increasing W_{SiO2} to values greater than 2 nm may be a feasible way to increase oxide breakdown voltage between CG and PG, but it reduces device performance. Reduction of W_{SiO2} to values less than 2 nm may lead to oxide breakdown between CG and PG. As a result, W_{SiO2} was considered 2 nm in our simulations.

3.2 NT-JLTFET and NT-HJLTFET device scaling

To investigate the short-channel effect of the simulated devices, drain induced barrier lowering (DIBL) was measured as follows [9]:

$$DIBL = \frac{V_{TVDS=1V} - V_{TVDS=0.05V}}{V_{DS=1V} - V_{DS=0.05V}}$$

where V_{TDS}=1 V and V_{TDS}=0.05 V represent the threshold voltage at V_{DS}=1 V and V_{DS}=0.05 V, respectively. The simulation results showed NW-JLTFET was in the subthreshold region at V_{DS}=0.05 V, calculating V_{TDS}=0.05 V was not possible and, consequently, *DIBL* was not calculated for this device. The vertical axis on the right side of Fig. 11a shows *DIBL* at different channel lengths (L_{ch}) of NT-JLTFET. Also, the vertical axis on the left side of Fig. 11a shows *DIBL* in NT-HJLTFET. *DIBL* was measured as 10.5 mV/V at the channel length of 20 nm in NT-HJLTEFT and *DIBL* was equal to 0.47 V/V in NT-JLTFET device. Therefore, *DIBL* of NT-HJLTFET was improved by about 44 times compared to that of NT-JLTFET, which was due to the better gate control in NT-HJLTFET. Fig. 11a illustrates *DIBL* changed by 8 mV/V and 100 mV/V in NT-HJLTFET and NT-JLTFET by reducing the channel length from 20 nm to 10 nm, respectively. Therefore, NT-



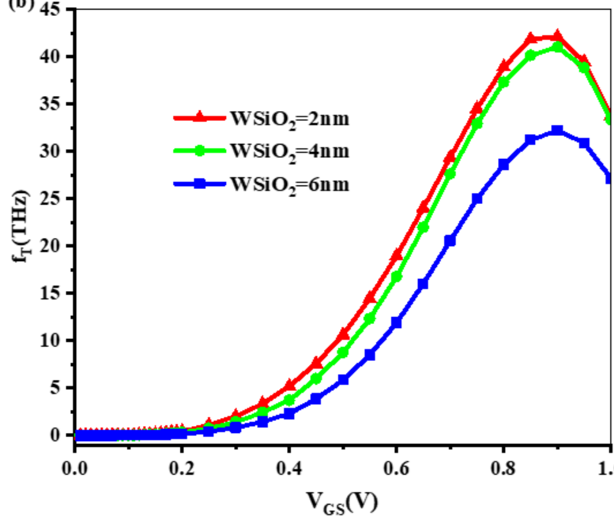


Figure 10. (a) g_m, (b) f_T as a function of V_{GS} at different W_{SiO2} values. Other structural parameters are the same as Table 1 and VDS=1 V for NT-HJLTFET.

Figure 11. (a) DIBL for NT-JLTFET and NT-HJLTFET in left and right vertical axis respectively, (b) Average *SS* of NT-JLTFET and NT-HJLTFET in different values of L_{ch} , (c) Energy band diagram in ON-state of NT-HJLTFET in L_{ch}=10 and 20 nm. (be noted to reach the comparable conditions of two profiles, the band profile of L_{ch}=10 nm, is shifted by 10 nm).

HJLTFET was more resistant to SCEs than NT-JLTFET. Fig. 11b indicates the average *SS* changes at different channel lengths of NT-JLTFET and NT-HJLTEFT. Contrary to what was expected, Fig. 11b shows the average *SS* in the simulated devices decreased by reducing the channel length. To further evaluate the physics of this phenomenon, Fig. 11c compares NT-HJLTFET energy bands around tunneling junction at channel lengths of 10 nm and 20 nm. It should be noted that for making a proper comparison of the tunneling width at the channel lengths of 20 nm and 10 nm, NT-HJLTFET energy bands with the channel length of 10 nm was shifted by 10 nm. As indicated in Fig. 11c, NT-HJLTFET energy bands were overlapped at channel lengths of 20 nm and 10 nm. Fig. 11c illustrates the tunneling width of the device with L_{ch}=10 nm is less than that of L_{ch}=20 nm. As a result, NT-HJLTFET with L_{ch}=10 nm was switched on at a smaller gate voltage than L_{ch}=20 nm and, then, the average *SS* decreased.
Table 4 compares digital performance of NT-HJLTFET proposed in this study with the recently proposed structures [15, 25, 27, 28]. I_{ON} of NT-HJLTFET with the gate length of 20 nm was improved by two orders of magnitude, three orders of magnitude, and two orders of magnitude compared to hetero-dielectric based silicon germanium source nanowire TFET (SiGe-S-NW-TFET) [25], silicon-germanium gate-all-around nanowire TFET (SiGe-GAA-NWTFET) [27] and GaSb/Si Vertical TFET with pocket (V-TFET-WP) [28] with the channel length (L_{Ch}) of 20 nm, respectively.
Despite the drift-diffusion mechanism in the strained tri-layer channel cylindrical gate-all-around FET (GAA FET) proposed in [15], I_{ON} of GAA FET was expected to be greater than that of TFETs. However, I_{ON} of NT-HJLTFET proposed in this study was improved by 300% compared to the GAA FET reported in [15]. The average *SS* of NT-HJLTFET was improved by 60%, 81%, 78% and 88% compared to SiGe-S-NW-TFET, SiGe-GAA-NWTFET, V-TFET-WP and GAA FET, respectively. Table 4 shows I_{ON}/I_{OFF} and V_{th} of NT-HJLTFET was significantly improved compared to the devices proposed in [15, 25, 27, 28]. NT-HJLTFET had significant g_m and f_T compared to the devices proposed in [33–35], see Table 5. g_m of NT-HJLTFET was 1000 times greater than that of germanium-silicon vertical tunnel field-effect transistor (Ge-Si-VTFET) [33] and hetero-metal gate, hetero-structure junctionless tunnel field effect transistor (HMG-HJLTFET) [33]. Also, g_m of NT-HJLTFET was improved by 70% compared to that of hybrid heterostructure-SOI-JLT (HH-SOI-JLT) proposed in [34]. f_T of NT-HJLTFET proposed in this study was about 100, 32 and 25 times greater than that of Ge-Si-VTFET, HMG-

Table 4. Digital characteristics performance comparison of NT-HJLTFET and recent study reported on [15, 25, 27, 28].

Design	L_{Ch}(nm)	I_{ON} (A/μm)	I_{OFF} (A/μm)	*SS*(mV/dec)	V_{th}(V)	I_{ON}/I_{OFF}
SiGe-S-NW-TFET[25]	20	1.166×10^{-5}	8.63×10^{-17}	23.75	0.37	1.35×10^{11}
SiGe-GAA-NWTFET[27]	20	6.63×10^{-6}	1.55×10^{-16}	51.37	0.49	4.28×10^{10}
V-TFET-WP [28]	20	1.89×10^{-5}	2.75×10^{-17}	43	0.45	6.8×10^{11}
GAA FET [15]	10	1.57×10^{-3}	5.5×10^{-9}	79	29	2.86×10^{5}
NT-HJLTFET	20	6.4×10^{-3}	6.3×10^{-17}	9.4	0.09	9.84×10^{13}

Table 5. Comparison g_m and f_T in NT-HJLTFET and devices proposed on [33–35].

Design	L_{Ch}(nm)	I_{ON} (A/μm)	g_m (mS/μm)	f_T (THz)
Ge-Si-VTFET [33]	20	5.5×10^{-5}	0.201	0.188
HMG-HJLTFET [34]	20	10.6×10^{-5}	0.35	1.28
HH-SOI-JLT [35]	20	-	10.3	1.6
NT-HJLTFET	20	6.4×10^{-3}	17.5	42.7

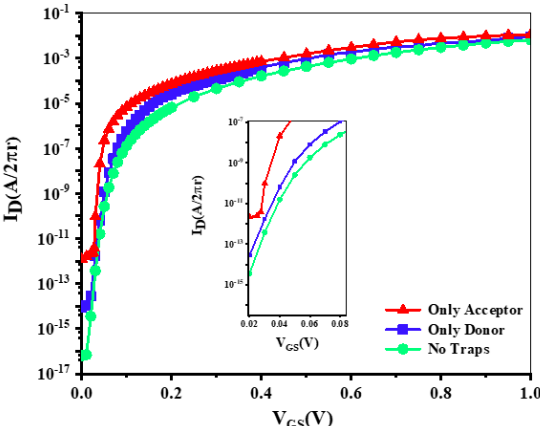


Figure 12. $I_D - V_{GS}$ characteristic in the presence of donor and acceptor defects at the source/channel interface of NT-HJLTFT.

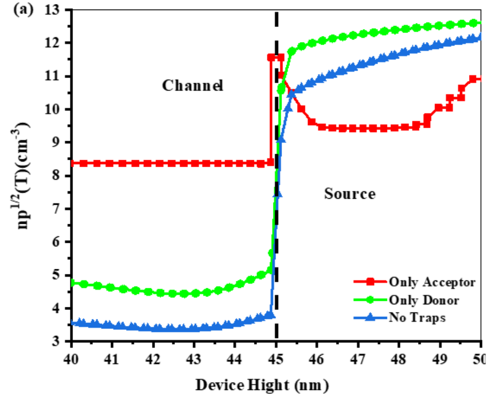
HJLTFET and HH-SOI-JLT, respectively. Based on the results presented in Tables IV and V, NT-HJLTFET proposed in this study could be suitable for digital and analog applications in integrated circuits.

3.3 Effect of defects on subthreshold behavior of NT-HJLTFET

The simulation results showed defects at the source/channel interface plays an important role in the subthreshold behavior of NT-HJLTFET. Defects at $Ga_{0.85}In_{0.15}Sb/Ga_{0.8}In_{0.2}As$ interface could be of donor or acceptor type and their density is between 105-107 cm^{-2} [36, 37].

To investigate the effect of source/channel defects on NT-HJLTFET performance, densities of donor and acceptor defects were considered 10^6 cm^{-2} and 10^7 cm^{-2}, respectively. These defects can significantly impact various performance metrics, such as V_{th}, I_{OFF}, f_T and g_m. Fig. 12 shows $I_D - V_{GS}$ characteristic of the simulated device considering defects. As indicated in Fig. 12, defects at the interface significantly increased I_{OFF} with acceptor defects increasing I_{OFF} by four orders of magnitude and donor defects increasing I_{OFF} by three orders of magnitude. Fig. 13a indicates the square root of product of electron-hole density $(np)^{1/2}$ around the tunneling junction of NT-HJLTFET in the OFF state. The presence of defects at the source/channel interface led to higher values of $(np)^{1/2}$ compared to the defect-free scenario. Fig. 13b demonstrates the recombination rate in the vicinity of the tunneling junction (in the OFF state) shifted toward the source/channel interface due to the defects. Furthermore, the maximum recombination rate increased in the presence of defects, leading to higher $(np)^{1/2}$ at the source/channel interface. The increasing np results in higher channel conductance, which in turn explains the elevated I_{OFF} in the presence of defects.

The simulation results also show that in the OFF-state, the presence of defects significantly affects the tunneling behavior of the NT-HJLTFET. Acceptor-type defects introduce negatively charged ions, which increase the hole concentration at the interface, especially near the source side. This accumulation of holes leads to a narrowing of the bandgap at the source-channel junction, which lowers the V_{th} to 0.065 V. However, this also increases the I_{OFF}, reducing the



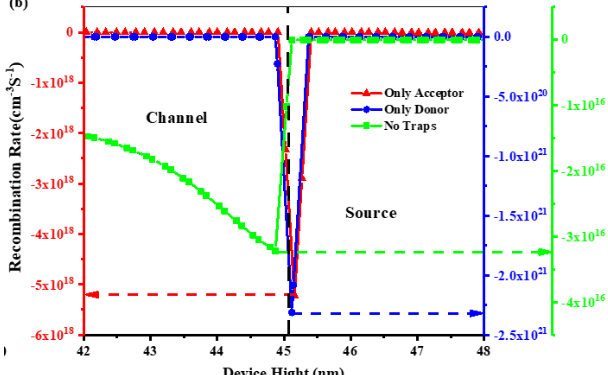


Figure 13. (a) Square of product of electron-hole density, (b) Recombination rate in the vicinity of the tunneling junction in the OFF state for NT-HJLTFT.

I_{ON}/I_{OFF} ratio to 1.03×10^2. In contrast, donor-type defects introduce positively charged ions that increase the electron concentration in the channel region, which also leads to a narrowing of the bandgap. This reduction in bandgap shifts the V_{th} to 0.08 V. Although the I_{OFF} increases due to donor defects, the I_{ON}/I_{OFF} ratio remains higher at 1.15×10^{11} compared to the acceptor defect scenario but still lower than the defect-free value of 1.01×10^1.

The simulation results indicate that the presence of acceptor defects reduces the width of the tunneling region in the ON-state, resulting in an increased electron tunneling rate. As a consequence, the maximum transconductance (g_{mmax}) rises. Similarly, donor defects also lead to a decrease in the tunneling region width during the ON-state, which further enhances the electron tunneling rate and increases g_{mmax}. Specifically, the g_{mmax} values in the presence of donor and acceptor defects were measured at 22 mS and 25 mS, respectively.

Additionally, the maximum frequency of transition (f_T) in the presence of donor and acceptor defects was recorded at 19 THz and 29 THz, respectively. However, these values were lower than those observed in the absence of defects. This reduction can be attributed to an increase in channel charge, which subsequently raises the gate capacitance (C_{gg}) when defects are present.

3.4 Sensitivity analysis

In the course of our sensitivity analysis, the impact of varying structural parameters such as N_D, L_{ch}, and T_b

Figure 14. Sensitivity analysis of NT-HJLTFET performance metrics (I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, V_{th}, SS) for varying N_D, L_{ch}, and T_b. I_{OFF} and I_{ON}/I_{OFF} show higher sensitivity to N_D, while V_{th} and SS remain stable across changes. This demonstrates the robustness of NT-HJLTFET across different structural configurations.

on the main electrical characteristics including I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, threshold voltage (V_{th}), and subthreshold slope (SS) was examined. To isolate the effect of each structural parameter, all other parameters were held constant according to the values given in Table 1. For instance, when analyzing the sensitivity of I_{ON}/I_{OFF} to N_D, parameters such as L_{ch}, T_b, WFS, and WFC were kept at their nominal values as specified in the Table 1, ensuring that observed variations in I_{ON}/I_{OFF} can be attributed solely to changes in N_D.

Furthermore, sensitivity in this context is quantitatively defined as the standard deviation of the given electrical characteristic divided by its mean. This metric provides a normalized measure of the fluctuation of a characteristic relative to changes in a specific structural parameter, offering insight into the robustness of the device performance across different design configurations.

As shown in Fig. 14, I_{OFF} and the I_{ON}/I_{OFF} ratio exhibit higher sensitivity to variations in N_D, demonstrating that changes in doping concentration significantly impact the device's off-state current and overall current ratio. In contrast, parameters like V_{th} and SS remain relatively stable when N_D is varied, suggesting that these characteristics are less influenced by changes in doping concentration. The figure also highlights the sensitivity of these electrical parameters to T_b, where narrow body introduces more significant variations on I_{ON}/I_{OFF}. This indicates that proper control of T_b is critical for maintaining device performance as scaling progresses. The relatively lower sensitivity of V_{th} and SS to L_{ch} suggests that these parameters are less affected by channel length reduction, offering more robustness during device scaling. The sensitivity analysis confirms that while some parameters show significant variability, others remain stable, making the device design versatile and scalable.

4. Conclusion

In this paper, we propose the use of cylindrical core-shell gates along with a $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ heterojunction at the tunneling junction to enhance the digital and analog performance parameters of junctionless TFETs. The simulation results demonstrate significant improvements in the NT-HJLTFET over the NW-JLTFET: a five orders of magnitude enhancement in the I_{ON}/I_{OFF} ratio, an 80% improvement in the subthreshold slope (SS), and an 84% improvement in the threshold voltage (V_{th}). Additionally, the NT-HJLTFET shows three orders of magnitude increase in transconductance (g_m) and two orders of magnitude increase in the cutoff frequency (f_T) compared to the NW-JLTFET. We thoroughly investigated the influence of key structural parameters, including work function of core (WFC) and shell gates (WFS), doping levels, body thickness, and the spacer width between p-auxiliary and control gates, on the performance of NT-HJLTFET.

Our findings indicate that increasing the work function of the core-shell gates converts the channel region from intrinsic to p-type, leading to an increase in V_{th}. Higher doping concentrations in the channel enhance conductivity but also raise I_{OFF}. Furthermore, an increase in the spacer width (W_{SiO2}) reduces I_{ON} while increasing the delay time (τ). A specific NT-HJLTFET configuration with a gate length of 20 nm and body thickness of 10 nm achieved remarkable performance metrics: $I_{ON}/I_{OFF} = 9.84\times10^{13}$, $SS = 9.4$ mV/dec, $I_{ON} = 6.4\times10^{-3}$ A/2πr, g_m = 17.5 mS, and f_T = 42.7 THz.

Therefore, NT-HJLTFET stands out as a promising candidate for digital and analog applications in integrated circuits. However, our simulations also reveal that acceptor and donor defects at the $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ heterojunction interface increase the generation-recombination rate, leading to a rise in the subthreshold slope and I_{OFF}.

Authors contributions
Authors have contributed equally in preparing and writing the manuscript.

Availability of data and materials
All data are available in the manuscript.

Conflict of interests
The authors declare no conflict of interest.

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