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High-K dual metal gate-nano tube (DMG-NT) field effect transistors (FETs): A possible solution to diminish the effect of temperature variation

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Original Research

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Abstract:

This paper provides a possible solution to minimize the effect of temperature on nano-tube (*NT*) FETs by applying performance enhancers. Here *high-k* and dual metal gates (*DMG*) are used as performance boosters. The *high-k* downgrades the leakage issues and improves the on-state current (I_{on}), while dual metal gate suppresses the *short-channel-effects (SCE)*. Simulation results reflect that I_{on} uplifts by 50.19% and I_{off} downgrades by 53.75% at 400K with the use of *DMG* and *high-k* dielectric in *NT* FETs. The paper also covers the temperature-dependent comparative *radio frequency(RF)* performance analysis of *high-k DMG NT* FETs and *NT* FETs. The temperature-dependent performance analysis has been done for temperatures ranging from 250K to 400K using *ATLAS* device simulator from *SILVACO*.

Keywords: Dual metal gate (DMG); Double gate all around (DGAA); Gate all around (GAA); High-K; Nanoscale; Nanotube; Short channel effects (SCE)

1. Introduction

Nowadays Multi-gate structures are the prominent solution for nano-scale CMOS fabrication technology. Such 3-dimensional structures are more immune to *SCE* compared to planner structures. FinFETs, gate all around (GAA) FETs and Nano sheet FETs are the most preferred 3-D structures. In 2021, "*International Roadmap for Devices and Systems(IRDS)*" claimed that wire-shaped *GAA* FETs are the most appropriate structure to reduce *SCE* in the sub-7-nm technology [1–4]. Leading foundries are moving towards 3nm technology by the end of this year with GAA/Nano-wire structure [5].
Nanotube (*NT*) structure shows their utility in various domains [6]. In the field of semiconductors, *NT*-FETs enhance the drive current, trans-conductance, and controllability. The double gate-all-around (DGAA)/Nanotube (*NT*) FETs have been proposed by H.M. Fahad [7]. The core-shell structure of *NT* provides two-fold controllability over the channel as well as drive current [9–11]. Optimizing nanotube diameter can lead to improved NT-FET performance [12]. Nitish and colleagues confirmed that the inner or core gate exhibits better controllability than the outer or shell gate, as noted in reference [13].
To further improve the immunity towards *SCE*, various performance enhancers are integrated into the device. High-K dielectric material minimizes gate leakage in Nano-scale devices and boosts the on-state current (I_{on}) while reducing the inverter delay, as detailed in references [14, 15]. Another important and usable performance booster is the dual metal gate (*DMG*) incorporated over the dielectric layer. Long *et al.* proposed this technique to improve the *SCE* in a device [16]. In this technique, the gate terminal is made of two materials with different work functions, Mϕ1 and Mϕ2. These gates are termed control and screen gates, respectively [17]. The control gate work function (Mϕ1) is higher than the work function of the screen gate (Mϕ2) for an n-channel MOSFET, and the converse is valid for a p-channel MOSFET [18]. B. Kwak utilized the concept of dual metal with ferroelectric material to improve the performance of

the memory unit [19]. T. Lei *et al.* also use the dual metal gate technique in thin film transistors and compare its performance with normal devices [20]. A device with a *DMG* structure is superior to a traditional one as it shows excellent immunity towards*SCE*, diminishes hot-carrier injection (*HCI*), and lowers the *DIBL*. *DMG* devices work on gate work function engineering and the gate work function has significant effects on various parameters. The higher work function value leads to a higher threshold voltage, improves on-current (I_{on}), and reduces the off-current (I_{off}) [21].
Researcher V. Kumari *et al.* [22] verified that temperature variation deteriorates the device performance due to changes in mobility (μ). The value of μ reduces with rising temperature due to the growing rate of phonon scattering in which μ varies with temperature as $T^{-3/2}$ [23]. The value of μ also reduces with falling temperature caused by impurity scattering [24]. Himanshi *et al.* also verified that high temperatures degrade the device performance [25]. Purwar *et al.* say that high temperature degrades the on-current (I_{on}) and trans-conductance (g_m) value of the device [15].
In the light of above literature review it can be concluded that device performance degrades with the rise in temperature and a suitable device structure is required to fight against temperature variation. In this paper, a temperature-based study has been done on *High-K dual metal gate (DMG)-nanotube (NT) FETs* and *NT*FETs. This study has been done for temperatures ranging from 250*K* to 400*K*. This study explores adverse effects generated by temperature variation on both devices and tries to explore the temperature immune device. A few analog/RF parameters are also compared on the temperature scale. To ensure the accuracy of the findings, a TCAD simulation tool has been employed.

2. Materials and methods

Fig. 1 shows the 3D view of the *high-K DMG-NTFET* extracted from *TCAD* simulator. Fig. 2a and Fig. 2b display the horizontal cut-plane view of *high-k DMG-NT*FET and

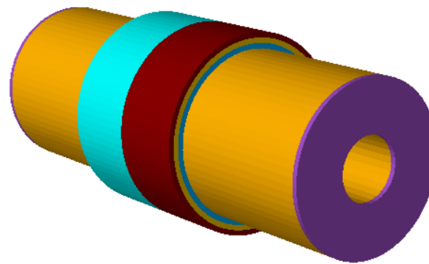

Figure 1. *3D View* of *high-k DMG NT FET*.

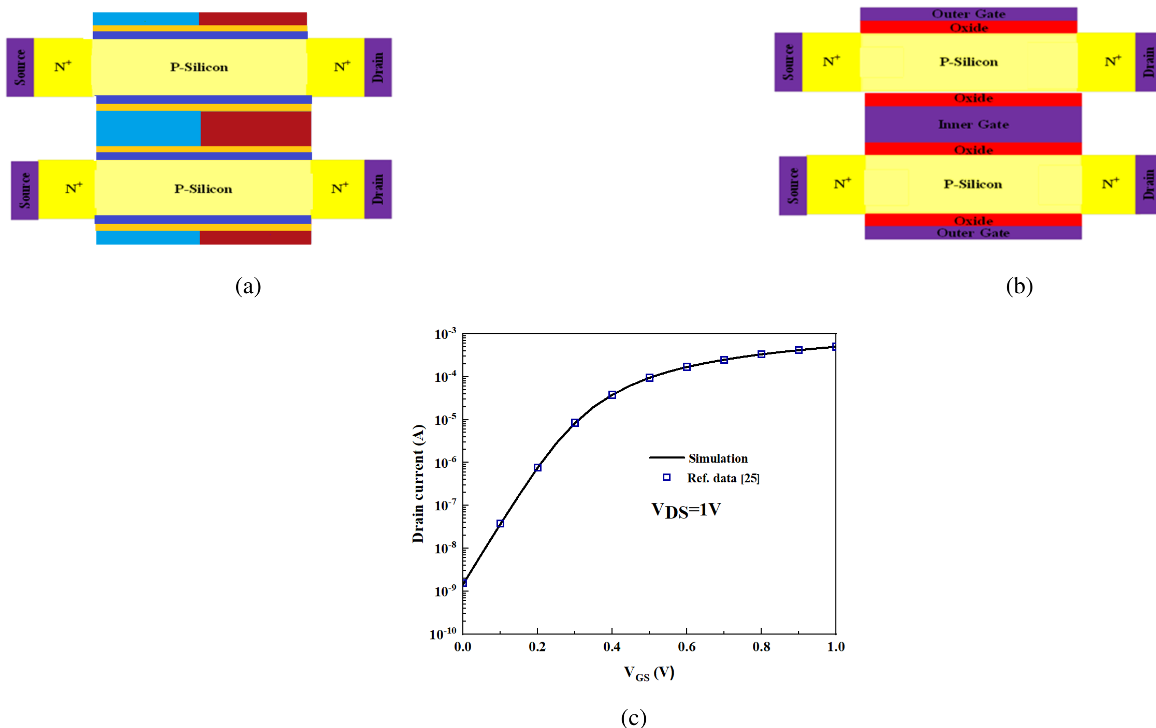

Figure 2. a) Horizontal cut plane view of *high-k DMG NT FET*. b) Horizontal cut plane view of *NT FET*. c) Comparison of Drain current (I_D) of TCAD simulation with experimental data Ref. [8] for *NT-FET*.

Table 1. Dimensions of *NT FET* and *high-k DMG NT FET* used for simulation.

S. N.		Device simulation/Calibration parameters	
	Parameter	*NT-FET*	*High-k DMG NT FET*
i	Channel length(L)	30 nm	
ii	Source/Drain Doping (Ns,Nd)	10^{20} cm^{-3}	
iii	Channel Doping (NA)	10^{15} cm^{-3}	
iv	Thickness of the oxide (tox)	2 nm	1 nm
v	High K Thickness (HfO_2)	—	1 nm
vi	Thickness of the channel (tsi)	10 nm	
vii	Core gate radius	4 nm	
viii	Work-function of the metal-1 (ϕm1)	4.82 eV	4.9 eV
ix	Work-function of the metal-2(ϕm2)	—	4.61 eV

*NT*FET. Fig. 2c covers the calibration of simulated data parameters with experimental parameters from reference [8]. The graph shows a good agreement between them. In *High-K DMG-NT*FET, two 1nm thick layers of SiO_2 and HfO_2 are grown over the channel. For DMG, metallization has been done in a ratio of 1:1 side-by-side. Table 1 covers the simulation parameters. In both devices, the source/drain terminal is of aluminium material. The gate terminal in *NT*FET is of molybdenum disilicide while in the *DMG-NT* FET device the gate material-1 is of molybdenum and gate material-2 is of niobium. For simulation, Drift-diffusion (*DD*), High-field saturation (*HFS*), concentration, and field-dependent (*CFD*) models/methods have been utilized. The drift-diffusion (*DD*) transport model utilizes the current continuity equations of electrons and holes. The high-field saturation (*ccsmob*), concentration, and field-dependent (*conmob,fldmob*) mobility models are used for mobility calculation. Lombardi model(*cvt*) is also utilized for mobility calculation. Quantum confinement effects (*QCE*) are irrelevant for a device having a tube width greater than 5 nm and length above 10 nm as mentioned in reference [26]. This effect is irrelevant to the device parameters considered in the paper.

3. Results and discussion

Fig. 3 displays the variation of drain current (I_D) against drain voltage(V_{DS}) for *NT* FET and *high-k DMG NT* FET for V_{GS}=1Volt and channel length(L) 30nm. Employing a high-k dielectric material increases the oxide capacitance, which in turn proportionally boosts the drain current [13]. Specifically, at a temperature of 300 K, a high-k dual metal gate (*DMG*) nanotube (*NT*) field-effect transistor (FET) exhibits a 49.9% increase in I_D relative to a standard *NT* FET. Fig. 4 shows the transfer characteristic of *NT* FET and *high-k DMG NT* FET at V_{DS} =1Volts. High k dielectric reduces the gate leakage current and reduces the off-state leakage current (I_{off}) as high-K offers more resistance in the path of minority carriers and reduces the leakage or off-state current (I_{off}). At room temperature reduction in I_{off} is about

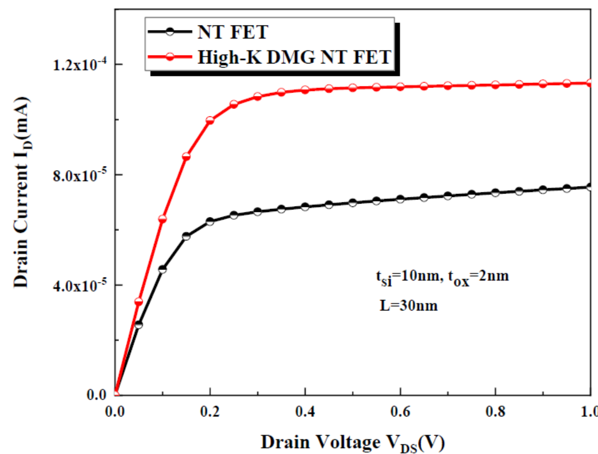

Figure 3. Drain current (I_D) against drain voltage (V_{DS}).

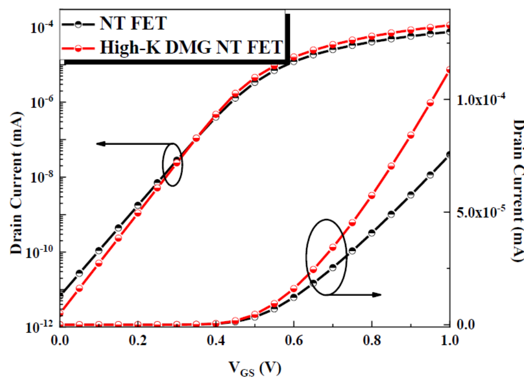

Figure 4. Transfer characteristic of *NT FET* and *high-k DMG NT FET*.

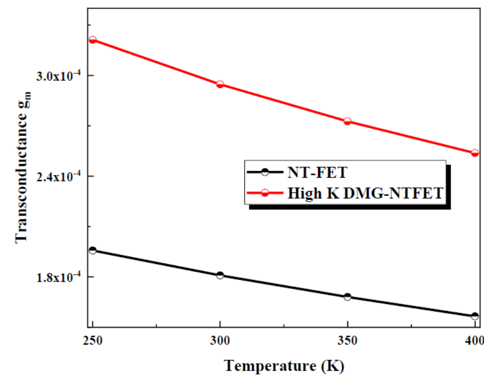

Figure 7. g_m variation against temperature.

65% in *high-K DMG NT* FET as compared to *NT* FET. The high value of on current (I_{on}) for *high-k DMG NT* FET can be clearly seen at V_{GS}=1Volt.This is due to higher oxide capacitance in high-k device.

Fig. 5 displays the variation of sub-threshold swing (*SS*) and DIBL against temperature variations ranging from 250 K to 400 K.these two are crucial parameters to judge the *SCE* in a device. The lower value of *SS* and DIBL provide more immunity towards *SCE*. The *SS* can be calculated as a change in V_{GS}, that will cause a one-decade variation in I_d in the subthreshold region [15], or it can be calculated by the formula given in ref [12]. For all temperatures ranging from 250K to 400K, *high-k DMG NT* FET has lower *SS* and DIBL values than *NT* FET.

Fig. 6 shows the variation of I_{on} and I_{off} against temperature for both the devices. On increasing the temperature, I_{off} increases due to the generation of more minority carriers and I_{on} decreases due to an increase in phonon scattering

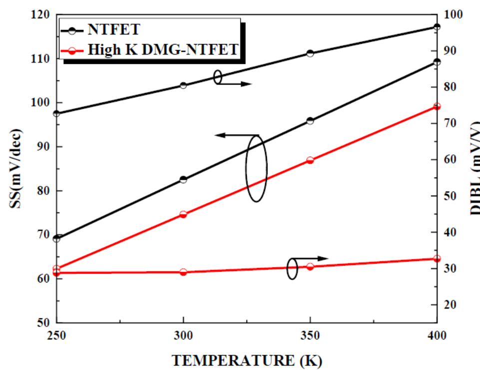

Figure 5. Sub-threshold swing (*SS*) and *DIBL* against temperature.

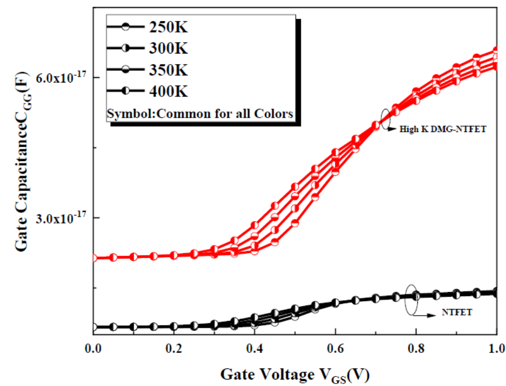

Figure 8. C_{GG} variation against V_{GS}.

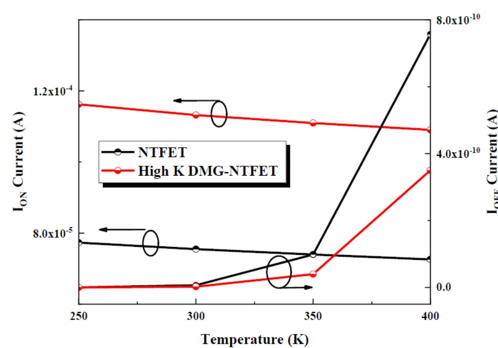

Figure 6. Change of I_{on} and I_{off} against temperature.

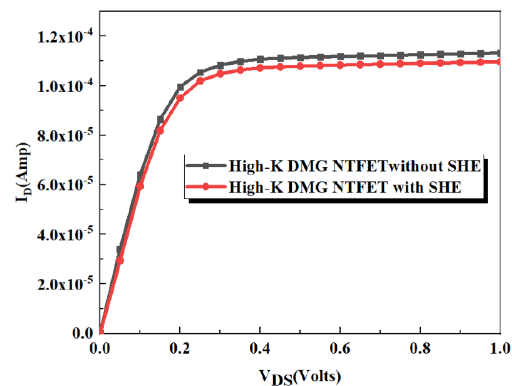

Figure 9. I_D variation against V_{GS} with considering self-heating and without considering self-heating effects (*SHE*).

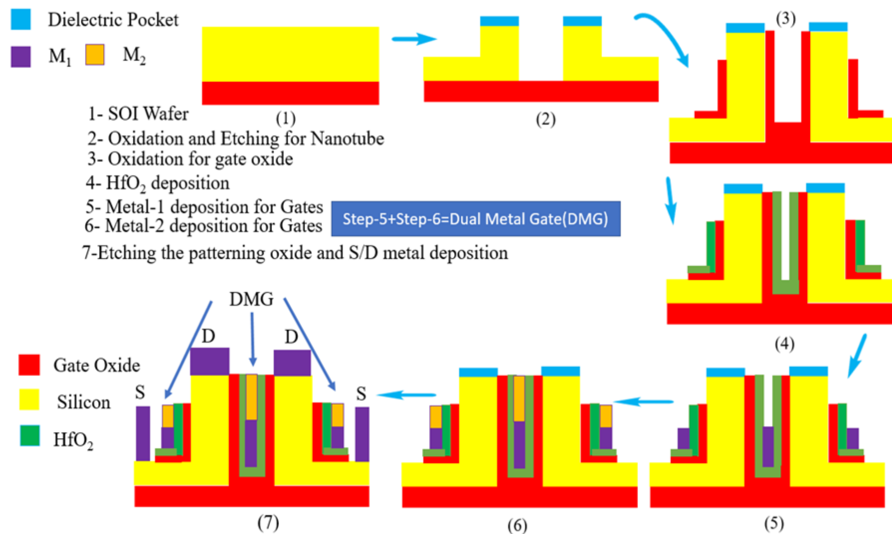

Figure 10. Fabrication step for High-k DMG NT-FET.

for both devices. However *High-K DMG NT* FET shows a higher value of I_{on} and a lower value of I_{off} for entire temperature range.

Fig. 7 shows the variation of g_m against the temperature for VDS=1volt. g_m represents the ratio of I_D to the V_{GS}. The higher value of g_m signifies the superior control of the gate over the channel. This graph shows that *high-k DMG NT* FET has superior control over the gate for all the temperatures compared with *NT* FET.

Fig. 8 reflects the variation of gate capacitance (C_{GG}) against V_{GS} for VDS=1 for the entire temperature range. The presence of *high k* enhances the gate capacitance of *high-k DMG NT* FET. On increasing the temperature value of C_{GG} decreases after the threshold for both the devices due to interface charges present in between the channel and dielectric layer. Graph clearly reflects that for all the temperatures *high-k DMG NT* FET shows the higher value of C_{GG} as compared to *NT* FET.

Fig. 9 depicts the variation of I_D against V_{DS} for V_{GS}=0.75 volts with and without considering self-heating effects (*SHE*).*SHE* causes the degradation in carrier mobility due to increase in carrier to carrier collisions. This collision occurs in the channel near the drain side, and causes the reduction in drain saturation current. According to the results of Fig. 9, the drain saturation current degrades by approx. 6% due to *SHE*.

Fig. 10 reflects all the steps involve in the fabrication of *high K DMG NT* FETs [14] [16].

4. Conclusion

This paper covers the effect of temperature on *high-k DMG NT* FETs and *NT* FETs devices for different device parameters. For temperatures ranging from 250 K to 400 K, it has been observed that *high-k DMG NT* FETs reflect a higher value of I_{on}, g_m, C_{GG} and lower value of I_{off}, *SS*, *DIBL*. Comparative results depict that *high-k DMG NT* FETs have higher immunity towards *SCE* as compared to *NT* FETs. It can also be predicted from the results that *high-k DMG NT* FETs are more immune to temperature and may be a possible solution to mitigate the effect of temperature as compared to *NT* FETs.

Authors Contributions
Not applicable.

Availability of Data and Materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of Interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] IEEE international roadmap for devices and systems. *IEEE publication*, 2024. DOI: https://doi.org/10.60627/8f13-at55.

[2] G. Pei, J. Kedzierski, P. Oldiges, M. Ieong, and E. C. C. Kan. Finfet design considerations based on 3-d simulation and analytical modeling. *IEEE Transactions on Electron Devices*, 49:1411–1419, 2002. DOI: https://doi.org/10.1109/TED.2002.801263.

[3] Y. Zhang, Z. Li, C. Wang, and F. Liang. Compact analytical threshold voltage model of strained gate-all-around mosfet fabricated on si1-xgex virtual substrate. *IEICE Trans. on Electron.*, 99:302–307, 2016. DOI: https://doi.org/10.1587/transele.E99.C.302.

[4] J. Y. Song, W. Y. Choi, J. H. Park, J. D. Lee, and B. G. Park. Design optimization of gate-all-around (gaa) mosfets. *IEEE Transactions on Nanotechnology*, 5:186–191, 2006. DOI: https://doi.org/10.1109/TNANO.2006.869952.

[5] N. Cohen. Samsung at foundry event talks about 3nm. *Mbc fet developments*, 2024.

[6] B. Sadeghi and R. A. R. Vahdati. Comparison and semcharacterization of novel solvents of dna/carbon nanotube. *Applied Surface Science*, 258:3086–3088, 2012. DOI: https://doi.org/10.1016/j.apsusc.2011.11.042.

[7] H. M. Fahad, C. E. Smith, J. P. Rojas, and M. M. Hussain. Silicon nanotube field effect transistor with core-shell gate stacks for enhanced high-performance operation and area scaling benefits. *Nano Lett.*, 11:4393–4399, 2011. DOI: https://doi.org/10.1021/nl202563s.

[8] D. Tekleab. Device performance of silicon nanotube field effect transistor. *IEEE Electron Device Lett.*, **35**:506–508, 2014. DOI: https://doi.org/10.1109/LED.2014.2310175.

[9] H. M. Fahad and M. M. Hussain. Are nanotube architectures more advantageous than nanowire architectures for field effect transistors. *Sci Rep*, 2:475, 2012. DOI: https://doi.org/10.1038/srep00475.

[10] D. Tekleab. Device performance of silicon nanotube field effect transistor. *IEEE Electron Device Lett*, 35:506–508, 2014. DOI: https://doi.org/10.1109/LED.2014.2310175.

[11] A. Kumar, S. Bhushan, and P. K. Tiwari. A threshold voltage model of silicon-nanotube-based ultrathin double gate-all-around (dgaa) mosfets incorporating quantum confinement effects. *IEEE Trans. Nanotechnol.*, 16:868–874, 2017. DOI: https://doi.org/10.1109/TNANO.2017.2717841.

[12] P. Rajendiran and N. A. Justeena. Structural process variation on silicon nanotube tunnel field-effect transistor. *Silicon*, 15:7149–7156, 2023. DOI: https://doi.org/10.1007/s12633-023-02575-4.

[13] N. Kumar, V. Purwar, H. Awasthi, R. Gupta, K. Singh, and S. Dubey. Modeling the threshold voltage of core-and-outer gates of ultra-thin nanotube junctionless-double gate-all-around (njl-dgaa) mosfets. *Microelectronics Journal*, 113:105104, 2021. DOI: https://doi.org/10.1016/j.mejo.2021.105104.

[14] V. Purwar, R. Gupta, H. Awasthi, and S. Dubey. Impact of different gate dielectric materials on analog/rf performance of dielectric-pocket double gate-all-around (dp-dgaa) mosfets. *Silicon*, **14**:9361–9366, 2022. DOI: https://doi.org/10.1007/s12633-021-01624-0.

[15] V. Purwar, R. Gupta, N. Kumar, H. Awasthi, V. K. Dixit, K. Singh, S. Dubey, and P. K. Tiwari. Investigating linearity and effect of temperature variation on analog/rf performance of dielectric pocket high-k double gate-all-around (dp-dgaa) mosfets. *Appl. Phys. A.*, **126**:746, 2020. DOI: https://doi.org/10.1007/s00339-020-03929-0.

[16] W. Long, H. Ou, J. M. Kuo, and K. K. Chin. Dual material gate (dmg) field effect transistor. *IEEE Trans. Electron Devices*, **46**:865–870, 1999. DOI: https://doi.org/10.1109/16.760391.

[17] M. J. Kumar and A. Chaudhry. Two-dimensional analytical modeling of fully depleted dual-material gate (dmg) soi mosfet and evidence for diminished short-channel effects. *IEEE Trans. Electron Devices*, **51**:69–574, 2004. DOI: https://doi.org/10.1109/TED.2004.823803.

[18] L. Jin, L. Hongxia, L. Bin, C. Lei, and Y. Bo. Two-dimensional threshold voltage analytical model of dmg strained-silicon-on-insulator mosfets. *Journal of Semiconductors*, **31**:084008, 2010. DOI: https://doi.org/10.1088/1674-4926/31/8/084008.

[19] B. Kwak, K. Lee, N. H. Park, S. J. Jeon, H. Kim, and D. Kwon. Recessed channel ferroelectric-gate field-effect transistor memory with ferroelectric layer between dual metal gates. *IEEE Transactions on Electron Devices*, **69**:1054–1057, 2022. DOI: https://doi.org/10.1109/TED.2022.3144621.

[20] T. Lei, R. Shi, Y. Wang, Z. Xia, and M. Wong. A comparative study on inverters built with dual-gate thin-film transistors based on depletion or enhancement-mode technologies. *IEEE Transactions on Electron Devices*, **69**:3186–3191, 2022. DOI: https://doi.org/10.1109/TED.2022.3167940.

[21] S. Kumar, A. K. Chatterjee, and R. Pandey. Performance analysis of gate electrode work function variations in double-gate junctionless fet. *Silicon*, **13**:3447–3459, 2021. DOI: https://doi.org/10.1007/s12633-020-00774-x.

[22] V. Kumari, M. Gupta, M. Saxena, and R. S. Gupta. Temperature dependent model for dielectric pocket double gate (dpdg) mosfet: a novel device architecture. *IEEE International Conference on Emerging Electronics.*, , 2012. DOI: https://doi.org/10.1109/ICEmElec.2012.6636264.

[23] S. M. Sze. Book: Physics of semiconductor devices. *3ed ed. Wiley New York.*, , 2021.

[24] P. Banerjee and J. Das. Gate work function-engineered graded-channel macaroni mosfet: exploration of temperature and localized trapped charge-induced effects with gidl analysis. *J. Electron. Mater.*, **51**:1512–1523, 2022. DOI: https://doi.org/10.1007/s11664-021-09419-0.

[25] H. Awasthi, N. Kumar, V. Purwar, and S. Dubey. Impact of temperature on analog/rf performance of dielectric pocket gate-all-around (dpgaa) mosfets. *Silicon*, **13**:2071–2075, 2021. DOI: https://doi.org/10.1007/s12633-020-00610-2.

[26] D. Querlioz, J. S. Martin, K. Huet, et al. On the ability of the particle monte carlo technique to include quantum effects in nano-mosfet simulation. *IEEE Transactions on Electron Devices*, **54**:2232–2242, 2007. DOI: https://doi.org/10.1109/TED.2007.90271.