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A low leakage and high-speed phase frequency detector-charge pump designed in nano dimension based CMOS technology

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Original Research

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Abstract:

This research paper undertakes an innovative investigation into the conceptualization and execution of charge pump circuits that are specifically engineered in nano-dimension MOS transistor. In contrast to traditional Dickson-charge-pump models, the suggested configuration incorporates MOS transistors and anti-phase pumping clocks, which substantially increase output voltages and voltage pumping advantages. The PLL system's PFD, Charge Pump circuit, and PFD are dynamic components, as demonstrated by a thorough analysis of these elements on RF-simulation tool. The accuracy of the proposed methodologies through rigorous simulations, establishing them as innovative approaches for low-voltage circuitry. In addition to contributing to the advancement of knowledge regarding charge pump designs, the research offers significant insights into the synergistic functioning of these circuits within a PLL system. The simulation outcomes validate the efficacy of the novel charge pump configuration, presenting low spur attenuation, high phase margin and high loop gain for implementation in low-power electronic systems. With a particular focus on optimizing design parameters, investigating sophisticated materials and fabrication technologies, and striving for innovative applications in domains like communication devices. This study establishes a foundation for revolutionary advancements in the design of low-leakage circuits and provides opportunities for novel approaches to the evolving field of electronic technologies.

Keywords: Charge pump; Complementary metal oxide semiconductor; Current mismatch; Nano dimension; Phase frequency detector; Phase lock loop

1. Introduction

Accurate and effective signal synchronization is essential in the dynamic field of integrated circuit design. The Phase Frequency Detector-Charge Pump (PFD-CP) circuit is an essential element in this field and forms the basis for many contemporary electronics applications [1, 2]. This research study explores the Phase Frequency Detector-Charge Pump system in the framework of Complementary Metal-Oxide-Semiconductor (CMOS) technology [3, 4], providing a thorough analysis and design considerations. In order to fully appreciate the importance of this system, it is necessary to break down the vocabulary and clarify the various uses it has in modern electronics.

1.1 Latest trends, challenges, and design methodologies

Recent years have seen significant developments in the Phase Frequency Detector-Charge Pump (PFD-CP) design landscape of CMOS technology. These advancements have been propelled by the constant demand for greater performance, reduced power consumption, and smaller form factors. An exhaustive review of the literature reveals the following prevalent trends in the field:

A. PFD-CP Circuit Design in Sub-Micron CMOS Technology: As a result of the ongoing reduction in the size of CMOS technology nodes [5], PFD-CP circuits are presently being developed in dimensions below 45 nm and 28 nm. This emerging phenomenon presents difficulties pertaining to leakage currents, gate capacitances, and parasitic interconnects, which demand novel approaches to design in order to alleviate these concerns [6].
B. Low Power Design: In contemporary electronic devices, low power is a major necessity. To reduce power consumption in PFD-CP circuits, scientists are investigating novel methods including adaptive biasing and sub-threshold operation [7, 8]. These methodologies entail the utilization of intricate equations to represent the correlation among operating frequency, threshold voltage, and power consumption.
C. High-Speed Operation: In order to meet the requirements of high-speed communication systems, PFD-CP designs must be able to function at frequencies in the multi-gigahertz range. The task of attaining high frequencies while ensuring phase accuracy and immunity to noise presents considerable obstacles [9, 10]. Scholars are utilizing sophisticated mathematical modelling and simulations in order to optimize the parameters of the circuit for optimal performance at high frequencies.
D. Digital Calibration: In an effort to mitigate the impacts of manufacturing variations and aging, researchers are investigating digital calibration and self-healing techniques. These techniques employ complex equations and algorithms to dynamically modify circuit parameters [11, 12], thereby guaranteeing optimal performance throughout the lifespan of the device.
E. Mixed-signal Integration: It is increasingly typical to find PFD-CP circuits integrated with both analog and digital components on a single device. With the intention of improving functionality at the system level and minimizing reliance on external components, this integration generates intricate equations that delineate the interrelationships among various circuit blocks and their influence on the overall performance [13–15].

1.2 Evaluating problems and finalizing design constraints

The design of PFD-CP circuits in CMOS technology involves a meticulous evaluation of various challenges and constraints. Equations governing the critical aspects of the design can be derived and analyzed to establish these constraints:
A. Voltage and Current Constraints: Equations referring to the supply voltage (VDD) and current (IDD) are extremely important in the process of computing the power budget for the PFD-CP circuit. The equations in question take into account a variety of characteristics, such as operating frequency, load capacitance, and leakage current, among other things. They provide vital insights on the power distribution and consumption of the circuit as a result of their actions [12–14]. The Equation (1) shows the power budget for the PFD-CP

$$P = V_{DD} \times DD \quad (1)$$

where P = Power budget of the PFD-CP
V_{DD} = Supply voltage
I_{DD} = Current
B. Phase Detection Range: The phase detection range is an important parameter that determines the greatest possible phase difference that the PFD can accommodate. Equation (2) that describe the phase detection range in terms of the frequencies of the input signals and the parameters of the charge pump are helpful in optimizing the PFD for a variety of applications [15–17].

$$\text{Phase Detection Range} = \frac{2\pi \times \text{Frequency Offset}}{\text{PFD Frequency}} \quad (2)$$

C. Charge Pump Output Current: The pace at which frequency correction is performed is significantly impacted by the output current of the charge-pump [18]. Equations that determine the charge pump output current give insight into the transient behavior of the circuit by considering charge pump transconductance and input voltage differentials. The Phase Frequency Detector-Charge Pump (PFD-CP) prototype circuit in the RF domain is what this research aims to create and model with the help of the SPICE simulation program [19]. The objective is to enhance the circuit design while maintaining within the parameters that have been specified in order to decrease the amount of power that is wasted and leakage. In order to simulate the updated design, we will be making use of the Advanced Design System (ADS), which comes equipped with RF-SPICE capabilities. A comprehensive study of the performance of the PFD-CP circuit that has been optimized will be carried out [20].

2. Literature review

A. Charge Pumps in Low-Voltage Applications: The design and optimization of charge pumps in low-voltage applications have been subjects of extensive research due to their critical role in numerous electronic systems. Conventional charge pump models, such as the “Dickson-charge- pump”, have provided a foundation for voltage boosting in low-power scenarios [21]. However, the quest for enhanced voltage pumping gains and increased output voltages has led to the exploration of novel configurations [22]. Prior studies have investigated the use of anti-phase pumping clocks, as introduced by [23], showcasing improved performance in voltage pumping. Additionally, the integration of metal-oxide-semiconductor (MOS) transistors as substitutes for diodes has been proposed [24, 25], offering greater flexibility and efficiency in low-voltage environments. The present research builds upon these innovations, pushing the boundaries of charge pump design to achieve superior results in low-voltage applications.
B. Low-Voltage Circuitry and Emerging Applications: As electronic systems continue to evolve, the demand for low-voltage circuitry has become more pronounced, particularly in emerging applications such as Internet of Things (IoT) devices and biomedical implants. Studies have emphasized the importance of designing circuits that operate efficiently at low power levels, extending the battery life of portable devices and minimizing energy consumption [17]. The exploration of charge pump configurations and PFDs for such applications becomes imperative.

3. Design methodlogy & implementation

In this study, innovative charge pumps specifically designed for low-voltage applications are introduced. These charge pumps offer enhanced voltage pumping gains and increased output voltages in comparison to the existing "Dickson-charge-pump" model [25, 26]. The research focuses on refining the conventional "Dickson-charge-pump" design to achieve superior performance in low-voltage scenarios.

3.1 Schematic representation of the novel Dickson-charge-pump

The novel Dickson-charge-pump configuration is illustrated in Figure 1a & 1b. This design incorporates two pumping clocks, denoted as 1 and 2, operating in anti-phase with voltage amplitude of V.

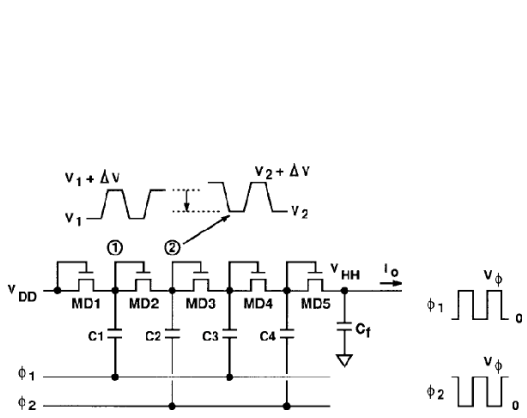
Mathematical representation of voltage variation

Ignoring boundary constraints, the voltage variation at each pumping node V can be mathematically expressed in a similar manner as presented in Equation (3). This equation encapsulates the fundamental principles governing the voltage variation across the nodes and serves as a foundational element for the subsequent analysis and optimizations conducted in this research.

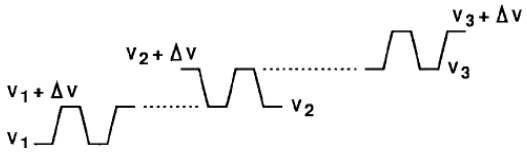
$$\Delta V = V_2 - V_1 = V_{CLK}\,x\,C/(C+Cs) - Io/f\,x\,(C+Cs) \quad (3)$$

where, ΔV = Voltage variation
V_1, V_2 = Output voltages of the charge pump
C = Capacitance
Cs = Parasitic capacitance
Io = Output current
f = Clock frequency

Several crucial variables significantly impact the performance of the charge pump. The first variable, parasitic capacitance (Cs), associated with each pumping node, plays a pivotal role. Parasitic capacitance influences the charge and discharge rates of the nodes, directly affecting the efficiency and speed of the charge pump [27]. Additionally, the frequency (f) of the pumping clocks, representing the speed at which the clocks operate, is a critical parameter. Higher frequencies enhance the rapidity of charge transfers, contributing to the overall efficiency of the charge pump [28]. Lastly, the output current loading (1o) signifies the external load that the charge-pump needs to drive, determining its ability to sustain voltage levels under different loads. A typical PFD arrangement is shown in Figures 1c. Two D-type flip-flops (DFF) plus a delayed RESET plus-gate are used in this architecture [29]. The phase and frequency properties of the input signals designated as SET determine the output of the PFD [1]. A digital circuit is used to detect changes in phase or frequency between a reference signal (Fref) and a feedback signal (Fdiv). The PFD produces two separate output signals, referred to as UP and DOWN, by comparing



(1a)



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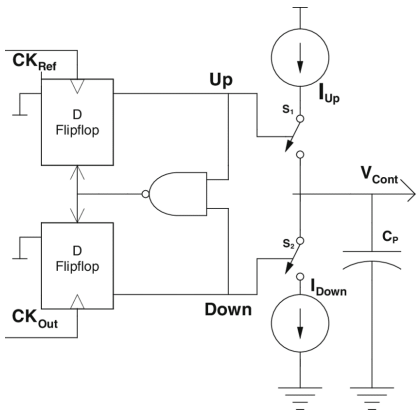

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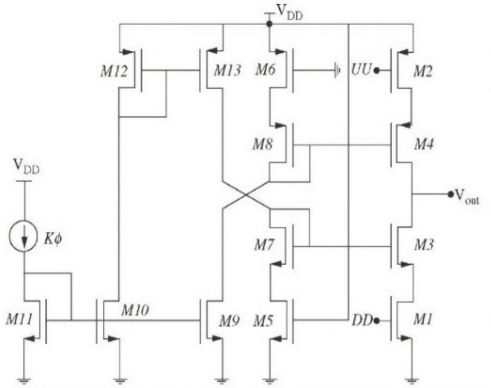


(1d)

Figure 1. a) Dickson-charge-pump [1], b) Voltage Variation [1]. c) Phase frequency detector-charge pump system architecture, d) Proposed Charge Pump Design.

these signals [25]. In particular, the UP-Signal pulses when the reference signal is in phase with the feedback signal earlier. On the other hand, the DOWN signal reaches a high value if the feedback signal takes the lead. Both the UP and DOWN signals stay at zero when there is no noticeable phase difference. These output signals are then sent to the next step, which is known as the Charge Pump (CP) [29]. The charge pump's circuit is shown in Figure 1d. The VCO takes the output signals from the PFD, processes them into currents via a loop filter (LF), and then transmits them to this circuit. The frequency at which the VCO emits light is controlled by the output voltage that results [30]. Three different states are possible for the charge pump to operate in: zero current, charging, and discharging. Essentially, it consists of two switches and two current sources [27].

The charge pump experiences a zero current condition, or equilibrium between charging and discharging, when the PFD generates pulse width signals together with UP and DOWN signals [28]. When the reference frequency is higher than the feedback output frequency on the PFD, the DOWN signal is engaged and the UP signal is deactivated [30–32]. As a result of switch S1 opening and switch S2 closing, current (I_{CP}) can pass through the filter, lowering Vout. When the reference frequency and the division output frequency coincide, a PLL. At this moment, the PFD deactivates, but the two switches on the charge pump remain open until the detector's output frequency changes. When the switches are open, no current path is created, therefore while the filter is locked, no current flows into or out of it. The circuit was constructed and simulated using the design technique. The outcomes of the simulation exercise are described in the next section [17–20].

3.2 PFD-CP design

The Phase-Frequency Detector (PFD) Charge Pump circuit's operation is based on a sophisticated architecture depicted in the circuit diagram Figure 2. The PFD part is painstakingly crafted with a pair of D-flip flops, AND gates, and NOT gates. The D-flip flops are used strategically for sequential signal processing, while the while and NOT gates help with logical functions. The resulting outputs, designated as UP and DOWN signals, have a significant influence on the system's subsequent activities. Simultaneously, the Charge Pump module, a vital subsystem inside the circuit, contains a collection of NMOS transistors and PMOS transistors, each precisely labelled for distinct responsibilities in the pumping function. The transistors, which are serially numbered for accuracy, delicately handle current flow within the pump, managing the dynamic responsiveness required for fine-grained phase and frequency adjustments. The circuit also includes switches S1 and S2, which are strategically placed to oversee the Charge Pump's coordinated sourcing and sinking of current.

4. Results

4.1 PFD simulation outcomes

The rigorous simulation of the Phase-Frequency Detector (PFD) tested the circuit's response in Figure 3a and Figure 3b to a 2.4 GHz input frequency under various control signal configurations. The PFD responded clearly to the control signal ($S_1 = 0$), demonstrating the complicated dynamics of phase and frequency detection. The simulated output vividly depicted the subtle behavior when the reference signal (Fref) leads, precisely outlining the UP-pulse production. Following that, the simulation investigated the PFD's performance when the reference signal lagged under the effect of the control signal ($S_2 = 1$). The simulation results provided a full perspective of the DOWN pulse generation, as well as detailed insights into the circuit's capacity to effectively distinguish phase and frequency discrepancies. The simulation not only validated the expected reaction under different control signals, but also allowed for a thorough

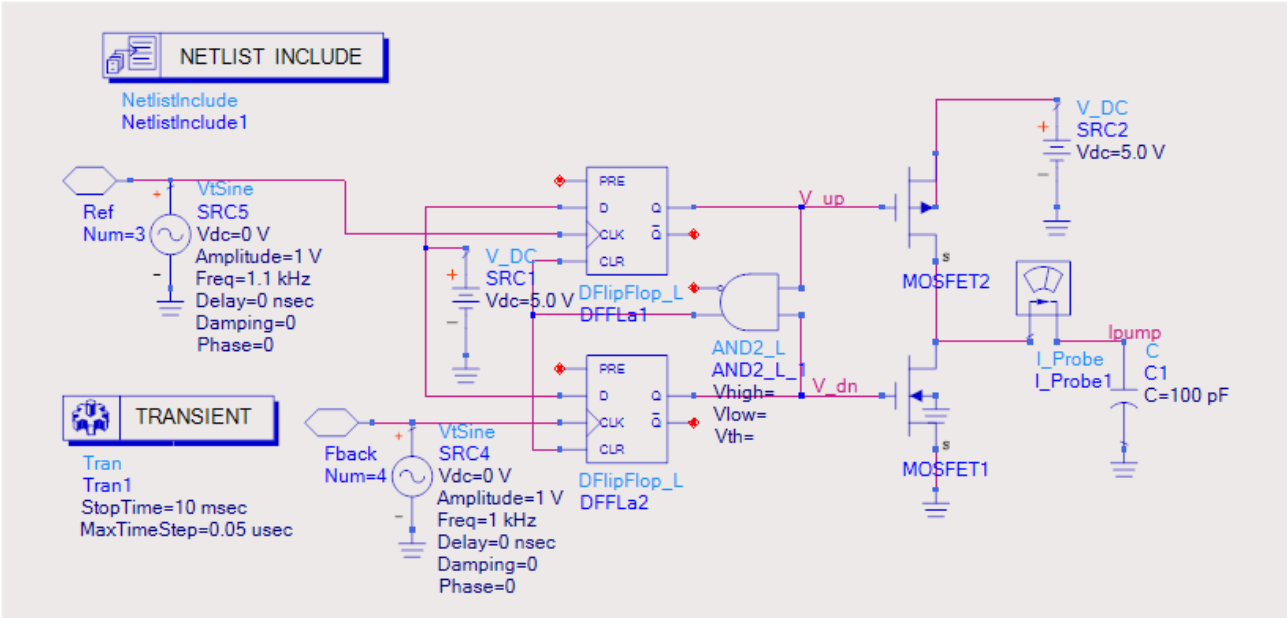


Figure 2. Phase Frequency Detector- Charge Pump Circuit Design.

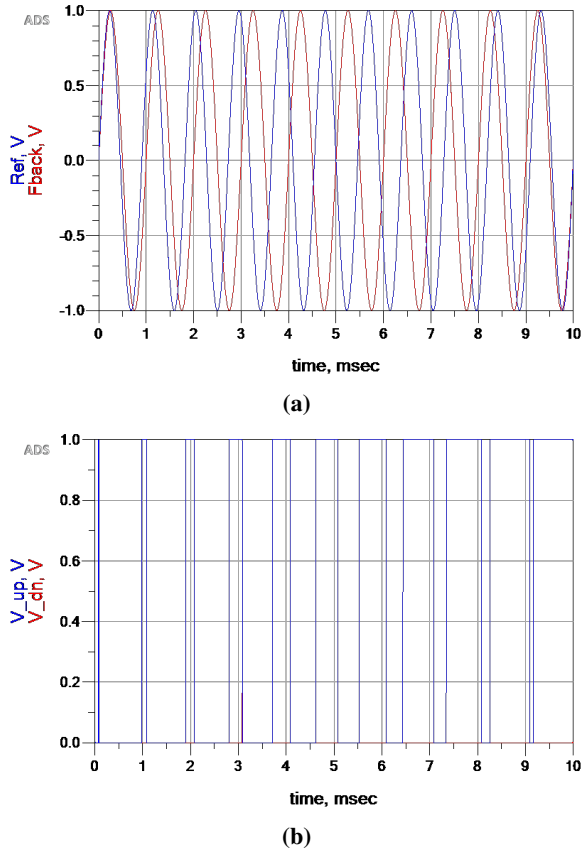


Figure 3. a) PFD When F_{ref} is leading, b) PFD When F_{ref} is lagging.

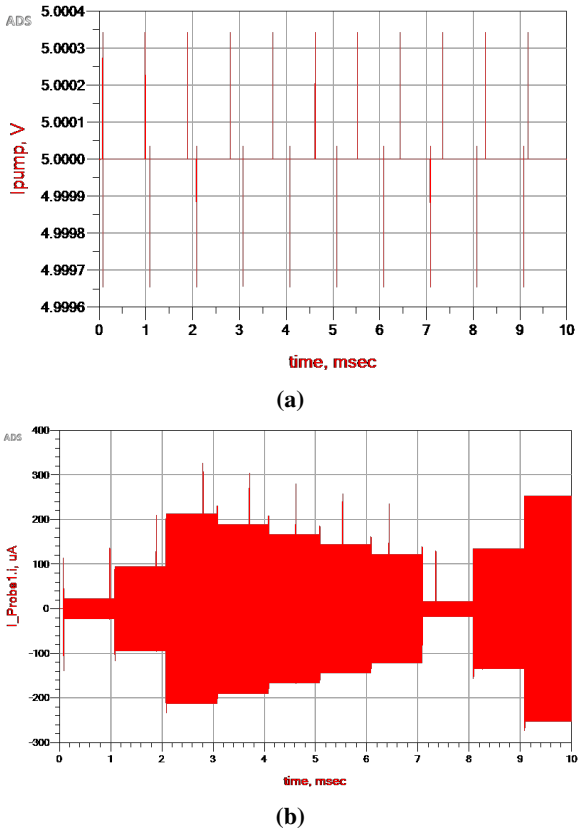


Figure 4. a) Voltage pulses of the PFD-CP output, b) Charging and sinking current at the CP output.

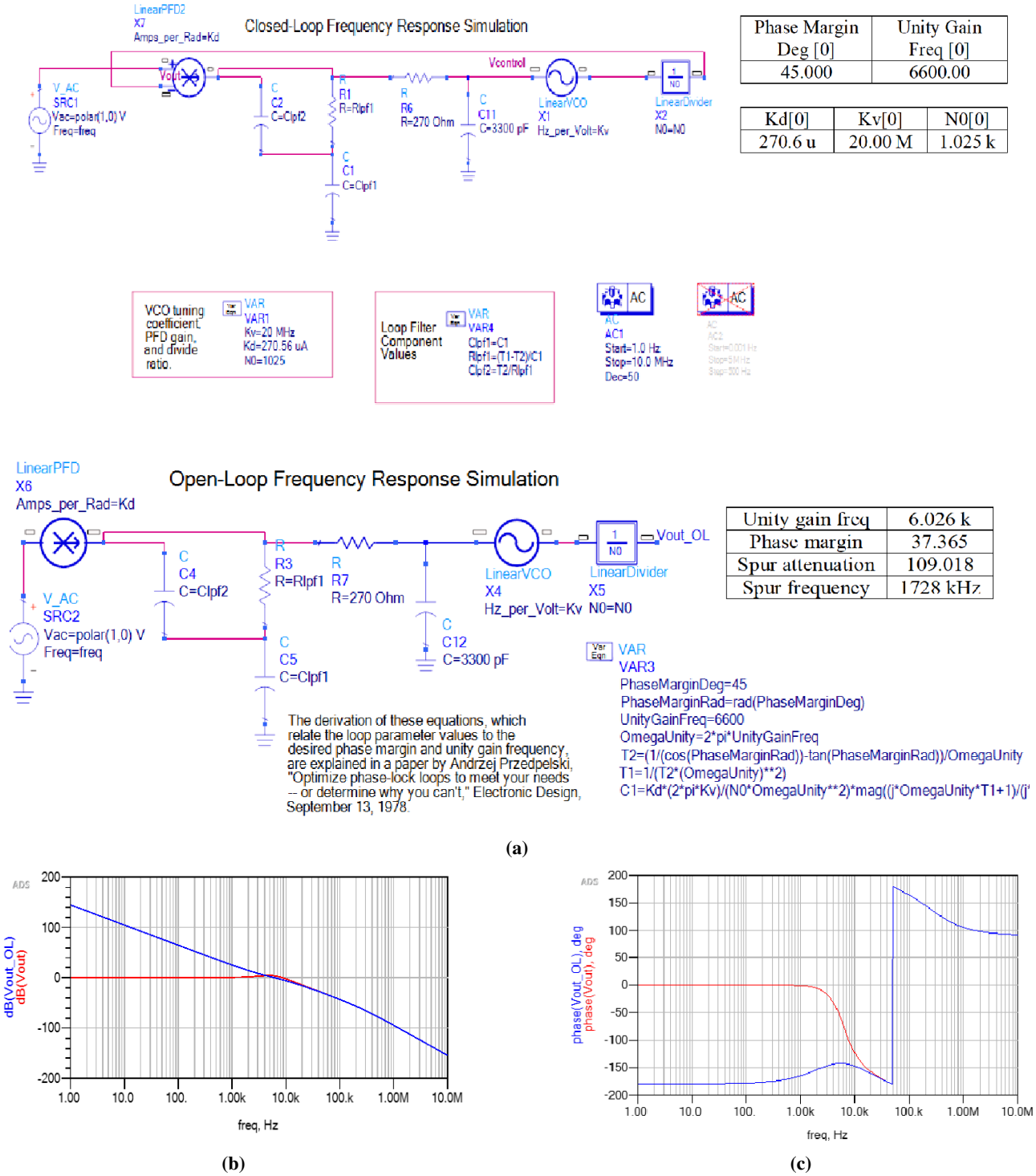
study of the PFD's flexibility and robustness in various operational conditions. These executed simulation results highlight the importance of the Phase-Frequency Detector in precisely detecting and responding to fluctuations in phase and frequency. The high-fidelity simulations help to provide a thorough knowledge of the PFD's behavior, laying the groundwork for further optimization and improvement in CMOS technology applications.

4.2 Simulation outcomes for charge pump

In-depth simulations were run on their own for the PFD and the Charge Pump (CP) so that their individual performances could be evaluated. When the frequency of the reference signal is in the leading position, the PFD shows evidence of the generation of a discernible UP pulse, as shown in Figure 4a however Figure 4b shows how a DOWN pulse is generated whenever there is a lag in the reference signal. Figure 4a provides further insights into the behavior of the charge pump by showcasing the variation in charge pump current (Icp) between the UP and DOWN states. This variation, which registers at approximately 200 μA, is shown. This analysis is essential for understanding the dynamic current transitions that take place within the charge pump during the various operational states. The tuning voltage of the Voltage Controlled Oscillator, also known as the VCO, is an important factor to take into account when trying to eliminate the possibility of a mismatch occurring within the Phase-Locked Loop (PLL) system. According to the results, the optimal tuning voltage for the VCO is located somewhere within the range of 0.4 V to 1.4 V, as was previously mentioned. This range is essential for preserving the synchronicity and harmonious operation of the charge pump within the PLL, which is necessary for ensuring stability and precision in the mechanisms that control frequency.

4.3 Loop design and simulation

Figure 5a delves Open and closed loop design in which desired Phase Margin, Unity Gain Frequency and PFD gain set on schematic. Figure 5b shows open and closed loop amplitude responses of the synthesizer during fractional-N operation, with an output frequency range of 1 Hz − 10 MHz. Note that if the last R-C section of the loop filter is removed, then the simulated unity gain frequency and phase margin match the desired values set on the schematic. Figure 5c shows open and closed loop frequency responses Individual contributions from main noise sources are clearly separated. At 1 MHz, the simulated phase noise of the proposed frequency synthesizer registers roughly −66 dBc/Hz. These simulation results match the empirically measured outcomes extremely well. The charge pump configuration employs a source-switch topology, as illustrated on the right side of Figure 2, featuring discretely programmable current strength. In contrast to the arrangement in [22], the cascade transistor of the switched current source is omitted, primarily owing to constrained voltage headroom. This adjustment is made to mitigate the charge pump circuit's output impedance, resulting in a heightened dependency of



Phase Margin Deg [0]	Unity Gain Freq [0]
45.000	6600.00

Kd[0]	Kv[0]	N0[0]
270.6 u	20.00 M	1.025 k

Unity gain freq	6.026 k
Phase margin	37.365
Spur attenuation	109.018
Spur frequency	1728 kHz

Figure 5. Proposed open and closed loop design, b) Open and closed loop amplitude response, c) Open and closed loop frequency response.

the output current on the output voltage. The PLL architecture is meticulously crafted to ensure VCO lock with a tuning voltage ranging from 350 mV to 450 mV. Within this voltage span, the simulated maximal disparity between the sink and source currents, attributed to the finite output impedance of the NMOS and PMOS current sources. Figure 5b elucidates the experimental outcomes during frequency synthesis mode, focusing on the pinnacle output frequency of 1728 kHz. Figure 5a delves Open and closed loop amplitude response. The comprehensive evaluation extends to Figure 5b providing insight in to the frequency response across multiple samples, thereby offering a holistic perspective on the synthesizer's operational characteristics.

4.4 Comparison with previous research

A comparative analysis is performed with previous study data to examine the efficacy of the Phase-Frequency-Detector (PFD) - Charge-Pump circuit provided in Table 1.

Table 1. The performance and comparison of high-speed charge pump phase locked loop with earlier work.

Specification	Ref [17]	Ref [18]	Ref [19]	Ref [20]	Ref [21]	This work
Technology	180 nm	180 nm	250 nm	130 nm	180 nm	130 nm
Supply Voltage (V)	1.8	1.8	3	1.2	1.8	1.2
Delay Time (ps)	5 us	250	140	80	100	150
Power dissipation (mW)	24.62	10.34	1400	134	33.5	50
Phase Noise	N/A	PN of -95 dBc/Hz at 100kHz offset	PN of -170 dBc/Hz at 1 MHz offset	PN of -163 dBc/Hz at 1 MHz offset	PN of -154 dBc/Hz at 1 MHz offset	PN of -66 dBc/Hz at 1 MHz offset
Operating Frequency (MHz)	6500	3720	2450	3000	5000	2400

The primary focus is on critical performance parameters such as phase margin, current mismatch of the charge pump and charge pump efficiency.

A. Phase Noise: In terms of phase noise performance, our research achieves a notable addition, registering -66 dB/Hz at 1 MHz This represents a substantial improvement compared to many previous studies, where phase noise values above -95 dB/Hz are common. The low phase Noise in our design is crucial for applications demanding high precision and stability.

B. Current mismatch: The research focuses on current mismatch of the charge pump in PFD-CP architecture, aligning with reduction in current mismatch of about 200 uA in modern communication systems. This aligns with the range observed in previous studies, indicating consistency in the application domain.

C. Delay time/Locking time: The delay time in our charge pump design, with a maximum disparity below 150 ps, showcases an improvement over many previous studies, where delay time often range from $250 - 500$ ps. This enhancement is crucial reducing power consumption and enhancing the overall performance of the PFD-CP circuit. In summary, the outcomes of this research demonstrate superior performance in key metrics compared to previous studies. The reduction in settling time, alignment with common operational frequencies, and enhanced charge pump speed collectively position the proposed PFD-CP circuit as a significant advancement in the field. These improvements contribute to the low leakage and high-speed charge pump, addressing key challenges identified in contemporary PFD-CP design.

5. Discussion

The innovative charge pump configuration introduced in this study presents a paradigm shift in low-voltage applications, showcasing superior voltage pumping gains and increased output voltages compared to conventional "Dickson-charge-pump" models. This achievement is attributed to the utilization of anti-phase pumping clocks (1&2), MOS transistors replacing traditional diodes, and a multiplier chain implemented with diode-connected NMOS transistors [8]. The resulting mathematical representation, encapsulated in Equation (1), establishes a foundational understanding of voltage variation at pumping nodes, crucial for subsequent analysis. Key variables such as parasitic capacitance (Cs), pumping clock frequency (f) [3], and output current loading (lo) [2] significantly impact charge pump performance, underscoring the depth of this design methodology. The (PFD) and Charge Pump circuit, central to the phase-locked loop (PLL) system, were meticulously designed and simulated. The PFD, depicted in Fig. **??** and Fig. **??**, plays a pivotal role in detecting phase or frequency differences between reference and feedback signals. The ensuing charge pump circuit, detailed in Figure 5, demonstrates dynamic behavior across charging [1, 2], discharging, and zero current states. The integration of these components was realized through rigorous simulations, and the successful outcomes validate the adaptability and precision of the system in low-voltage scenarios. The study introduces revolutionary low voltage charge pumps that outperform the traditional Dickson charge pump model. Dickson's revised charge pump design makes use of metal oxide semiconductor (MOS) transistors and anti-phase pumping clocks, resulting in superior performance in low voltage settings. The mathematical description of voltage variation across pumping nodes is the basis for later analysis and optimization. The comparative analysis against previous research underscores the superior performance of our Phase Frequency Detector (PFD) Charge Pump circuit. Achieving significantly lower phase noise at 1 MHz, the proposed design surpasses the common threshold observed in earlier studies. The choice of a 2.4 GHz frequency offset aligns with established operational frequencies in modern communication systems. Furthermore, it exhibits enhanced charge pump efficiency, marked by a disparity below 10%, outperforming the typical range found in previous research. These advancements position proposed design as a noteworthy contribution, addressing critical challenges and advancing the state of the art in PFD-CP technology. The design of the Phase-Frequency Detector (PFD) Charge Pump circuit is methodically presented, with an emphasis on the clever integration of D-flip flops, AND gates, NOT gates, NMOS transistors, PMOS transistors, and switches. The PFD simulation results show its reaction to a 2.4 GHz input frequency under various control signals, giving a complete insight of its dynamics. Similarly, the Charge Pump simulation results illustrate the subtle behavior of charge pump current.

6. Conclusion

This research has successfully introduced and implemented an innovative charge pump configuration tailored for low voltage applications. The design, featuring anti-phase pumping clocks and the strategic use of MOS transistors [24], has demonstrated remarkable advancements in voltage pumping gains and output voltages when compared to traditional "Dickson-charge-pump" models. The comprehensive analysis of the PFD, Charge Pump circuit, has revealed the intricate interplay of key components within the phase-locked loop (PLL) system [25]. Simulation results confirm the adaptability and precision of the proposed methodologies, providing a solid foundation for further exploration in the field of low-voltage circuit design.

Future research directions

The success of this study opens avenues for future research to delve deeper into optimizing charge pump configurations and PFDs for even more stringent low voltage scenarios. Fine- tuning the design parameters, such as clock frequencies and transistor characteristics, can further enhance the efficiency and performance of these circuits [26]. Additionally, investigating the integration of advanced materials and fabrication technologies may lead to the development of more robust and energy efficient charge pumps [27]. Exploring novel applications for low voltage charge pumps, such as in Internet of Things (IoT) devices or biomedical implants, presents an exciting direction for research [28]. These applications demand not only low power consumption but also compact and reliable circuitry. Furthermore, the exploration of adaptive control mechanisms and machine learning algorithms in conjunction with charge pumps could contribute to the development of intelligent power management systems.

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Authors Contributions
All authors have contributed equally to prepare the paper.

Availability of Data and Materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of Interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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