Accepted manuscript (author version)

To appear in:
International Journal of Nano Dimension (Int. J. Nano Dimens.)

Online ISSN: 2228-5059 Print ISSN: 2008-8868

Dates:
Received: 15 December 2025
Revised: 16 January 2026
Accepted: 24 February 2026

DOI: https://doi.org/10.57647/ijnd.2026.1703.08

Enhanced Electrostatic Control and Biosensing in a No Junction Gate all Around Hetero Dielectric Tunnel Field Effect Transistor (NJGAA-HTFET): A Nanoscale Study Through Analytical Modeling and TCAD Simulation

Vimala Palanichamy[1*], Sharon Geege Augustine[2], Arun Samuel Thankamony Sarasam[2], Suveetha Dhanaselvam[3], Jayagowri Ramamoorthy[4]

[1]*Department of ECE, Dayananda Sagar College of Engineering, Bengaluru, India*

[2]*Department of ECE, National Engineering College, Tamilnadu, India*

[3]*Department of ECE, Velammal College of Engineering & Technology, Madurai, India*

[4]*Department of ECE, BMS College of Engineering, Karnataka, Bengaluru, India*

**Corresponding Author:* Vimala Palanichamy, Email Address: ervimala@gmail.com

Abstract

In the modern era of miniaturization, Tunnel Field Effect Transistor (TFET) is considered to be a dominant device for low-power applications due to its primary switching mechanism. The concept of TFETs is that quantum tunnelling across a barrier is regulated, whereas in conventional MOSFETs, the thermionic emission across a barrier is regulated. In this paper, the No Junction Gate All Around Hetero Dielectric Tunnel Field Effect Transistor (NJGAA-HTFET) is modelled at large drain voltage, even though the effect of drain voltages is less pronounced. Theoretical tests have proved that using the low-voltage TFETs in logic circuits instead of MOSFETs, will conserve significant amounts of electricity. Hence, this work presents the analytical modelling of the No Junction Gate All Around Hetero Dielectric Tunnel Field Effect Transistor, where surface potential profile, IDS VGS, and IDS VDS characteristics are analytically modelled using the Kane approach. A comparison of TCAD simulation and modeling under various device parameters, including gate oxide dielectric constant, channel lengths, and junction/junctionless structures, is conducted and further discussed to validate the model. The results of the Ion/Ioff ratio of the proposed device prove to be superior to those of conventional JLTFET devices. More specifically, the NJGAA-HDTFET is identified for use as a biosensor to detect various biomolecules.

Keywords: *TFET, Nanometer, No junction, Gate all around, TCAD, Analytical model, Parabolic approximation.*

1. INTRODUCTION

Modification of the device structure and its performance improvement at the device level is essential to meet today's demands. As a result, electronic gadgets are available in small, portable sizes. Traditional devices were found, manufactured and downsized, resulting in newer devices with increased speed, cheaper prices and a greater number of gates packed in a chip. Moore's law came true for various decades, but beyond Moore, this constant field scaling had several disadvantages [1]. Many different device architectures were developed to overcome the limitations of MOSFETs. After the development of the MUGFET (Multi-gate Field Effect Transistor) [2], there was a significant revolution brought in the semiconductor industry, and it became a popular device for extremely low power and high frequency applications. A device with Gates around the structure was also developed [3-5] called as Gate All Around structures. Then the device structure is modified to include a dielectric layer (tox) between the substrate and the channel region. This technology is referred to as Silicon on Insulator (SOI) technology. The SOI technology was employed to construct the FinFET transistor, facilitating many gates to aid charge control in the channel by forming a structure above the silicon [6-9].

As the name suggests, the TFET (Tunnel FET) is working based on quantum tunnelling. It operates on the BTBT (Band to Band Tunneling) principle and is a relevant device for low-power applications [10, 11]. The significant features of TFET allowed it to break past boundaries. To improve the ON current of TFETs, attempts were undertaken to insert a Nanowire into the Channel. The introduction of the Nanowire proved to be quite beneficial in terms of increasing carrier mobility. Devices such as CNTFET and GFET, which utilize carbon as a channel and carbon nanotubes as the foundational material, are advantageous for sensing applications in the semiconductor industry [12, 13]. Unlike a typical MOSFET, it lacks a junction, and the number of doping's controls how much current it can drive. A MOSFET conducts via surface conduction, whereas a Junctionless transistor conducts via bulk conduction [14]. The source, drain and channel regions of Junctionless transistors have consistently high doping concentrations. Because of this, random doping variations do not affect Junction-less transistors [15, 16]. This paper includes performance analysis of the NJGAA-HTFET. Electrical factors such as I_{DS} characteristics and gm that help in deriving the I_{ON}/I_{OFF} ratio were also analyzed. Analytical modelling was used for the relevant research and the results were validated using Silvaco TCAD simulation values.

2. MATERIALS AND METHODS

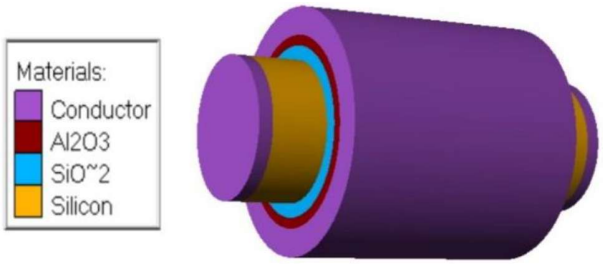

Fig 1. 3D Structure of NJGAA Hetero Dielectric Tunnel FET.

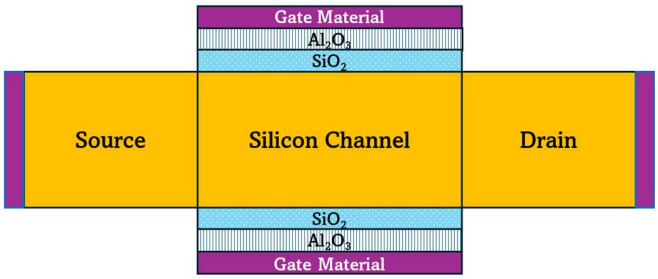

Fig 2. Two-Dimensional diagram of NJGAA Hetero Dielectric Tunnel FET.

A 3-dimensional cylindrical structure is presented in Fig. 1. The Source and Drain terminals are enclosed by a cylindrical tube. The Channel is the region situated between the Source and the Drain. An oxide layer surrounds the Channel. Silicon (Si) is the channel material, while the dielectric layer is Silicon Dioxide (SiO_2), with a dielectric constant of 3.9. Over the SiO_2 layer, a High-K dielectric material is employed representing gate oxide engineering. The Al_2O_3 layer is wrapped around the SiO_2 layer, with a dielectric constant of 9. Figure 2 illustrates the device in 2 Dimension: the oxide layers and the encompassing gate. At the source end of the proposed construction, a portion illustrates the materials utilized to fabricate the device incrementally. The central cylindrical core consists of wrapped oxide material, high-k oxide and a conductor functioning as a surrounding gate.

3. ANALYTICAL MODEL

3.1 Surface Potential

The potential distribution over the device and the channel potential at the interface were computed using the two-dimensional Poisson equation.

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \emptyset(r,z)}{\partial r}\right)+\frac{\partial^2 \emptyset(r,z)}{\partial z^2}=-\frac{qN_c}{\varepsilon_{si}} \qquad (1)$$

The two-dimensional Poisson's Equation for the n-channel TFET is resolved utilizing the parabolic approximation method. The potential distribution is computed in two-dimensional space (along the device's length) via the parabolic approach, and the potential solution is shown as:

$$\emptyset(r,z) = S_0(z) + S_1(z)r + S_2(z)r^2 \quad (2)$$

Where $S_0(z), S_1(z)$ and$S_2(z)$ are the arbitrary constants and functions of z alone.

The boundary conditions necessary for solving Equation (1) are,

a. The device's central Surface Potential,$\emptyset_S(z)$

b. $$\emptyset(r=0,z) = S_0(z) = \emptyset_S(z) \quad (3)$$

c. The central electric field is zero.

$$\left.\frac{\partial\emptyset(r,z)}{\partial r}\right|_{r=0} = 0 \quad (4)$$

d. At Si and SiO2 interface, the electric field is given by

$$\left.\frac{\partial\emptyset(r,z)}{\partial r}\right|_{r=2t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{1}{2t_{si}}\left[\frac{\Psi_g - \emptyset_s(z)}{\ln\left(1+\frac{t_{0x}}{2t_{si}}\right)}\right] \quad (5)$$

e. The source end potential is

$$\emptyset(r=0,\ z=0) = V_{bi} \quad (6)$$

f. The drain end potential is

$$\emptyset(r=2t_{si}, z=L) = V_{bi} + V_{ds} \quad (7)$$

For the simplicity of derivation, the following assumptions are made.

Let $R = 2t_{si}$,$C_f = R\ln\left(1+\frac{t_{0x}}{R}\right)$ and $K^2 = \frac{2}{R}\frac{\varepsilon_{0x}}{\varepsilon_{si}} \times \frac{1}{C_f}$

By applying all boundary constraints from Eq. (3) to Eq. (7) to the parabolic approximation delineated in Eq. (2), the constants S_0(z), S_1(z), and S_2(z) can be expressed as functions of the surface potential Ø_S(r,z).

$$S_0(z) = \phi_s(z) \quad (8)$$

$$S_1(z) = 0 \quad (9)$$

$$S_2(z) = \frac{\varepsilon_{0x}}{\varepsilon_{si}}\frac{1}{2R}\frac{1}{C_f}\left(\psi_g - \phi_s(z)\right) \quad (10)$$

Substituting the Eq. (viii-x) in Eq. (ii), we get

$$\emptyset(r,z) = \emptyset_s(z) + \left(\frac{r^2}{2R}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{1}{C_f}\left(\psi_g - \phi_s(z)\right)\right) \quad (11)$$

The surface potential Ø_s(z) can be derived by solving Poisson's equation (1) with equation (11).

$$\frac{2}{R}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{1}{C_f}\left(\psi_g - \emptyset_s(z)\right) + \frac{\partial^2 \emptyset(r,z)}{\partial z^2} = -\frac{qN_C}{\varepsilon_{si}} \quad (12)$$

Let $K^2 = \frac{2}{R}\frac{\varepsilon_{0x}}{\varepsilon_{si}} \times \frac{1}{C_f}$

$$\frac{\partial^2 \emptyset_s(r,z)}{\partial z^2} - K^2\emptyset_s(z) = -\left(\frac{qN_C}{\varepsilon_{si}} + K^2\psi_g\right) \quad (13)$$

The solution for the Differential Equation (xiii) is given by-

$$\emptyset_s(r,z) = Ae^{Kz} + Be^{-K} + \frac{qN_C}{K^2\varepsilon_{si}} + \psi_g \quad (14)$$

Using the Eq. (vi-vii), the coefficients A and B are expressed as -

$$B = \frac{\left(1 - e^{LK}\right)\left[\psi_g + \frac{qN_C}{K^2\varepsilon_{si}} - V_{bi}\right] - V_{ds}}{2\sinh(LK)} \quad (15)$$

$$A = V_{bi} - \left(\frac{qN_C}{K^2\varepsilon_{si}} + \psi_g\right) - \left(\frac{\left(1-e^{LK}\right)\left[\psi_g + \frac{qN_C}{K^2\varepsilon_{si}} - V_{bi}\right] - V_{ds}}{2\sin\ (LK)}\right) \quad (16)$$

3.2 Electric Field

The surface potential concerning r and z are utilized to distinguish the vertical and lateral electric fields in the NJGAA-HTFET model. The lateral electric field E_Z (z) can be determined by differentiating ∅_s (r,z) (Eq. (14)) with regard to z.

$$E_Z(z) = -\frac{\partial \emptyset_s(r,z)}{\partial z} = K\left(Be^{-Kz} - Ae^{Kz}\right) \quad (17)$$

The vertical electric field $E_r(z)$can be found by differentiating $\emptyset_s(r,z)$ (Eq. 2)) with respect to r,

$$E_r(z) = \frac{\partial \emptyset_s(r,z)}{\partial r} = 2rS_2(z) \quad (18)$$

The total (average) electric field is given by,

$$E = \sqrt{(E_Z)^2 + (E_r)^2} \quad (19)$$

3.3 Drain Current

These gated p-i-n diode transistors operate under the principle of band-to-band tunnelling (BTBT). Because the semi-classical technique lacks a straightforward mechanism to account for quantum mechanical (QM) effects, BTBT can be introduced using Kane's model as an additional term called BTBT generation rate (or) tunnelling generation rate (GBTB). Consequently, the drain current is computed throughout the volume of the proposed NJGAA-HTFET structure utilizing the carrier generation rate from band to band.

Ez is the lateral electric field along the Channel in the z-axis (0 to L), which is significant in calculating

the device's drain current and transconductance. The drain current analysis ignores the radial electric field (Er) since tunnelling occurs mostly along the z-axis at the source/channel contact.

Using Kane's model, the following is the equation for tunnelling generation rate GBTB:

$$G = A_{kane} E_Z (E_{avg})^{\beta-1} e^{-\left(\frac{B_{kane}}{E_{avg}}\right)} \quad (20)$$

Akane and Bkane are tunneling-dependent parameters, and β=2.5 for the direct tunneling. The term "Eavg" stands for "average electric field over the tunnelling volume" and is

$$E_{avg} = \frac{E_g}{qL_{path}} \quad (21)$$

Where, *L*path is the instantaneous length of the BTBT tunneling path.

By integrating the BTBT generation rate in lateral directions across the entire tunnelling volume, the drain current is calculated and is provided by-

$$I_D = q \int G \, dV = q \int A_k E_Z (E_{avg})^{\beta-1} e^{-\left(\frac{B_k}{E_{avg}}\right)} dV \quad (22)$$

4. RESULTS AND DISCUSSION

MATLAB was used to implement the results of the derived analytical model. The analytical results and the simulation results from Silvaco TCAD are found to match well. The modelled results are represented by lines, whereas symbols represent the simulated results. In addition, the proposed device is capable of acting as a label-free biosensor. By changing each biomolecule's unique K-value, various biomolecules can be identified.

4.1 Performance Analysis of NJGAA-HTFET

Fig. 3 plots the Surface Potential (∅_s) variation over the channel length, L. The Surface Potential (volt) vertical axis fluctuates with the horizontal axis of channel length (m). The graph illustrates the variance across three separate V_{GS} levels. The accumulation of charge carriers at the drain end exceeds that at the source end, resulting in an increasing potential along the channel length, which is greater at the drain end than at the source end. The structure attains its maximum value at an elevated V_{GS} of 1V.

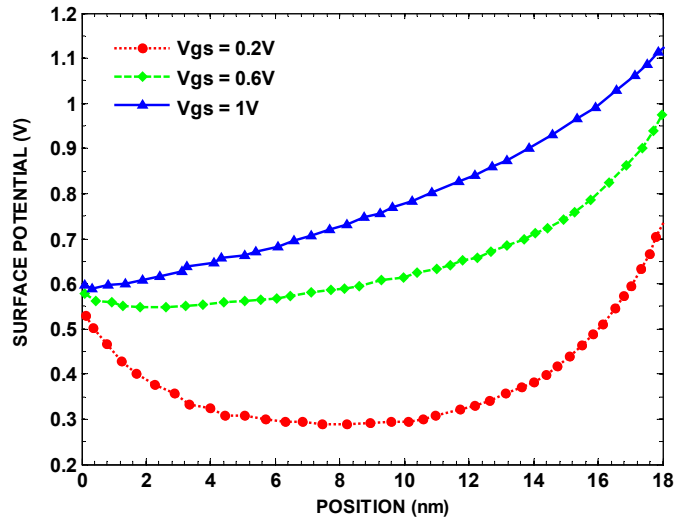

Fig 3. Surface Potential across the Channel Length.

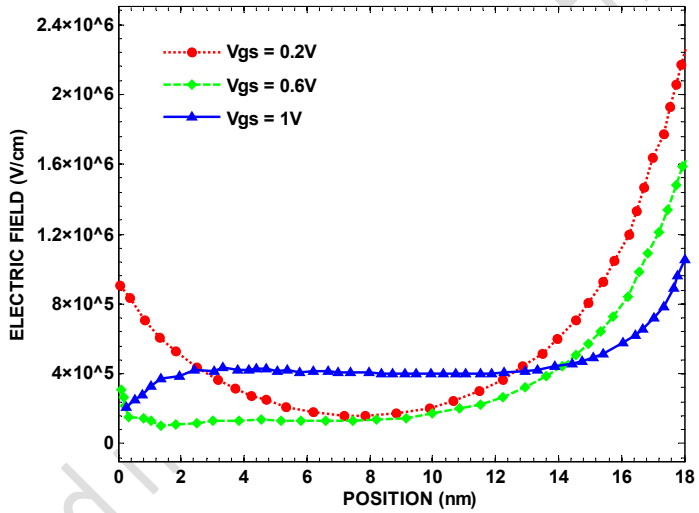

Fig 4. Electric Field across Channel Length.

Figure 4 illustrates the variations in the Electric Field along the channel length. The electric field (V/cm) along the y-axis depends on the channel length (m) along the x-axis. The electric field is presented for three distinct V_{GS} values; the electric field, E(z), at the source end and along the channel length is nearly identical; however, the electric field at the drain end increases. The electric field at the drain side is greater than at the Source, which can be found to the superior potential at the drain end. The three distinct electric field plots illustrate that the electric field at the drain terminal decreases as the V_{GS} value increases, indicating that the lateral electric field at the drain terminal exerts a diminished influence with rising V_{GS} values.

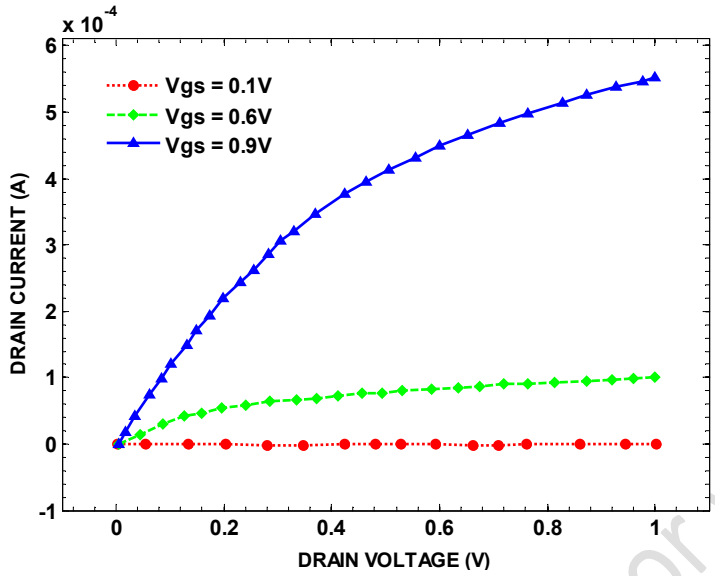

Fig. 5 Drain current (I_D) versus drain-to-source voltage (V_{DS}) characteristics of the device for various gate-to-source voltages (V_{GS}).

The plot of drain current (I_D) versus drain voltage (V_{DS} for various V_{GS} is illustrated in Fig.5. The horizontal axis measures drain voltage (volts), whereas the vertical axis measures drain current (amperes). The drain current is 0 mA, and the device is non-conductive when V_{GS} equals 0.1 V. When V_{GS} increases from 0.1V to 0.6V, I_D equals 0.1mA. The I_D value swiftly ascends to a maximum of around 0.6mA when the peak V_{GS} value of 0.9V is applied. Table 1 compares the performance of several JLTFET architectures using three important parameters: drive current (I_{ON}), leakage current (I_{OFF}), and I_{ON}/I_{OFF} ratio. The proposed NJGAA-HDTFET is advantageous due to its high ON current (10^{-3} A/μm) with a high I_{ON}/I_{OFF} ratio (10^{12}), enabling faster switching and providing better performance for high-speed applications.

Table:1 Comparison of I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} ratios for Various JLTFET Architectures.

Device	I_{on}(A/μm)	I_{off}(A/μm)	I_{on}/I_{off}
GAA-H-JLNTFET [17]	10^{-5}	10^{-17}	10^{12}
C-JLNTFET [17]	10^{-7}	10^{-17}	10^{10}
NT-HJLTFET [18]	10^{-2}	10^{-13}	10^{11}
NT-JLTFET [18]	10^{-4}	10^{-13}	10^{9}
NW-JLTFET [18]	10^{-6}	10^{-16}	10^{10}
NJGAA-HDTFET (Proposed)	10^{-3}	10^{-18}	10^{15}

Figure 6 illustrates the transconductance curve concerning gate voltage (V_{GS}) for various drain-source voltages (V_{DS}). The transconductance (Siemens) on the vertical axis fluctuates with the horizontal axis's gate voltage (volts). The device's transconductance indicates the output drain current corresponding to a specific input gate bias voltage. Transconductance remains at zero from 0V to 0.4V (V_{GS}) and thereafter increases as VGS exceeds 0.4V. As the value of V_{DS} increases, the value of transconductance also increases. When V_{DS} is 0.1V, the transconductance value is below 0.1 ms. Transconductance levels commence their ascent at a V_{DS} of 0.6V, culminating at a high of 1.6mS when the gate voltage reaches 1V. The transconductance value constantly increases from a gate voltage of 0.9V to 1V, to a maximum of 2ms. Consequently, transconductance elevates in conjunction with the value of V_{DS}.

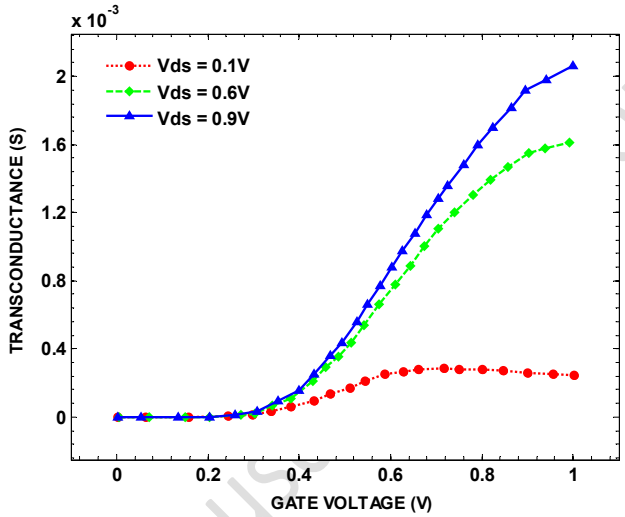

Fig 6. Transconductance vs Gate Voltage for different V_{DS} values.

4.2 Application of NJGAA-HDTFET for Low-Power Biosensing

The biosensor application of the proposed NJGAA-HDTFET shown in fig.7 and it is discussed in this section. The dielectric modulated-based approach is used to relate the biosensor to detect immobilized biomolecules. The different biomolecules and their permittivity are listed in Table 2, used for this simulation study.

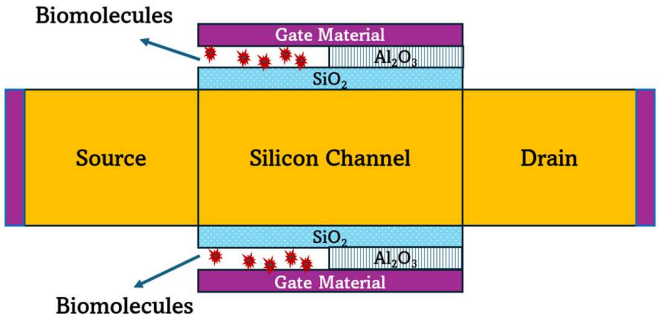

Fig 7. NJGAA-HDTFET device structure for biosensing applications.

Table:2: Biomolecules and their dielectrics used for simulation.

S.No	Biomolecules	permittivity
1	Biotin	2.64
2	Ferricytochrome	4.7
3	Bacteriophage	6.3
4	Keratin	8

The sensitivity of the biosensor is measured to prove its application. Fig.8 illustrates how the drain current changes with gate voltage for various dielectric constants (K) of biomolecules. It has been observed that the drain current increases with gate voltage and significantly influences dielectric values. The sensitivity factor is equivalent to the drain current. The drain current value differs when different types of biomolecules are immobilized in the cavity region. The larger K values exhibit higher drain current than the lower K values. This occurs because a greater dielectric constant improves the gate capacitance, providing better control of the Channel, resulting in stronger inversion and thereby improving carrier flow.

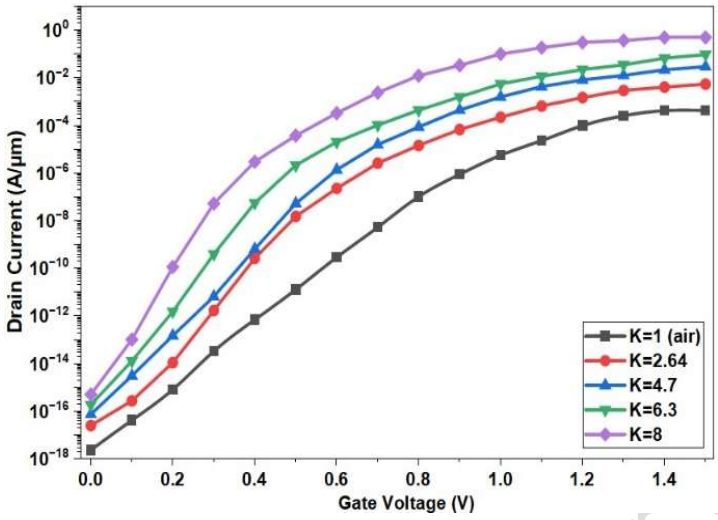

Fig 8. Detection of various Biomolecules in the NJGAA-HDTFET device structure and its dielectric values.

Small changes in the output signal can identify the efficiency of a biosensor due to target biomolecules. It can be represented mathematically as follows:

$$Sensitivity = \frac{I_{DS}(bio) - I_{DS}(air)}{I_{DS}(air)} \quad (23)$$

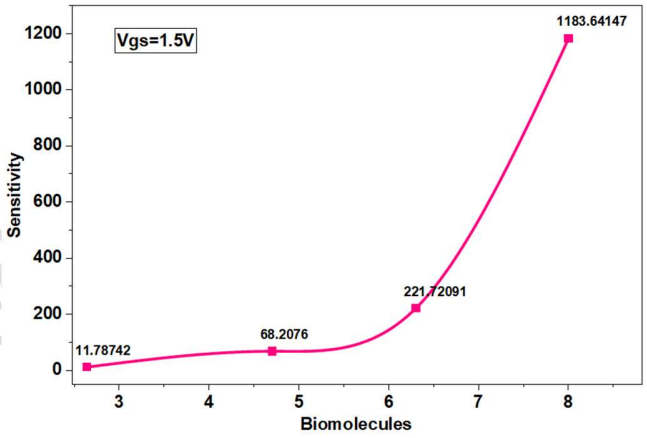

Fig 9. Biomolecule sensitivity as a function of the K value.

Fig.9 illustrates that the sensitivity of biomolecules increases as the corresponding K value rises. The biosensor's sensitivity is minimal at low biomolecule dielectric concentration and shows an apparent increase for high dielectric concentrations, with the highest sensitivity of 1183 at 8 as the dielectric value. This implies that the proposed sensor responds well and is suitable to detect higher biomolecule dielectric concentration.

5. CONCLUSION

A simulation study for a No Junction Gate All Around Hetero Dielectric Tunnel FET (NJGAA-HDTFET) is performed in our research, coupled with a physics-based analytical model, and the findings are validated. Simulations of parameters such as Surface Potential, Electric Field and Drain Current were carried out to improve the proposed device's characteristic output. The 18nm technology used produced a superior result by outperforming the I_{ON}/I_{OFF} ratio. The gate metal work function, when Aluminum is used, performed better. The intrinsic Channel's surface potential is calculated by solving the 3-D Poisson's equation with a parabolic approximation. An extended Kane's model was used to calculate the drain current in the model. As a result, the suggested analytical model shows enhanced performance and can offer insight into future TFET technology in low-power and high-speed switching applications.

Declarations:

Conflict of Interest
The authors declare that they have no conflict of interest.

Funding
This research did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors.

Data Availability
The data that support the findings of this study are available from the corresponding author upon reasonable request.

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