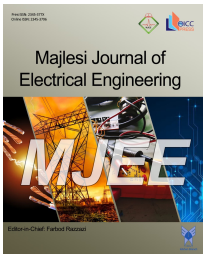

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DC link Voltage balancing for enhanced performance in multilevel inverter-based distribution static synchronous compensator

Kalagotla Chenchireddy[1,*], Mulla Gouse Basha[1], Vislavath Kumar[2], Shabbier Ahmed Sydu[3]

[1]*Department of Electrical and Electronics Engineering, Geetanjali College of Engineering and Technology, Hyderabad, India.*
[2]*Department of Electrical and Electronics Engineering, Teegala Krishna Reddy Engineering College, Hyderabad, India.*
[3]*E&E Section, Department of Engineering,University of Technology and Applied Sciences, Al-musannah, Oman.*

[*]**Corresponding author:** chenchireddy.kalagotla@gmail.com

Original Research

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Abstract:

This article describes the use of a sliding mode controller (SMC) in conjunction with an integral (PI) controller for a MLI based DSTATCOM to balance DC side voltage, control a cascaded H-bridge inverter, and compensate for power quality issues related to current harmonics. Several benefits come with using SMC for distribution static synchronous compensator (DSTATCOM) link voltage regulation, including a decrease in switching ripple in the DC side voltage and a steady DC side capacitor voltage under dynamic conditions. A DSTATCOM-based CHBMLI supplying three-phase loads is used to implement the SMC algorithm. When using the suggested dc link voltage balancing method, the DSTATCOM characteristics perform satisfactorily in terms of voltage balancing and the removal of power quality issues such as current harmonics. Additionally, the DSTATCOM's improved voltage balancing (IVB) scheme is used to compare the performance of the PI controller with the SMC's improved voltage balancing method. The real-time investigation validates the performance characteristics, and the enhanced voltage balancing scheme of SMC results in better transient and steady state response.

Keywords: Distribution static synchronous compensator; PI Control; Sliding mode controller (SMC); Power quality; Cascaded H-Bridge multilevel inverter (CHBMLI)

1. Introduction

Most industrial applications require high voltage and high power with enhanced power quality in terms of the recommended level of total harmonics distortion with unity power factor. The multilevel converter permits the increased power rating with improved efficacy without compromising its performance characteristics [1]. The multilevel converter is used to synthesize almost sinusoidal voltage waveforms from low switching frequency, low switching loss, and nearly insignificant EMI/CMV [2]. The rating of the multilevel inverter can be increased by series/parallel combinations of small voltage level to achieve the required voltage rating without increasing the individual switching device rating. In addition, the series/parallel combination of small voltage allows the reduced distortion at the inverter terminal voltage [3]. In literature; the two-level voltage source converter-based APF is used in low-voltage and low-power applications. However, for medium voltage/medium power and high voltage/high power applications, MLI-based voltage source inverter provides more advantages [4]. On the contrary, the two-level voltage source converters have many disadvantages in medium/high voltage applications and they require complex transformer, bulky switching inductor, snubber, and also sophisticated control circuitry [5]. In addition, MLI offers several benefits namely the

elimination of bulky transformer, reduced size of switching reactor, low switching voltage stress, modular structure which allow the expansion of level for medium voltage and high voltage applications [6]. Moreover, MLI-based active power filter has low total harmonic distortion for the additional number of voltage levels with reasonable rise in cost. The basic topology of MLI can be categorized as (a) Diode Clamped MLI (DCMLI) (b) Flying Capacitor MLI (FCMLI) (c) Cascaded H-bridge MLI (CHBMLI). The selection of MLI topology for high voltage and high power applications depends on so many factors such as system parameters, voltage rating, power rating, size and cost, etc [7].

In this paper, the SMC algorithm along with IVB scheme is employed for distribution static synchronous compensator (DSTATCOM) voltage regulation and elimination of current related harmonics power quality problems. The reference current of the DSTATCOM is estimated with SRF along with SMC to regulate the voltage and improve the power quality at the PCC. In literature, various control methods are available such as IRP theory method, Icos ∅ control method, Adeline based control method, and notch filter based control method are used to sense the load current for estimation of reference phase current. For the improved performance characteristics of DSTATCOM, the SMC is used along with the SRF method based on the load current sensing method. The DSTATCOM power loss component and dc link voltage supports are obtained from the dc link voltage error. The dc link voltage error is processed through the SMC controller which gives the robust control of DSTATCOM during dynamic conditions. The current harmonics-related power quality problems at the point of common coupling are improved within the recommended standards of IEEE-519 standards.

In this present paper, the CHBMLI-based DSTATCOM dc link voltage is regulated with IVB method along with SMC controller and PI controller. The DSTATCOM with IVB method using SMC controller suppresses the overshoot and undershoot in the DC side voltages of the capacitor. The reduced peak-to-peak ripple in dc link voltage results in decreased capacitor size of the DSTATCOM. Moreover, the DSTATCOM improves current harmonics-related power quality issues. With reduced harmonics current in the source current leads to improved utilization of supply.

2. Configuration of CHBMLI-based DSTATCOM

Figure 1 depicts the entire electrical power system network with DSTATCOM. Electrical sources, the DSTATCOM power circuit, and a load make up the DSTATCOM system. The three phases that make up the system's electrical sources are separated by 1200. Eleven IGBTs in each leg, three interface inductors, and three dc link capacitors make up the DSTATCOM power circuit. Three commutation inductors and six diode bridges with a resistive-inductive load on the dc side are used to realize the non-linear load. The CHBMLI consists of several H-bridge inverters connected in series. Each H-bridge inverter typically consists of four power switches (usually IGBTs or MOSFETs) that

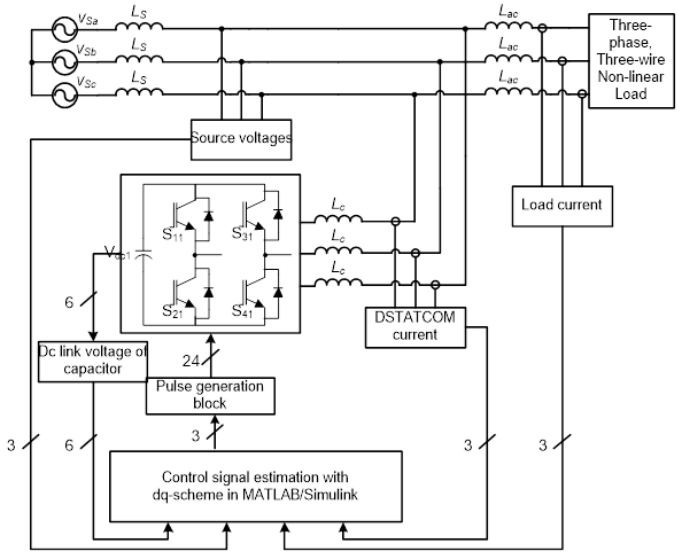

Figure 1. Topology of DSTATCOM

can be controlled independently. The number of voltage levels in the output waveform is determined by the number of H-bridges. For each H-bridge, the output voltage can be either +Vdc, 0, or -Vdc, where Vdc is the DC voltage across the capacitor. The output voltage of each H-bridge is summed up to produce a stepped multilevel waveform. The resulting waveform has a higher resolution and is capable of closely approximating a sinusoidal waveform. The multilevel waveform generated by the CHBMLI has significantly lower harmonic content compared to conventional two-level inverters. This is crucial in DSTATCOM applications where the objective is to compensate for reactive power and improve power quality.

3. Control scheme of the DSTATCOM

The system terminal voltages can be written as

$$\begin{aligned} v_{sa_i} &= V_{m_i}\sin(\omega t) \\ v_{sb_i} &= V_{m_i}\sin(\omega t - \frac{2\pi}{3}) \\ v_{sc_i} &= V_{m_i}\sin(\omega t - \frac{4\pi}{3}) \end{aligned} \quad (1)$$

The corresponding load currents can be given as

$$\begin{aligned} i_{La_i} &= \sum I_{Lan_i}\sin n_i(\omega t) - \theta_{an_i} \\ i_{Lb_i} &= \sum I_{Lbn_i}\sin\{n_i(\omega t - \frac{2\pi}{3}) - \theta_{bn_i}\} \\ i_{Lc_i} &= \sum I_{Lcn_i}\sin\{n_i(\omega t - \frac{4\pi}{3}) - \theta_{cn_i}\} \end{aligned}$$

The SRF method is based on the transformation of the synchronously rotating currents in d-q frame. The simple building blocks of the synchronously rotating reference frame are shown in Figure 2. The measured input phase voltages and load currents such as v_{sa}, v_{sb} and v_{sc} and i_{La}, i_{Lb} and i_{Lc} are fed to the signal processing controller [8–10]. The voltage signals are used in a phased locked loop to compute the voltage templates such as sine and cosine signals.

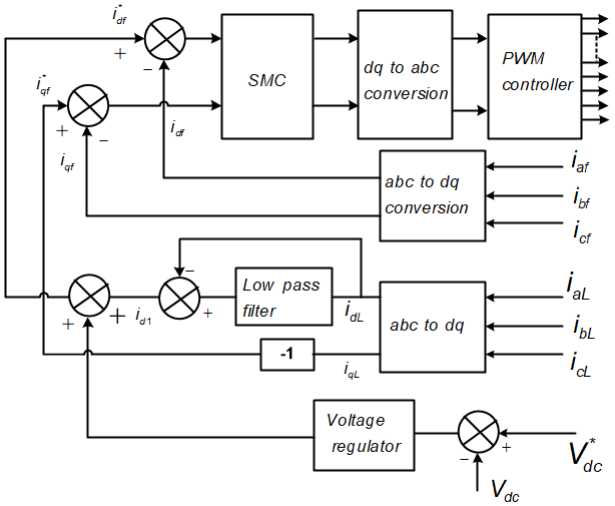

Figure 2. Control scheme based on SRF for DSTATCOM control.

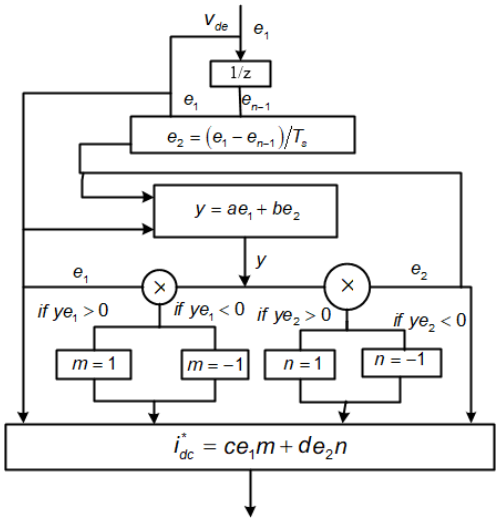

Figure 3. SMC controller for dc voltage regulation of DSTATCOM.

Initially, current signals are transformed into d-q quantities. The transformed d-q signals are filtered and transformed back to the abc frame such as, i_{sa}, i_{sb} and i_{sc} subsequently, abc signals are fed to current controller and are used to generate pulse width modulated signals. Finally, the modulated signals are fed to the DSTATCOM. Therefore, this control method is used as the controller for DSTATCOM as shown Figure 1. Similar to the instantaneous reactive power theory, the current component α–β is generated from abc current signals. The voltage unit templates such as sine, cosine, and transformation angle are used to transform α–β current to d–q current frame defined as Park's transformation

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2}$$

SRF isolator is used to extract the harmonics component of each id and iq iq using low-pass filters (LPFs). The LPF is realized using a moving average at 100 Hz. The extracted harmonics components of $\tilde{i}_d$ and $\tilde{i}_q$ are transformed back to the α–β frame by means of the reverse Park's transformation.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sa} \\ i^*_{sa} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i^*_0 \\ i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} \tag{4}$$

From (4), the α–β frame is transformed to three-phase reference source current such as a-b-c phases to track the desired source with DSTATCOM. The control method based on SRF and SMC is shown in Figure 2.

4. DC voltage balancing

Figure 3, SMC and PI controllers, illustrates the IVB scheme of the CHBMLI-based DSTATCOM. Both average and individual balance are part of the plan. In order to ascertain the capacitor's maximum voltage and contrast it with a reference voltage, individual balancing is utilized. Until the voltage of the capacitors is balanced, the maximum value of the capacitors is changed once. Comparably, the voltage balancing of each leg of the CHBMLI-based DSTATCOM employs average balancing.

The SMC control method is used for the control of three-phase CHBMLI-based DSTATCOM. The SMC control method offers robust control in dynamic conditions in response to the overshoot and undershoots of dc-link voltage during load variation. In some of the cases, the SMC method has certain limitations such as steady-state error [11–13]. On the other hand, the SMC monitors reference with minimal steady state error and very robustly. The flow chart of the SMC control method used with improved voltage balancing is presented in Fig. 4. The SMC control method is used for meeting losses in DSTATCOM and load active

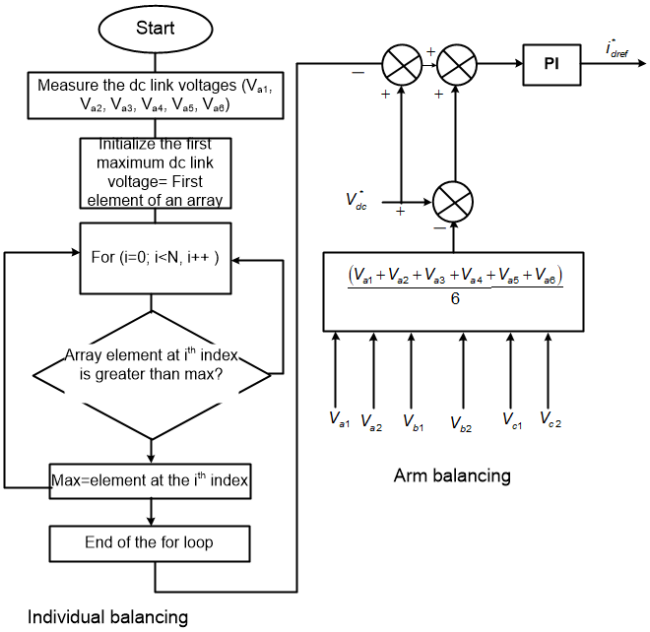

Figure 4. IVB control scheme for DSTATCOM.

power demand. In SMC, compensating currents of DSTATCOM are regulated to slide beside the reference trajectory. The SMC based control algorithm detects the deviation of signal from sliding surface and rapidly restores to the switching control signal of DSTATCOM to track the reference trajectory. The SMC control algorithm provides robust performance under uncertain conditions such as external disturbance. The loss component of the reference current is estimated from the dc link in SMC algorithm.

The measured dc link is filtered using a low pass filter and compared with reference voltage $v_{dc}^{*}$to obtain an error signal. The measured DC voltage of DSTATCOM v_{dc} is filtered by means of a LPF and it is compared with the reference set dc link voltage v_{dc}^{*} to generate the error signal, e_1 as

$$e_1 = v_{dc}^{*} - v_{dc} \tag{5}$$

Also, the derivative of the above equation gives

$$e_2 = \dot{e_1} = v_{dc}^{*} - v_{dc} \tag{6}$$

In addition, the derivative of the above equation can be written as

$$e_2 = \dot{e_1} = \frac{1}{T_s}\{e_1 - e_{(n-1)}\} \tag{7}$$

where e_1, e_2 are used to represent the state variables and $e_{(n-1)}$ is used to represent the previous sample value and T_s is the corresponding sampling time. The parameters m, and n are selected from the DC-link voltage errors. The values of m and n are found from the following logic of the algorithm

$$\begin{aligned} m = +1 \quad \text{if} \quad ye_1 > 0 \quad = \quad -1 \quad \text{if} \quad ye_1 < 0 \\ n = +1 \quad \text{if} \quad ye_2 > \quad = \quad -1 \quad \text{if} \quad ye_2 < 0 \end{aligned} \tag{8}$$

where 'y' is the switching hyper plane of the function of SMC control $y = ae_1 + be_2$. The dc link loss component and dc capacitor supporting current are found as

$$i_{dc}^{*} = ce_1 m + de_2 n \tag{9}$$

5. Simulation results

Fig. 1 depicts the entire electrical power system with DSTATCOM. The electrical sources block set of the Simpower system library is used to create the three-phase electrical sources for the DSTATCOM. Power electronics and the Simpower system's element library are used to realize the nonlinear. The Simpower system library of Simulink and its power electronics components are also used to implement the DSTATCOM. DSTATCOM is utilized with two separate controllers, such as the PI and SMC controllers. Table 1 shows the system parameters. The Simulink library's control blocks are used to develop the DSTATCOM power circuit and control scheme. Figure 5 illustrates the DSTATCOM simulated response using a PI controller. Before DSTATCOM is executed, the source current first follows the load current. The load current's waveform is severely

Table 1. System parameters for simulation.

S.No	Parameter	Simulation Parameter
1	Source	Vpeak=230V & f=50Hz
2	DC-Link voltage	450V
3	DC bus capacitance	4700μF
4	Filter inductance	5mH
5	Switching frequency	1kHz

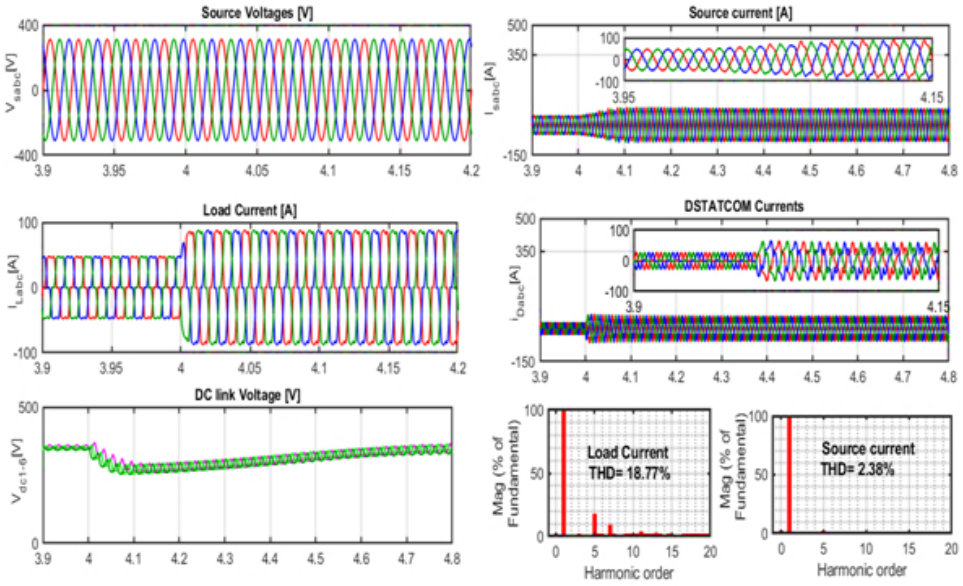

Figure 5. Simulated waveforms of DSTATCOM with PI controller.

distorted and stepped in shape. The existence of triplen harmonic components in the load current is the cause of this characteristic. When the DSTATCOM is turned on, the source voltage waveform is followed by a source current waveform that tends to be almost sinusoidal. Both the voltage and current waveforms have power factors that are nearly equal to unity. It takes approximately 4-5 cycles for the source current to stabilize. Fig. 5 displays the DSTATCOM capacitor's associated dc side voltage. Fig. 6 shows the THD of the source current prior to harmonics reduction. It takes nearly 0.7 seconds for the dc voltage of DSTATCOM to become steady. Before harmonics are eliminated by DSTATCOM, the source current's overall harmonic distortion is 18.77%. As shown in Fig. 3, the THD of the source current is decreased to 2.38% after compensating with DSTATCOM.

Figure 7 displays the DSTATCOM's current waveforms with an SMC-based SRF. The source current initially follows the load current before DSTATCOM execution. The load current's waveform is severely distorted and stepped in shape. The existence of triplen harmonic components in the load current is the cause of this characteristic. Following the source voltage waveform, the source current waveform tends to almost have a sinusoidal waveform once DSTATCOM is turned on. Both the voltage and current waveforms have a power factor of unity. It takes roughly two to three cycles for the source current to stabilize. Fig. 6 displays the DSTATCOM capacitor's associated dc side voltage. It takes nearly 0.4 seconds for the DSTATCOM's dc voltage to stabilize. Fig. 6 displays the source current's total harmonic distortion prior to harmonics removal. Before harmonics are eliminated by DSTATCOM, the source current's overall THD is 18.78%. The source current's THD is decreased to 2.13% after DSTATCOM adjustment, as shown in Fig. 6. The simulated results achieved with the SMC based control scheme outperform the standard PI control based SRF

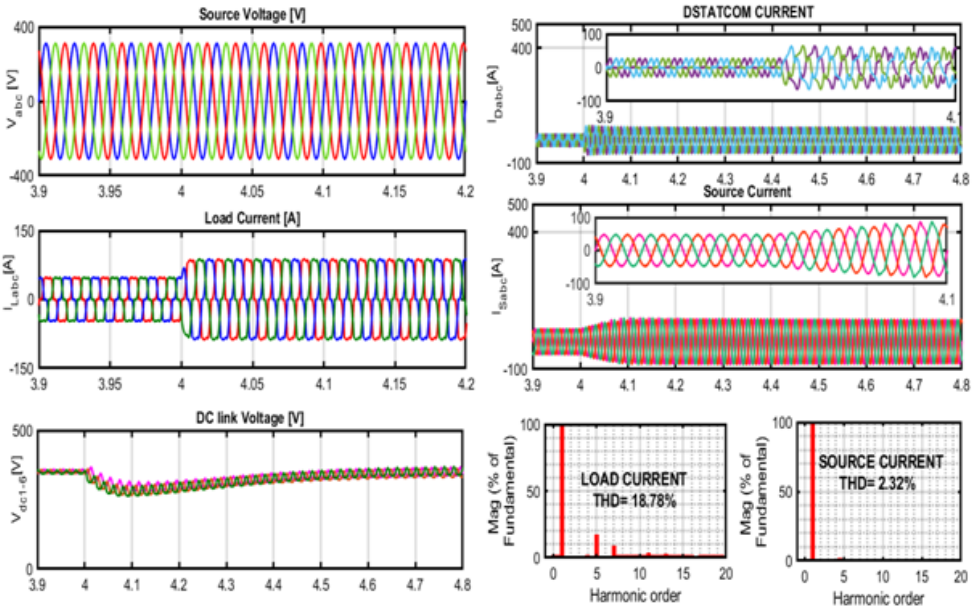

Figure 6. Simulation characteristics of DSTATCOM.

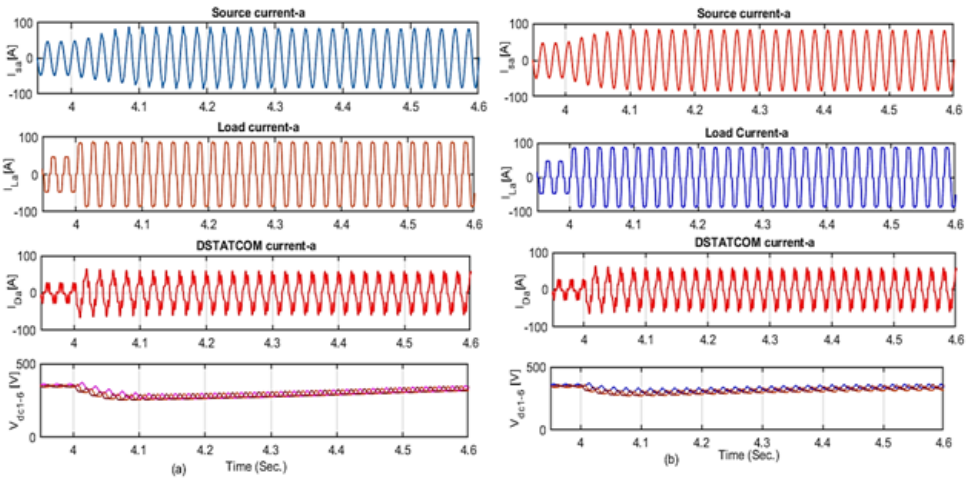

Figure 7. Simulated waveforms of DSTATCOM with SMC/PI.

Table 2. Comparative study of improved voltage balancing of CHBMLI DSTATACOM with PI/SMC.

Parameter	DSTATCOM with PI Controller	DSTATCOM with SMC controller
Source current THD (%)	2.38	2.32
Settling Time(Vdc-Voltage) (s)	0.7	0.4
Settling Time (Source current) (cycle)	4-5	3-4

schemes, according to the characteristics DSTATCOM. To maintain balance among the capacitor voltages across the H-bridges, balancing algorithms are implemented. This ensures that the voltage levels are evenly distributed, enhancing the reliability and efficiency of the inverter. The CHBMLI configuration in DSTATCOM applications provides a flexible and efficient solution for generating high-quality output voltage with reduced harmonic distortion, contributing to improved power quality in distribution systems.

The comparative simulation study of the DSTATCOM with PI/SMC control is shown in Fig. 7. The corresponding dc link voltage with load variation is also depicted in Fig. 8. From the simulated comparative study, the SMC based improved voltage balancing algorithm outperforms than PI controlled-based improved voltage balance during dynamic conditions. However, the steady-state performance characteristics are identical for both PI control-based voltage balancing strategy and SMC-based control strategy. Table 2 shows the comparative results.

6. Conclusion

This paper adopts the DSTATCOM based on CHBMLI for voltage balancing with an enhanced suggested scheme and current harmonics elimination in the electrical system's source current. The purpose of the simulation study is to compare the DSTATCOM's performance with two different controllers for the voltage balancing scheme. The comparison findings demonstrate that, under dynamic situations, the enhanced voltage balancing control with SMC control scheme works better than those of proportional and integral. Superior voltage balancing and an SMC control scheme give the CHBMLI-based DSTATCOM superior steady-state responsiveness than the PI control schemes. SPWM is used to create the firing pulse of the CHBMLI-based DSTATCOM.

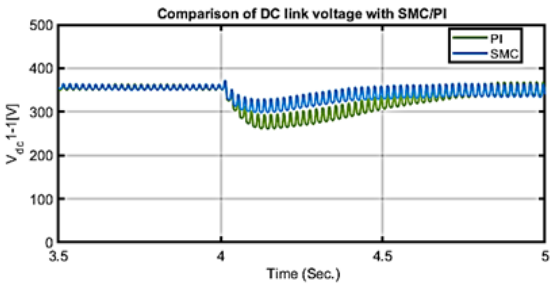

Figure 8. Simulated DC link voltages waveform of DSTATCOM with SMC/PI.

Authors Contributions
All the authors have participated sufficiently in the intellectual content, conception and design of this work or the analysis and interpretation of the data (when applicable), as well as the writing of the manuscript.

Availability of data and materials
Data presented in the manuscript are available via request.

Conflict of Interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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