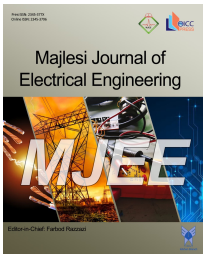

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An enhanced asymmetrical multilevel inverter with reduced switch count utilizing a DC source

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Original Research

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Abstract:

This research paper introduces a modified single DC-sourced multilevel inverter (MLI) consisting of several cells made from a controlled switch, a diode, and a capacitor to generate voltage levels in series connection with the H-bridge. By increasing the number of cells more output voltage levels can be generated in proposition to $2n+3$ for symmetrical multilevel inverter (S-MLI) and maximum $2^{(N+1)}+1$ for asymmetrical multilevel inverter (A-MLI), where N is the number of connected cells. In this article, the proposed inverter utilizes seven control switches, three power diodes, a DC voltage source, and three floating capacitors to generate nine-level (S-MLI), fifteen-level, and seventeen-level (A-MLI) output. By employing a modified single DC source configuration, we achieve a substantial reduction in the number of isolated DC sources and switches required for operation. The reduction in control switches minimizes the requirement of gate driver and protection circuit. This enhancement not only simplifies the circuitry but also enhances the inverter's cost-effectiveness and efficiency. A comparison of proposed and other recently developed single-sourced topologies has been done to show the benefits of the proposed topology. The performance of the proposed modified inverter topology is analyzed through MATLAB/Simulink and validated by a laboratory prototype. Through extensive simulation and analysis, we demonstrate the improved performance, reduced component count, and complexity of the proposed MLI design.

Keywords: Multilevel inverter (MLI); Nearest level control (NLC); Reduced switch inverter; Single DC source

1. Introduction

In 1975, MLI was first introduced in the field of DC to AC power conversion and the demand for multilevel inverters (MLI) has been increasing promptly [1]. Nowadays, to reduce harmonic distortion and filtering requirements multilevel inverters are developed with a high number of output levels [2], [3]. The multilevel inverter is a crucial technology and performs a vital role in high voltage DC transmission, AC motor drives, active filters, flexible AC transmission systems (FACTs), electric and hybrid electric vehicles, static var compensators, utilization and integration of renewable energy sources, and uninterruptible power supplies [4–14].

Cascaded H-bridge converter (CHB), flying capacitors (FC) converter, and neutral point clamped (NPC) converter are widely used conventional topologies of the multilevel inverter. Among these topologies, the flying capacitor and neutral point-clamped converter work with a single DC source. Nevertheless, the utilization of flying capacitors and neutral point clamped inverters necessitates the incorporation of several components operating at higher voltage levels. Consequently, maintaining control over the equilibrium of the capacitor voltage becomes a challenging task due to the complexity involved [15]. Furthermore, cascaded HB inverters possess certain limitations such as a substantial reliance on isolated DC sources and a deficiency in boost capacity [16]. It is worth mentioning that MLIs employing the switched capacitor (SC) technique possess the ability to automatically balance the voltage across the capacitors and amplify the input voltage. [17, 18]. Although the excellent output quality of MLI has been known for quite a while, the quality of isolated DC sources, the higher number of components, and the overall complex system have restricted

their use in many applications. MLI topologies with lesser component counts are more efficient and reliable [19–21]. Several researchers are currently trying to produce elevated levels of voltage by employing a reduced number of components, a decreased amount of direct current sources, and enhanced amplification capabilities. [22]. To address the aforementioned problem, several single-source switched-capacitor multilevel inverters (SCMLIs) were put forward. [23–25]. In reference [23], the inverter successfully attained a seven-level output by utilizing only one source. Furthermore, additional levels were obtained through the implementation of extended structures as described in references [24, 25]. All of these configurations utilize the H-bridge to alter the orientation of the resulting voltage.

In this article, a modified topology of a single-phase single DC-sourced multilevel inverter has been introduced. The primary objective in designing this topology is to achieve increased voltage gain while minimizing the number of components required. This design also focuses on modularity, allowing for a structured and organized system. Additionally, redundancies in voltage levels are implemented to enhance reliability and stability. Here, the proposed inverter utilizes three cells which contain seven control switches, three power diodes, a DC voltage source, and three floating capacitors to generate 9-level (S-MLI), 15-level, and 17-level (A-MLI) output. In the proposed topology by increasing the number of cells more output voltage levels can be generated in proposition to $2n+3$ for symmetrical multilevel inverter (S-MLI) and maximum $2^{(N+1)}+1$ for asymmetrical multilevel inverter (A-MLI), where N is the number of connected cells. Compared to the conventional and recently proposed MLI topologies it requires only a single DC source and fewer components. The proposed configuration has been analyzed symmetrically and asymmetrically and compared with conventional MLI topologies and some recently proposed topologies based on parameters like a variety of DC sources and the number of semiconductor switches. The proposed modified MLI topology can work as single and multiphase converters.

In the following section, the theoretical background will be introduced with a circuit description. The working principle of the proposed topology including different modulation techniques and mathematical analysis is discussed. Simulation models and their results for 9-level symmetrical MLI, 15-level, and 17-level asymmetrical MLI circuits are presented, as well. Section V of the article presents the hardware outcomes for the modified single-sourced multilevel inverter with 9, 15, and 17 levels. Finally, the paper ends with a short conclusion.

2. Modified multilevel inverter topology

By revisiting the conventional design, we devised a novel configuration that efficiently utilizes a single DC source while reducing the number of switches required. Our approach involves strategically reconfiguring the power circuit to optimize its performance without compromising the output quality. The proposed inverter shown in Fig. 1. is made up of two different parts, specifically the polarity changer and the level generator part. The polarity-changing part comprises an H-bridge and a DC source which provides a stepped AC voltage to the load. The level-generating part is made with several cells, which consist of a power diode, a control switch, and a floating capacitor. Several output voltage levels can be increased by different combinations of cell capacitors assumed like unary, natural number sequence, and binary.

2.1 Symmetrical configuration

In symmetric MLI all energy-storing devices such as floating capacitors are kept at the same voltage amplitude. The unary arrangement consists of all floating capacitor's voltages being kept at equal voltage, which is called symmetric arrangement as per Equation (1). By using this, a maximum number of output voltage levels generated, requirements of IGBTs, diode, and capacitors can be obtained from Equation (2)-(4) respectively, where n is the number of cells. The magnitude of the DC voltage source in a symmetrical MLI configuration can be calculated from Equation (5).

$$V_{cap.,n} = \frac{V_{dc}}{n+1} \tag{1}$$

$$N_{level} = 2n+3 \tag{2}$$

$$N_{IGBT} = n+4 \tag{3}$$

$$N_{Diode,cap.} = n \tag{4}$$

$$V_{dc} = (n+1)V_c \tag{5}$$

2.2 Asymmetrical configuration

Asymmetrical multilevel inverter configurations are an efficient methodology to make use of energy storage elements.

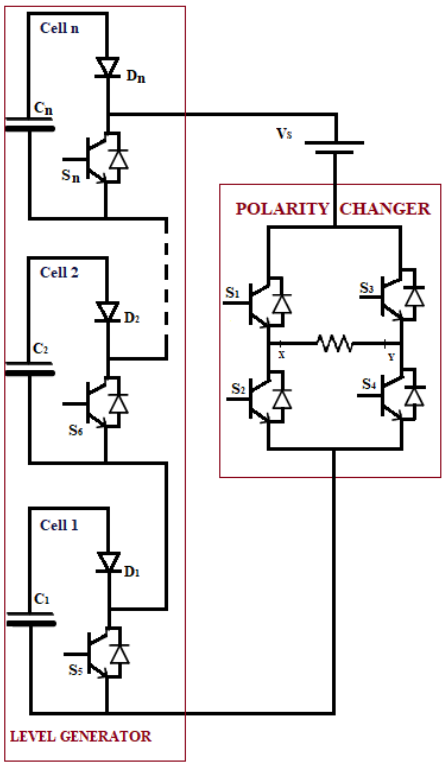

Figure 1. Circuit topology of proposed MLI.

The non-equal magnitude of capacitor voltages is utilized rather than equal in symmetric configuration. It provides more flexibility in integrating non-identical values of floating capacitors. Hence it generates higher output voltage levels with an equal number of utilized floating capacitors and control power semiconductor switches in contrast with the symmetrical approach in the same multilevel inverter configuration.

In an asymmetrical arrangement, the voltages of the floating capacitors are maintained at different levels. For the natural sequence number, the capacitor voltages are kept at an incremental number as (1:2:3:...n) and the generated output voltage levels can be derived from Equation (6). The magnitude of DC source voltage in natural sequence number-based asymmetrical MLI can be calculated from Equation (7).

$$N_{level} = n^2 + n + 3 \tag{6}$$

$$V_{dc-nat.-seq.} = (\frac{n^2+n+2}{2})V_c \tag{7}$$

In the binary configuration, the capacitor voltages are kept in a geometric progression of two as (1:2:4:....n), and the output voltage levels are generated as Equation (8). The magnitude of DC source voltage in binary geometric propagation (GP) ratio-based asymmetrical MLI can be calculated from Equation (9).

$$N_{level} = 2^{(n+1)} + 1 \tag{8}$$

$$V_{dc-binary} = 2^n V_c \tag{9}$$

The suggested MLI configuration allows us to calculate the highest achievable output voltage and peak voltage using Equations (10) and (11) correspondingly.

$$V_{0-max} = V_{dc} - (D_1 V_{c1} + D_2 V_{c2} + ... + D_n V_{cn}) \tag{10}$$

$$V_{peak-V} = V_{dc} \tag{11}$$

Table 1 presents the various combinations of switching employed in the suggested 3-cell MLI, along with their respective output voltage levels. From that, for 3 cells proposed MLI topology with unary configuration can generate a maximum nine-level output voltage, natural sequence number configuration can generate fifteen levels, and binary configuration can generate a maximum seventeen-level output voltage. The highest number of output voltage levels can be generated by binary configuration and hence it has having least voltage total harmonic distortion (THD). Unary and natural sequence number configurations have several redundant switching states as compared to binary configurations. The redundant switching states are mostly used

Table 1. Switching states of symmetrical and asymmetrical 3-cell MLI configuration.

V_{level}	**Symmetrical**	**Asymmetrical**	
	Unary	**Natural sequence number**	**Binary**
0	S_i S_{iii} S_v S_{vi} S_{vii}	S_i S_{iii} S_v S_{vi} S_{vii}	S_i S_{iii} S_v S_{vi} S_{vii}
	S_{ii} S_{iv} S_v S_{vi} S_{vii}	S_{ii} S_{iv} S_v S_{vi} S_{vii}	S_{ii} S_{iv} S_v S_{vi} S_{vii}
V_c	S_i S_{iv}	S_i S_{iv}	S_i S_{iv}
$2\,V_c$	S_i S_{iv} S_v	S_i S_{iv} S_v	S_i S_{iv} S_v
	S_i S_{iv} S_{vi}		
	S_i S_{iv} S_{vii}		
$3\,V_c$	S_i S_{iv} S_v S_{vi}	S_i S_{iv} S_{vi}	S_i S_{iv} S_{vi}
	S_i S_{iv} S_v S_{vii}		
	S_i S_{iv} S_{vi} S_{vii}		
$4\,V_c$	S_i S_{iv} S_v S_{vi} S_{vii}	S_i S_{iv} S_{vii}	S_i S_{iv} S_v S_{vi}
		S_i S_{iv} S_v S_{vi}	
$5\,V_c$	-	S_i S_{iv} S_v S_{vii}	S_i S_{iv} S_{vii}
$6\,V_c$	-	S_i S_{iv} S_{vi} S_{vii}	S_i S_{iv} S_v S_{vii}
$7\,V_c$	-	S_i S_{iv} S_v S_{vi} S_{vii}	S_i S_{iv} S_{vi} S_{vii}
$8\,V_c$	-	-	S_i S_{iv} S_v S_{vi} S_{vii}
$-V_c$	S_{ii} S_{iii}	S_{ii} S_{iii}	S_{ii} S_{iii}
$-2\,V_c$	S_{ii} S_{iii} S_v	S_{ii} S_{iii} S_v	S_{ii} S_{iii} S_v
	S_{ii} S_{iii} S_{vi}		
	S_{ii} S_{iii} S_{vii}		
$-3\,V_c$	S_{ii} S_{iii} S_v S_{vi}	S_{ii} S_{iii} S_{vi}	S_{ii} S_{iii} S_{vi}
	S_{ii} S_{iii} S_v S_{vii}		
	S_{ii} S_{iii} S_{vi} S_{vii}		
$-4\,V_c$	S_{ii} S_{iii} S_v S_{vi} S_{vii}	S_{ii} S_{iii} S_{vii}	S_{ii} S_{iii} S_v S_{vi}
		S_{ii} S_{iii} S_v S_{vi}	
$-5\,V_c$	-	S_{ii} S_{iii} S_v S_{vii}	S_{ii} S_{iii} S_{vii}
$-6\,V_c$	-	S_{ii} S_{iii} S_{vi} S_{vii}	S_{ii} S_{iii} S_v S_{vii}
$-7\,V_c$	-	S_{ii} S_{iii} S_v S_{vi} S_{vii}	S_{ii} S_{iii} S_{vi} S_{vii}
$-8\,V_c$	-	-	S_{ii} S_{iii} S_v S_{vi} S_{vii}

to attain equal power loss distribution between switching devices. Unary configuration can generate the least number of voltage levels among three different configurations but it possesses the advantage of modularity. All three configurations have their advantages and disadvantageous compared to each other and they can be used as per the requirement of the system. The modulation technique, simulation, and hardware results of the proposed modified multilevel inverter topology are discussed in the following.

3. Switching strategy

The suggested MLI configuration can function effectively at both the fundamental frequency and the elevated pulse-width modulation (PWM) switching frequency [26, 27]. There will be higher switching losses may occur when MLI operates at a higher switching frequency hence fundamental switching schemes are mostly used in MLI having higher output voltage levels. In the selective harmonic elimination (SHE-PWM) method, the offline calculations of switching angles and storing them are tiring work to use with the proposed MLI. As the number of output voltage levels increases the complexity of the space vector modulation (SVM) algorithm increases [28, 29]. Due to lesser switching losses and reduced lower-order harmonics, the nearest-level control technique is favored over SVM and SHE-PWM techniques [29, 30].

3.1 Nearest level control (NLC)

The main principle of NLC is to select a nearby level by comparing the reference voltage with the output voltage. The rising edge of the output voltage signal can be equally divided into two sections namely lower and upper levels and both are equal in magnitude. The NLC technique is shown in Fig. 2. for symmetrical 9-level MLI. In the case of floating numbers, a rounded function is used to select the nearest even number. In this article, NLC and sine pulse width modulation (SPWM) methods are applied to a 9-level, 15- level, and 17-level MLI. In the NLC technique, each level is switched several times in a period. Switching angles are changed at which levels can be calculated by using

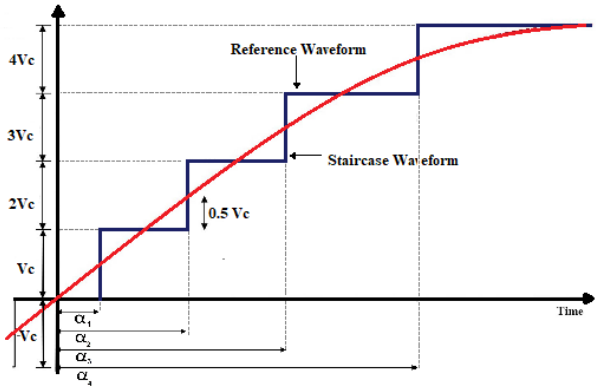

Figure 2. Basic concept of nearest level control technique for 9-level MLI

Equation (12).

$$\alpha_{i+1} = sin^{-1}\left(\frac{m_n + i}{(N-1)/2}\right) \tag{12}$$

where, i is 0, 1, 2, 3, 4,....., $(\frac{N-1}{2} - 1)$, mn is modulation index for NLC, 0<mn<1.
Different values of switching angle α can be determined by using an Equation (12). Table 2 shows the value of different switching angles for 9-level, 15-level, and 17-level output voltage. RMS Values of the MLI's output voltage can be obtained from the Equation (13).

4. Simulation models and their results

To validate the effectiveness of the proposed altered MLI structure in generating the desired output voltage, we present a Simulink model based on the recommended topology, as depicted in Fig. 1. The accompanying parameters for the Simulink model can be found in Table 3. For simulation purposes, MATLAB/Simulink software is used here in this article.

4.1 Symmetric state

The simulation model in which all the cells contain a floating capacitor with the same voltage having a unary GP

Table 2. Switching angles of symmetrical and asymmetrical 3-cell MLI configuration

For 3-cell MLI configuration	N = 9 level (Unary)	N = 15 level (Natural sequence number)	N = 17 level (Binary)
V_c	$\alpha_1 = \sin^{-1}(\frac{m_n}{4})$	$\alpha_1 = \sin^{-1}(\frac{m_n}{7})$	$\alpha_1 = \sin^{-1}(\frac{m_n}{8})$
2 V_c	$\alpha_2 = \sin^{-1}(\frac{(m_n+1)}{4})$	$\alpha_2 = \sin^{-1}(\frac{(m_n+1)}{7})$	$\alpha_2 = \sin^{-1}(\frac{(m_n+1)}{8})$
3 V_c	$\alpha_3 = \sin^{-1}(\frac{(m_n+2)}{4})$	$\alpha_3 = \sin^{-1}(\frac{(m_n+2)}{7})$	$\alpha_3 = \sin^{-1}(\frac{(m_n+2)}{8})$
4 V_c	$\alpha_4 = \sin^{-1}(\frac{(m_n+3)}{4})$	$\alpha_4 = \sin^{-1}(\frac{(m_n+3)}{7})$	$\alpha_4 = \sin^{-1}(\frac{(m_n+3)}{8})$
5 V_c	-	$\alpha_5 = \sin^{-1}(\frac{(m_n+4)}{7})$	$\alpha_5 = \sin^{-1}(\frac{(m_n+4)}{8})$
6 V_c	-	$\alpha_6 = \sin^{-1}(\frac{(m_n+5)}{7})$	$\alpha_6 = \sin^{-1}(\frac{(m_n+5)}{8})$
7 V_c	-	$\alpha_7 = \sin^{-1}(\frac{(m_n+6)}{7})$	$\alpha_7 = \sin^{-1}(\frac{(m_n+6)}{8})$
8 V_c	-	-	$\alpha_8 = \sin^{-1}(\frac{(m_n+7)}{8})$

Table 3. Simulation Parameters of A-MMC

Parameters	**Description**		
Number of DC sources	1		
Number of floating capacitors	3		
Modulation technique	Nearest level control (NLC)		
Output frequency	50 Hz		
Number of control switches	7 IGBTs		
R-L load values	100 Ω, 1 mH.		
Number of output voltage levels	**Unary**	**Natural seq. No.**	**Binary**
	9	15	17
	V_{dc}= 80 V	V_{dc}= 70 V	V_{dc}= 80 V
Ratings of floating capacitors voltage (V)	V_{ci}= 20	V_{ci}= 10	V_{ci}= 10
	V_{cii}= 20	V_{cii}= 20	V_{cii}= 20
	V_{ciii}= 20	V_{ciii}= 30	V_{ciii}= 40

ratio is called a symmetrical multilevel inverter. Each floating capacitor is charged up to a 20 V. H-bridge and three cells are taken here in a Simulink model which can generate a maximum 9-level output voltage in a phase. Table 2 illustrates the ON switching states corresponding to the various voltage levels of a 9-level inverter. Table 3 shows the simulation parameters which are used to simulate the MLI circuits to check their performance. Fig. 3. illustrates the output voltage of the 9-level inverter at various modulation indexes, along with its harmonic spectrum. Additionally, it showcases the output current and its corresponding total harmonic distortion (THD). The responses of the 9-level inverter are presented in subfigures (a) to (e). A proposed MLI topology can generate stepped 9-level output voltage (V_{out}) shown in Fig. 3. (a). V_{out} has a step equal to 20 V, first, second, and third level each while the peak voltage is equal to the source voltage which is 80 V and 0 V level at the end of the positive half-cycle. The same amplitude but with reverse polarity is obtained in the negative half-cycle. The harmonic profile shown in Fig. 3 (b) explains the advan-

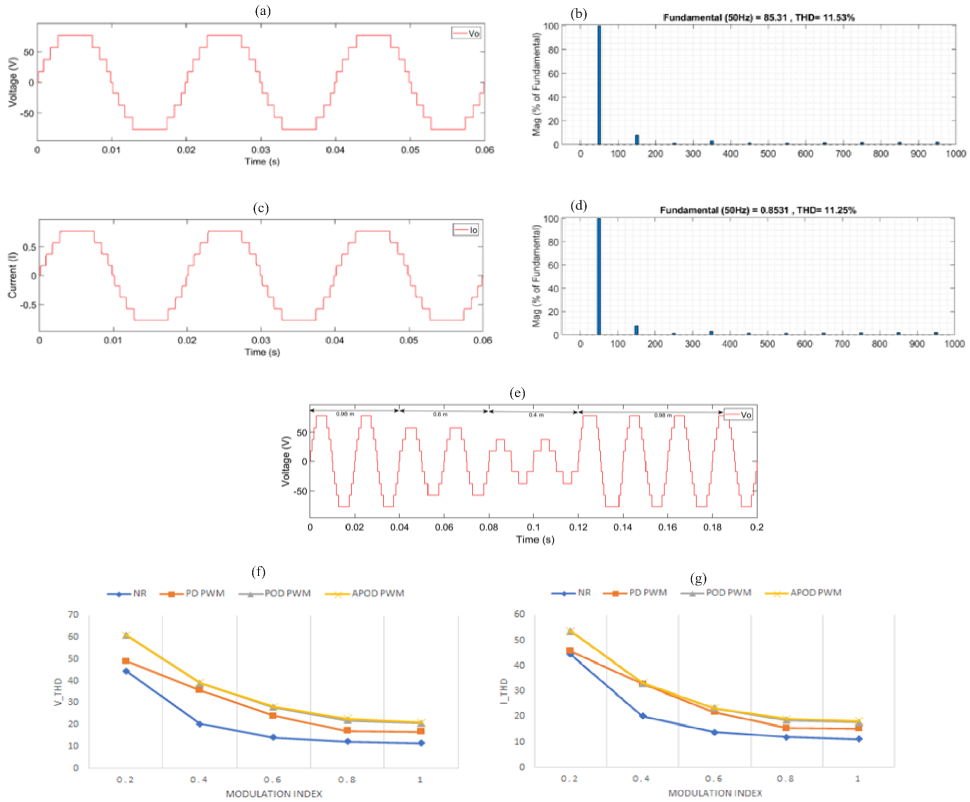

Figure 3. Simulation results of 9-level inverter with unary GP ratio (a) 9-level output voltage, (b) output voltage THD, (c) output current, (d) output current THD, (e) 9-level inverter response at different modulation index, (f) V_{THD} with various modulation techniques, (g) I_{THD} with various modulation techniques

tages of the proposed modified MLI topology which results in a lesser THD of 11.53% in contrast with conventional two-level inverter topologies.

Also, performance analysis of a 9-level inverter with different modulation techniques like nearest level control (NR), phase displacement (PD), phase opposite displacement (POD), alternate phase opposition displacement (APOD) based on V_{THD} and I_{THD} with various modulation indexes are presented with graph (f)-(g). From those graphs, it is said that the 9-level inverter performs efficiently with the nearest-level technique and, also THD is reduced with the increment in modulation index.

$$V_{rms} = \frac{2}{\pi} \times \sqrt{\left[\sum_{i=1}^{\frac{N-3}{2}} \{(\alpha_{i+1} - \alpha_i) i.V_c\}^2\right] + .. + \{(\frac{\pi}{2} - \alpha_N)\frac{N-1}{2} V_c\}^2} \quad (13)$$

4.2 Asymmetric state

In an asymmetrical arrangement, the voltages of the floating capacitors are maintained at different levels. For the natural sequence number, the cell capacitor voltages are kept at the incremental number as per Table 3. The same structure with a natural sequence number configuration can generate a maximum 15-level output voltage in phase. Table 3 states the Simulink model parameters and based on that Fig. 4 (a)-(d) shows both outputs current I_{out} and voltage V_{out} with their respective harmonic spectrum. The newly proposed configuration of the MLI offers a remarkable feature of generating a 15-level voltage output in each phase, while simultaneously minimizing the need for numerous components. Impressively, the 15-level output voltage exhibits an exceptionally low level of total harmonic distortion (THD), reaching as low as a mere 7%. The proposed modified MLI topology is effective in obtaining lower THD levels of output currents and voltages which can be obtained from Fig. 4. The simulation findings demonstrate the output voltage of the single-phase fifteen-level inverter under various modulation indexes (1.0, 0.6, and 0.4), as illustrated in Fig. 4 (e). Fig. 4 clearly shows that the output phase voltage of the multilevel inverter (MLI) is inherently balanced, with a 15-level output voltage characterized by 10 V increments at $m_i = 1$. Nearest-level control techniques are best suited for fifteen-level inverters as per Fig. 4 (f)-(g), which shows the values of V_{THD} and I_{THD} with various modulation techniques.

Using a binary GP ratio between the cell capacitor voltages of the proposed modified MLI can generate a maximum of 17-level output voltage. Table 3 states the system parameters and based on that Fig. 5 (a)-(d) shows both outputs current I_{out} and voltage V_{out} with their respective harmonic spectrum. The simulation results of the output voltage for the proposed modified single-phase 17-level MLI are con-

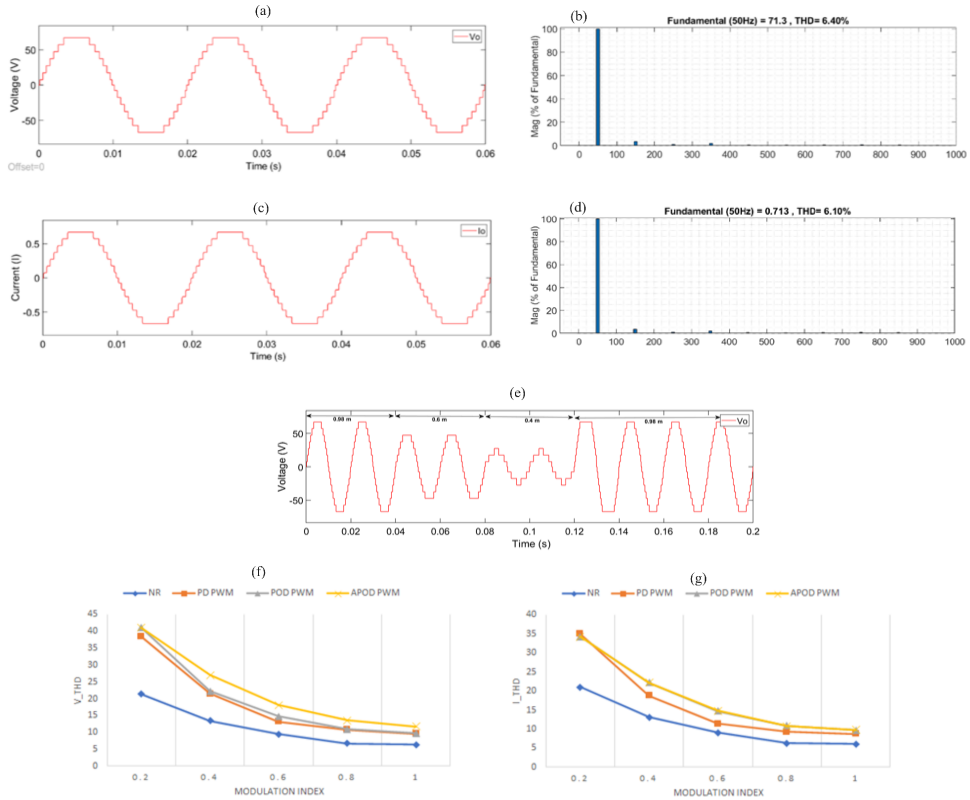

Figure 4. Simulation results of 15-level inverter with unary GP ratio (a) 15-level output voltage, (b) output voltage THD, (c) output current, (d) output current THD, (e) 15-level inverter response at different modulation index, (f) V_{THD} with various modulation techniques, (g) I_{THD} with various modulation techniques.

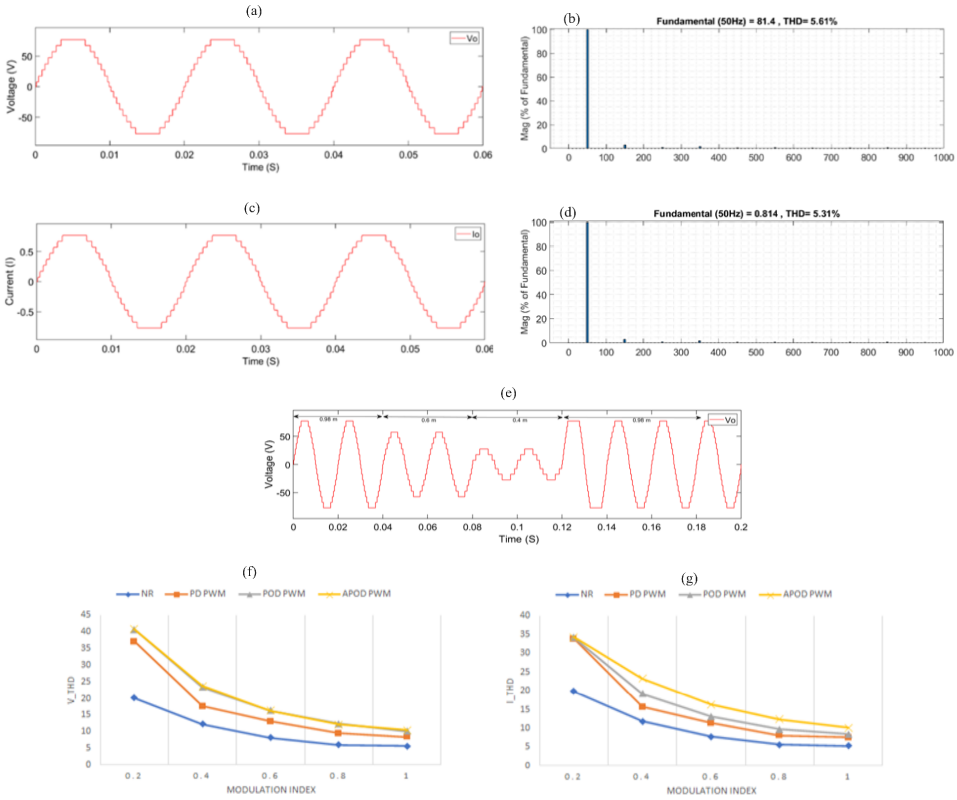

Figure 5. Simulation results of 17-level inverter with binary GP ratio (a) 17-level output voltage, (b) output voltage THD, (c) output current, (d) output current THD, (e) 17-level inverter response at different modulation index, (f) V_{THD} with various modulation techniques, (g) I_{THD} with various modulation techniques.

ducted with different modulation indexes (0.4, 0.6, and 1.0) as depicted in Fig. 5 (e). Performance analysis of a 17-level MLI with different modulation techniques is shown in Figure 5 (f)-(g). It is clear from the above-depicted figures that as the modulation index increases the THD decreases and power quality improves. So it is advisable to use the proposed modified MLI topology on a high modulation index to obtain its superior performance.

By utilizing the same number of cells having symmetrical and asymmetrical GP ratios, binary GP ratio-based MLI topology has advantages over unary and natural sequence number-based topology in terms of V_{THD} and I_{THD} as per Fig. 6 (a) and (b). Moreover, the suggested MLI topology based on binary GP ratios necessitates fewer control switches and capacitors compared to the unary GP ratio-based topology when the number of output voltage levels rises. This is evident in Fig. 6 (c) and (d), respectively.

5. Hardware results

The experimental hardware model of the proposed 9-level, 15-level, and 17-level modified MLI has been developed to ensure its practicability and for validation of the concept. To generate the gating signals DSP controller TMS320F28379D has been used. To supply DC input power for 9-level, 15-level, and 17-level MLI, a regulated power supply of 80 V for unary and binary GP-based MLI while 70 V for natural sequence-based MLI is used. The hardware parameter for the proposed modified MLI topology is given in Table 4. An oscilloscope is used to record and measure all the waveforms of MLI. Fig. 7. illustrates the obtained outcomes from the hardware model of the proposed modified multilevel inverter for three different levels: 9-level, 15-level, and 17-level. In Figure 7 (b), the waveform of the output voltage for the 9-level inverter is displayed. Similarly, Fig. 7 (c). presents the output voltage waveform for the 15-level inverter. Moreover, the voltage waveform of the 17-level inverter in the proposed asymmetrical MLI topology is depicted in Fig. 7 (d). The hardware model is comprised of various equipment such as a four-channel oscilloscope, DC source, floating capacitors, workstation, discrete IGBTs, their drivers, and protection circuits.

A brief comparison is discussed here to match the proposed modified MLI topology among developed single-source DC-based topologies. It is important to emphasize the advantages of the proposed modified MLI topology in comparison to the recently developed MLI topologies. A typical comparison of MLI topologies based on a 9-level output voltage versus some floating capacitors and a number of control switches N_{Sw} is discussed [31–34]. This is based on the fact that control switches and isolated DC sources determine the overall size of the system, cost, and feasibility in a particular application. A quantitative comparison concerning N_{Sw} (number of control switches), N_{Diode} (number of power diodes), N_{cap} (number of floating capacitors),

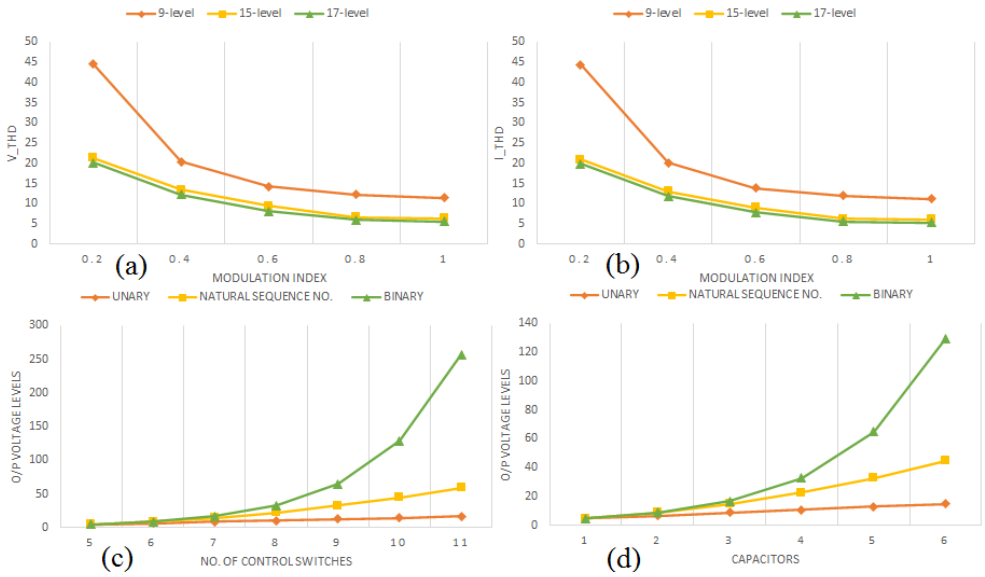

Figure 6. Comparison of a unary, natural sequence number and binary GP ratio based 3-cell configuration (a) V_{THD} with various modulation index (b) I_{THD} with various modulation index (c) Requirement of control switches (d) Req. of capacitors.

Table 4. Hardware Parameters of A-MMC.

Parameters	**Description**		
DC sources	V_{dc} = 80 V (unary and binary) V_{dc} = 70 V (Natural seq. number)		
DSP controller	TMS320F28379D-DSP		
Output frequency	50 Hz		
Number of control switches	7 IGBTs, KGT15N120NDS224, 1200 V, 30 A		
Number of power diodes	3, 1N4007 1000 V, 1 A.		
R load values	100 Ω		
Number of output voltage levels	**Unary**	**Natural seq. No.**	**Binary**
	9	15	17
Ratings of floating capacitors voltage (V)	V_{ci}= 20	V_{ci}= 10	V_{ci}= 10
	V_{cii}= 20	V_{cii}= 20	V_{cii}= 20
	V_{ciii}= 20	V_{ciii}= 30	V_{ciii}= 40

Table 5. Comparison between recently proposed 9-level single-sourced topologies and proposed modified MLI topology.

Topology	**NPC**	**FC**	[31]	[32]	[33]	[34]	**Proposed topology (Symmetrical)**	**Proposed topology (Asymmetrical)**
N_{Sw}	16	16	17	10	8	8	7	6
N_{Dd}	14	0	4	0	0	0	3	2
N_C	8	8	4	3	1	2	3	2
N_{Driver}	16	16	17	10	8	8	7	6
N_T	54	40	42	23	17	18	20	16

N_{Sw}, N_{Diode}, N_C, N_{Driver}, and N_T : indicate the number of switches, discrete diodes, capacitors, drivers and total components respectively.

N_{Driver} (number of drivers), and N_T (Total number of components) is made between single-sourced conventional and recently developed topologies. The presented modified single DC sourced asymmetrical multilevel inverter exhibits remarkable improvements over conventional and newly developed MLIs. Through comprehensive simulations and comparative analyses, we observed a significant reduction in the switch count, resulting in enhanced cost-effectiveness and reliability. Moreover, the proposed design maintains excellent output waveform quality and achieves higher efficiency levels than its counterparts. The lower requirement of power semiconductor switches and floating capacitors indicates that the proposed modified MLI topology can be a good alternative to MLIs enlisted in Table 5 for several

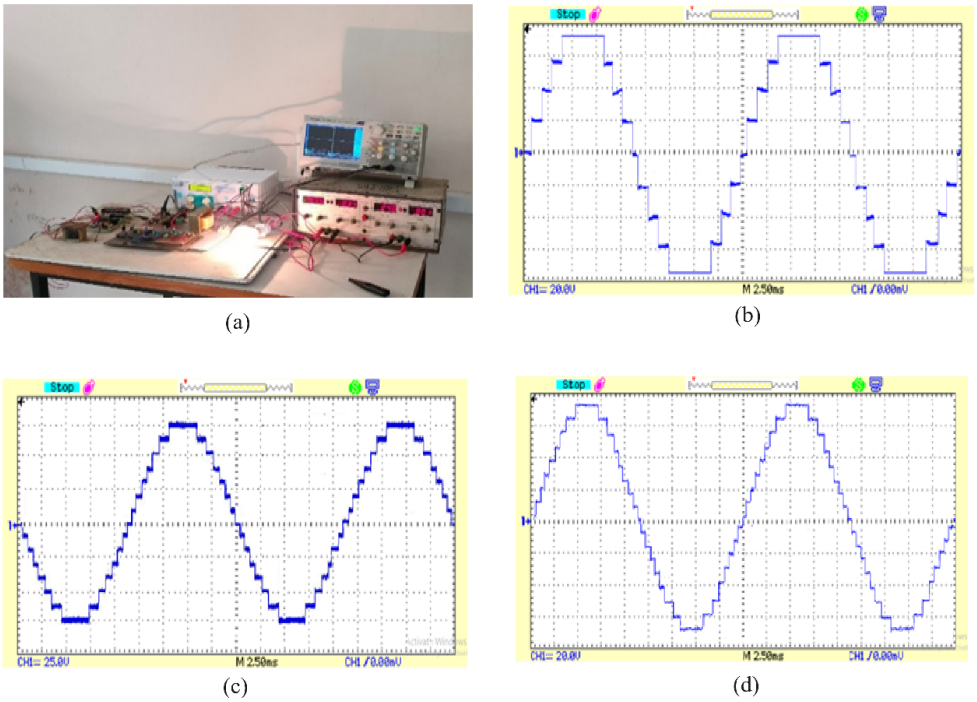

Figure 7. Experimental set-up and its results of proposed topology (a) Experimental set-up (b) 9-level V_{OUT} (c) 15-level V_{OUT} (d) 17-level V_{OUT}.

applications. Though it has many advantages it requires capacitor voltage balancing circuits with each cell which increases its complexity Also these configurations require switches with a high voltage stress value because of high total standing voltage (TSV). A The proposed modified MLI finds its applications in a low-power system where small size, low cost, and high performance are most appreciated.

6. Conclusion

This paper presents a modified MLI topology with concern to single DC sourced and lower switch count. The proposed modified MLI topology has been discussed briefly with a basic unit of a 3-cell series connection with an H-bridge configuration generating 9 levels with unary GP ratio, 15 levels with natural sequence number-based GP ratio, and 17 levels with binary GP ratio. A comparative analysis of the proposed modified MLI topology and recently reported topologies for 9-level configuration has been carried out with three cells and three capacitors with a single voltage source. To check the dynamic performance of the proposed modified MLI topology a Simulink model has been developed having dynamic modulation indexes in the laboratory a prototype model of the proposed MLI is developed, to validate different hardware results with the simulation results considering different modulation indexes. Finally, the experimental results prove the workability and suitability of the proposed modified MLI topology in low-power applications. In summary, our research introduces a pioneering modification to the asymmetrical multilevel inverter field. The modified single DC-sourced MLI design effectively reduces the switch count, leading to improved performance, cost-effectiveness, and reliability. This innovation has the potential to revolutionize the development of asymmetrical MLIs, making them more accessible and efficient in various applications ranging from renewable energy systems to electric vehicles.

Authors Contributions
All the authors have participated sufficiently in the intellectual content, conception and design of this work or the analysis and interpretation of the data (when applicable), as well as the writing of the manuscript.

Availability of data and materials
Data presented in the manuscript are available via request.

Conflict of Interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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