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High-Speed Current-Mode Full-Adder with Carbon Nanotube Technology

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ABSTRACT:
The relationship between the amount of energy consumption and the circuit speed to change the design efficiency is an important challenge in designing digital circuits. Adders are essential components of computing circuits that play an important role in computing speed. This article proposed a new design for a single-bit current mode full adder using the field effect transistors based on carbon nanotubes to enhance the speed and reduce the occupied space on the chip. The correct combination of the majority function, the current mirror technique, and the sum value on carry reduced the delay of all adder circuits. The simulations have been done by HSPICE software and based on the provided standard model of 32 nm with CNTFET technology. The proposed design has improved by 55% in terms of delay. The PDP level in the proposed design has decreased by 63% compared to the previous designs.

KEYWORDS: Full adder, Current Mode, Field Effect Transistors, Carbon Nanotubes, Majority Function.

1. INTRODUCTION

The increasing use of electronic and digital devices and equipment such as mobile phones, tablets, and IOT equipment in daily life and also in most industries, including medicine, military, communication, etc., has turned man into a machine. Human life is intervened with technology such that it urgently needs powerful, efficient, and low-consumption tools. Accordingly, faster digital processors with stronger memories are needed [1]- [2]. One of the parts of the processors is the computing circuits that play an important role in the speed of the processor. Therefore, optimal design for computing operations in digital processors is very important [3]. The most important performance parameters for digital processors is speed and power consumption. Full adders are one of the components of computing circuits used in the critical path of complex mathematical circuits for multiplication and division [4]. Thus, full adders' performance can affect the entire system's performance [5]- [6]. So far, most of the digital circuit designs have been in the voltage mode platform [7]. However, this platform is not responsive to the increasing need to develop more advanced circuits for more accurate analysis. The method of implementing circuits in voltage mode has major problems. The connections occupy a large part of the physical area even when not used [8]- [9].

Improvements in the manufacturing process of VLSI circuits have led designers to focus on current-mode circuits to implement basic and important circuits such as adders. Working in the current-mode platform has many advantages, which have made the designs in that platform simpler, less consuming, and more efficient [10]. In the current mode, if two wires containing two different currents are short-circuited, the output will be the algebraic sum of the two currents. This is the basis of the operation of current mode circuits and the main advantage of current mode over voltage mode. Also, the use of the current mode has features such as reducing the complexity of circuit wiring by placing several

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logical levels in one wire using the implementation of many-valued logic [11]- [12].

In addition, the current direction to show the sign and using the algebraic sum of the values by connecting the wires are other properties that can be used in the current mode. Circuits processed in current mode are more significant than circuits in voltage mode because of lower power consumption, higher linearity, fewer constituent elements, larger dynamic range, and higher bandwidth [13].

On the other hand, CMOS has been the main technology in the last decades in the design of VLSI circuits and has satisfactorily played a role in the process of shrinking transistors to achieve energy efficiency and speed [7].
This process continued until the reduction of the size of CMOS transistors in the nanometer size created challenges that reduced gate control. These problems became a barrier to shrinking dimensions in CMOS technology and subsequently reduced speed and energy efficiency in various applications, in high density [13]; [14]- [15]. The main limitation of CMOS technology and the expectations that researchers had from Moore's law, led them to replace this technology.
Researchers tried to have a serious approach towards nanotechnologies such as single electron transistors (SET) [16]-[17], carbon nanotubes (CNTFET) [18], and quantum dot cell atoms (QCA) [19] to overcome the limitations mentioned above. The mentioned items have been introduced as possible successors of CMOS.

Meanwhile, the similarity between traditional MOSFET infrastructure and CNTFET introduced CNTFET as a suitable alternative to CMOS without tough challenges [20]. CNTFET operates at a very high speed. CNTFET has significantly better efficiency due to higher efficiency than CMOS, higher carrier speed, and lower power consumption. Capabilities such as greater mobility to change carriers, less sub-threshold oscillation, and fewer interference components are among its outstanding features [21].

Theoretically, a carbon nanotube (CNT) is defined as a folded sheet of carbon called graphite. CNT is a sheet of a graphite layer with a thickness of one atom, rolled as a cylinder [22]. CNTs are classified into two groups based on the number of internal tubes: single-walled CNTs (SWCNTs) and multi-walled CNTs (MWCNTs) [18]-[23].
Single-walled CNTs are formed by rolling a graphene sheet to create a cylindrical wall. However, multi-walled CNTs have several single-walled cylinders placed inside each other [24] (Fig. 1.)

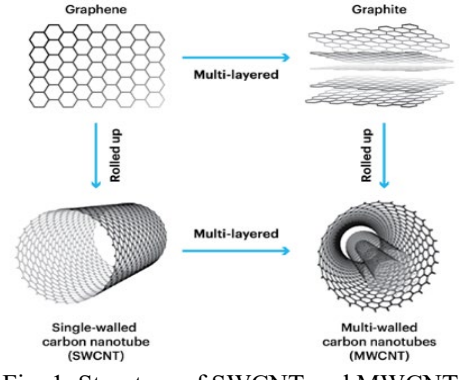

Fig. 1. Structure of SWCNT and MWCNT

SWCNTs have better electrical conductivity and are more transparent than MWCNTs. However, the production and purification of SWCNT are more difficult than MWCNT. Also, SWCNTs have very high mechanical resistance because, in SWCNTs, carbon-carbon atoms are connected by sigma (σ) bonds, which are the strongest [23]-[25]. CNFETs use single-wall semiconducting carbon nanotubes (SWCNT) as their channel. SWCNT can act as a conductor or a semiconductor depending on the angle of arrangement of atoms along the CNT. This property is characterized by two parameters (n_1, n_2). They are non-negative integers representing a vector (chirality vector) that determines how to transform a flat sheet into a nanotube [26].

If $n_1 - n_2 = 3i$, $i \in Z$, the nanotube is metallic; otherwise, CNT is a semiconductor. The diameter of CNTs (DCNT) can be calculated using equation (1). The value of a = 0.142 nm is the distance between two neighboring carbon atoms [24].

$$D_{cnt} = \frac{a\times\sqrt{n_1^2+n_2^2+n_1n_2}}{\pi} \quad (1)$$

The threshold voltage Vth is inversely dependent on the CNTD equation (2). Thus, changing the nanotube diameter results in different transistors with different turn-on voltages. This feature can be used in easier design and improve complex circuit performance [27].

$$V_{th} = \frac{0.42}{D_{CNT(nm)}} \quad (2)$$

Fig. 2 shows the structure of a CNTFET. The main parameters in this structure are as follows.

DCNT: The diameter of CNT
Tube: The number of CNTs under the Gate terminal
Pitch: The distance between the centers of two neighboring CNTs
Lg: Physical channel length, the undoped region
Lss: The length of the doped CNT source-side extension region
Ldd: The length of the doped CNT drain-side extension region

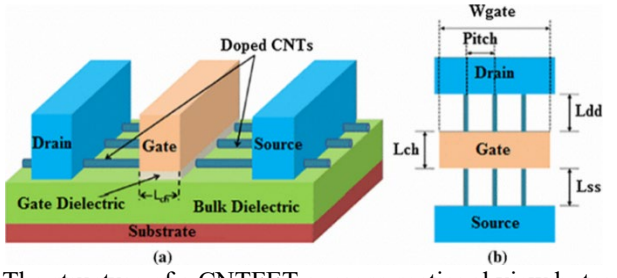

Fig. 2. The structure of a CNTFET a: cross-sectional view b: top view.

During these years, several designs of full adders using CNTFETs have become popular. Most of them had a significant speed improvement compared to CMOS designs. In this regard, the challenge of reducing the scales has been solved to a large extent. Improving the speed of the full adder has a significant effect on the speed of microprocessors and processors that solve complex algorithms using computing circuits. In general, these improvements had several main motivations: reducing power consumption, reducing the number of transistors, and increasing speed.
Usually, the efficiency of integrated circuits is influenced by how to perform calculation operations that the designer implements and uses in combination.

This article presents a full adder design using CNTFET technology and in the current mode platform. It increases speed and improves the PDP of the circuit by using the majority function technique and current mirror. The use of the majority function, the non-dependence of the sum value on the carry, also simplifies the sum operation reduces the delay, and improves the circuit performance. Next, in section 2, there is an overview of some full-adder designs presented in recent years. Section 3 provides the proposed idea. In section 4, the implementation results are provided, and section 5 is the conclusion.

2. REVIEW OF LITERATURE

Since the full adder cell is one of the main components of computing circuits, various designs have been presented based on needs and applications. Each of them has its characteristics and disadvantages.
The review and analysis of the full adder circuits presented allow the designing of newer circuits that eliminate the weaknesses of the existing circuits as much as possible and improve the strengths by knowing the strengths and weaknesses of each of them.

First, a circuit called the new current mode adder based on the majority function is shown in Fig. 3 [28].
This design generates the carry using the majority function (Equation (3-5)). The majority function simplifies the circuit and reduces the delay and power consumption in the circuit. On the other hand, the circuit delay increases due to the dependence of the sum value on the carry.

$$C'_{out} = \text{Majority}(A.B.C_{in}) \quad (3)$$

Also, the total value is made through the majority function (Equation (4)).

$$\text{Sum}' = \text{Majority}(A.B.C_{in}.C'_{out}.C'_{out}) \quad (4)$$

The truth table (1) proves the statement of this problem.

Table 1. The truth Table (1) majority function adder

A	B	Cin	Cout'	Majority(A,B, Cin, Cout', Cout')	SUM
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	1	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	1	1

This circuit has two major problems. First, the construction of the sum value requires the generation of a carry, which increases the delay in the circuit. Second, the sum value and carry are produced in reverse, and they must be reversed by an inverter to be applicable, increasing the circuit's size and power consumption.

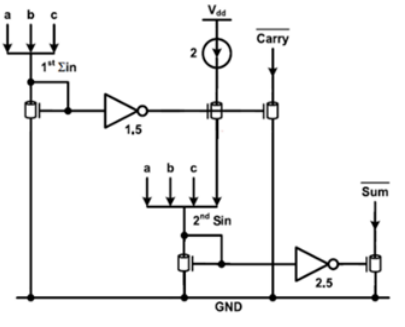

Fig. 3. New current mode adder based on the majority function

The second circuit called the six-transistor adder, is shown in Fig. 4 [29]. The proposed design uses only 6 transistors. This adder consists of a PMOS transistor as a current source, an inverter as a detector, and a current mirror. In this circuit, the value of the carry is generated as in the previous design with the majority function (Equation 3).

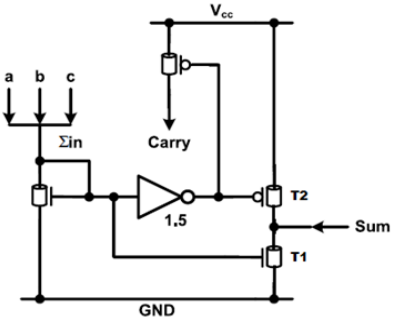

Fig. 4. Six- transistor adder

The total value is calculated from equation (5).

$$\text{Sum} = I_{DS}(T_2) - I_{DC}(T_1) = 2 \times \frac{\sum \text{in}}{2} - \sum \text{in} \qquad (5)$$

Transistor T_1 makes an identical copy of Σin. The dimensions of T_2 are adjusted in such a way that when it turns on, it produces two units of current. Kirchhoff's current law is used at the junction of two transistors T1 and T_2, and the current difference between the two transistors makes the total value. The truth Table (2) shows the truth of this problem. The delay of this design is high because of the dependence of the sum on the carry.

Table 2. The truth table (2) six- transistor adder.

∑in	TD (1.5)	I (T_2)	I (T_1)	Sum
0	1	0	0	0
1	1	0	1	1
2	0	2	2	0
3	0	2	3	1

The circuit named efficient adder is shown in Fig. 5 [6]. As its truth table (3) shows, the value of the carry is produced by the majority function (Equation (3)). NAND values and the three inputs (NOR a, b, c) and their carry's value are calculated to make the sum value. Finally, the sum is generated using the output minority function (equation (6)). The delay of the circuit is high due to the dependence of the sum value on the carry and the simultaneous use of minority and majority functions.

$$Sum = Mino[NAND(a.b.c).NOR(a.b.c).Cout] \qquad (6)$$

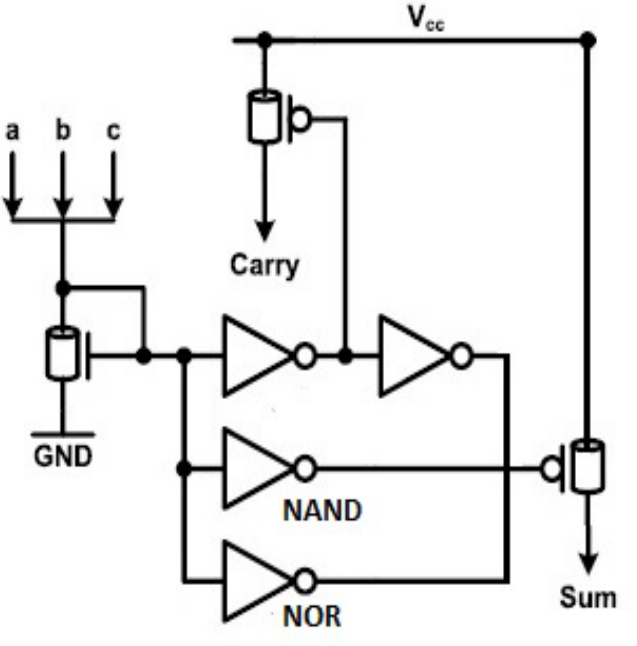

Fig. 5. The efficient adder circuit.

Table 3. The majority and minority function adder.

Input			Output				
A	B	C	Nand(A,B,C)	Nor(A,B,C)	Majority(A,B,C)	Majority(Nand(A,B,c),Nor (A,B,C),Majority(A,B,C))	SUM
0	0	0	1	1	0	1	0
0	0	1	1	0	0	0	1
0	1	0	1	0	0	0	1
0	1	1	1	0	1	1	0
1	0	0	1	0	0	0	1
1	0	1	1	0	1	1	0
1	1	0	1	0	1	1	0
1	1	1	0	0	1	0	1

The fourth and fifth designs presented by Ms. Moradi in 2016 can be seen in Fig. 6 [10].

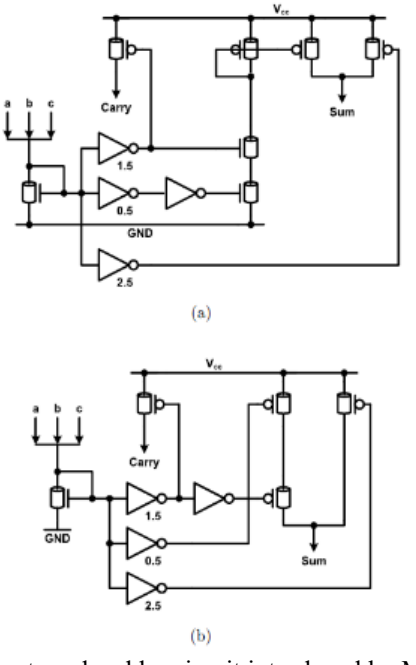

Fig. 6. Current mode adder circuit introduced by Mrs. Moradi.

Both circuits have the same function. The carry is produced by the majority function in them. Each has three inverters with different excitation thresholds (0.5, 1.5, and 2.5) to specify Σin=0 to Σin=1, Σin=1 to Σin=2, and Σin=2 to Σin=3. In both designs, transistor T1 turns on when Σin=>1. On the contrary, the transistor T2 turns on when Σin=<1. Therefore, if they are put in series, they will pass the current when Σin=1 (Equation (7)). Transistor T3 is in another parallel path. If Σin > 2.5, it directs the current to the output. The difference between the two schemes is that the first scheme copies the output current from an intermediate path to the output, while the second scheme directly generates the output current without copying. Therefore, the second plan has a lower delay, power consumption, and circuit level.
The delay in this design is high due to the complexity and the increased circuit layers.

$$\text{Sum} = \sum in \times [1-(\sum in)/2\ ] + [(\sum in)/3] \quad (7)$$

The last circuit, called the new current mode adder, can be seen in Fig. 7 [9]. This adder calculates the carry by ultra-low consumption ULPD diode and voltage mirror.

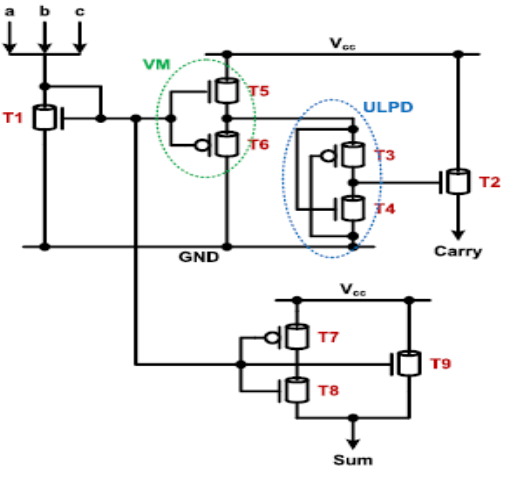

Fig. 7. New current mode adder circuit.

Table 4 shows how to generate the value of the carry and the sum value.

Table 4. Production of the output of the carry and sum based on different input values

∑in	I(∑in)	V(∑in)	Diode	T2	Carry	T7	T8	T9	SUM
0	0xI	0V	OFF	OFF	0	ON	OFF	OFF	0
1	1xI	1/3Vcc	OFF	OFF	0	ON	ON	OFF	1
2	2xI	2/3Vcc	ON	ON	1	OFF	ON	OFF	0
3	3xI	Vcc	ON	ON	1	OFF	ON	ON	1

It converts the sum of input currents to voltage. However, neither inverters nor current sources are used to detect thresholds. Instead, a diode is utilized to regulate voltage upon a specific threshold. A diode is a two-terminal device, which allows current to flow from its positive pole (anode) to its negative pole (cathode) when a special voltage is applied to its terminals in the forwarding bias. In this design, the delay value of the circuit has been improved compared to the previous designs due to the non-dependence of the sum value on the carry, and the balance between the delay and the power consumption has been established.

According to the designs presented so far, a compromise can be made between delay and power consumption, and the circuit performance can be brought to the optimum state with a good design.

3. PROPOSED DESIGN

Fig. 8 shows the implementation of the proposed circuit designed based on equations (8) and (9) and also the truth table (5). The proposed full-adder is implemented by a majority function and uses carbon nanotube technology.

$$Cary=\lfloor(\sum in)/2\rfloor=1 \quad \text{if} \quad \sum in>1.5 \qquad (8)$$

$$Sum=\sum in \times\lceil 1-(\sum in)/2\rceil+\lfloor(\sum in)/3\rfloor \qquad (9)$$

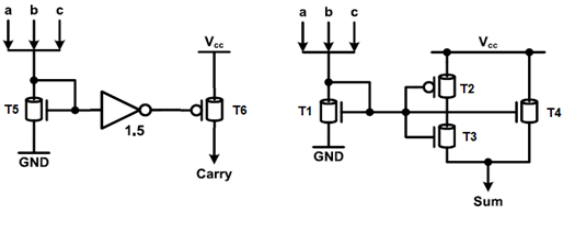

Fig. 8. The proposed adder design.

In this design, the equations are stated based on the Kirchhoff flow law, and the algebraic sum of the incoming flows governs the relations. The carry is implemented based on the majority function (equation (8).

In equation (8), if the algebraic sum of the input currents is greater than 1.5, the carry signal is generated; otherwise, the carry is zero.

The sum is implemented based on Equation (9). Transistor T3 is turned on when Σin=>1. On the contrary, transistor T2 turns on when Σin=<1. So if they are put in series, they will pass current when Σin=1. Transistor T4 is located in another parallel path, which directs the current to the output if Σin > 2.5 (Equation (9).

Table 5. Operation of the adder circuit

∑in	T2	T3	T4	Sum
0	ON	OFF	OFF	0
1	ON	ON	OFF	1
2	OFF	ON	OFF	0
3	OFF	ON	ON	1

The threshold voltage values of the transistors in Table (5) must be accurately calculated and implemented to reach the sum output.

Fig. 9 shows the accuracy of the proposed circuit and the input and output waves.

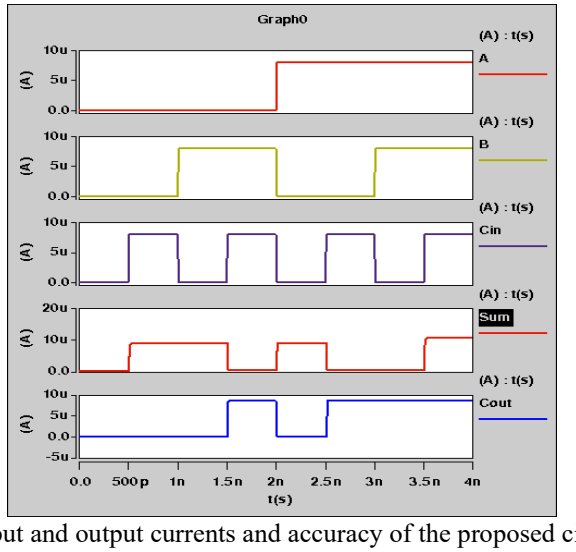

Fig. 9. Input and output currents and accuracy of the proposed circuit.

As can be seen, the output results of the designed circuit are completely SWING-FULL; that is, the output is very close to logical zero and one. Another reason for the full-swing circuit of the proposed adder circuit is the absence of elements such as capacitors, which are considered destructive elements in designs.

3.1. Simulation and Comparison

The proposed circuit and other previous designs have been simulated by Hspice software and 32 nm CNTFET technology. All circuits have been simulated in the same conditions and at a room temperature of 27°. The working frequency of 1 GHz and the supply voltage of 0.9 V have been used. Table (6) exhibits transistor sizing parameters for the proposed design.

The delay of a circuit shows how fast that circuit responds to inputs, and it represents the delay that the signal undergoes in passing through a gate. In general, the time required for the output to reach 50% of its swing when the input has reached 50% of its swing is called a delay, and the longest delay is considered a circuit delay.

A random pattern is applied to the circuit for a long time to calculate the average power consumption. The average power consumption, which is measured by the simulator, includes dynamic, static, and short-circuit power consumption. Propagation delay and power consumption of a valve are related. The propagation delay is mainly determined by the rate of energy storage in the gate capacitors. The faster this energy transfer is, the faster the valve works.

Table 6. Transistor sizing parameters for the proposed Full Adder

Transistor	L_g (nm)	L_{ss} (nm)	L_{dd} (nm)	D_{CNT} (nm)	Pitch (nm)	#Tube
T_1	152	152	152	7.047	16	2
T_2	32	32	32	2.349	12	6
T_3	32	32	32	1.096	12	4
T_4	32	32	32	0.626	18	12
T_5	32	32	32	1.252	20	3
T6	32	32	32	0.861	20	3
T7	32	32	32	1.331	20	3
T8	32	32	32	0.783	20	2

In technology with a particular topology, the product of power consumption and propagation delay is usually constant. This product, which is called a power-delay product (PDP), is a criterion for evaluating the quality of a switching device. PDP is the same energy the valve consumes in each switching time and is obtained by equation (10).

Max (Delay)×Ave (Power Consumption) (10)

The simulation results are shown in Table (6). The best result in each design is bolded.

Table 7. Comparison of the performance results of adder circuits.

Full adder	Delay ($\times 10^{-11}$ s)	Power ($\times 10^{-5}$ W)	PDP ($\times 10^{-16}$ J)	Transistors
new design	0.7366	2.2327	1.6446	8
ULPD (2021)	1.9415	2.6762	5.1957	9
Majority&Minority (2018)	2.9663	2.4986	7.4117	11
(2st Design) (2016)	2.7688	2.2375	6.1953	13
(1st Design) (2016)	2.985	2.5483	7.6067	15
six transistor (2008)	2.679	2.5031	6.7058	6
Majority function (2008)	5.8768	6.973	40.979	13

According to Table (7), the first and third designs have the highest delay in the circuit, and the reason is the dependence of the production of the sum value on the generation of the carry in the previous stage. Due to its simpler structure and independence of the sum value of the carry, the proposed design has the lowest delay (0.7366 x 11-10) compared to other designs. There is a 55% improvement in delay time in this circuit compared to the design presented in reference [9], which has the lowest delay among previous designs (Fig. 10). The power consumption of the design is 2.2327 x10-5W, which has improved by 0.3% compared to the design [10], which had the lowest power consumption among the previous designs (Fig. 11).

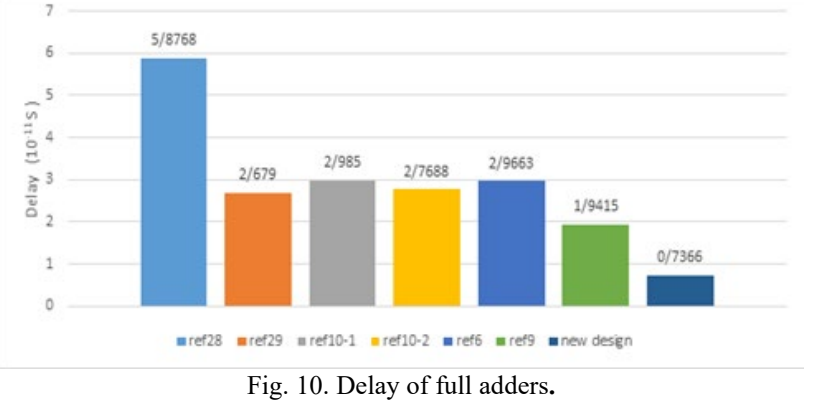

Fig. 10. Delay of full adders.

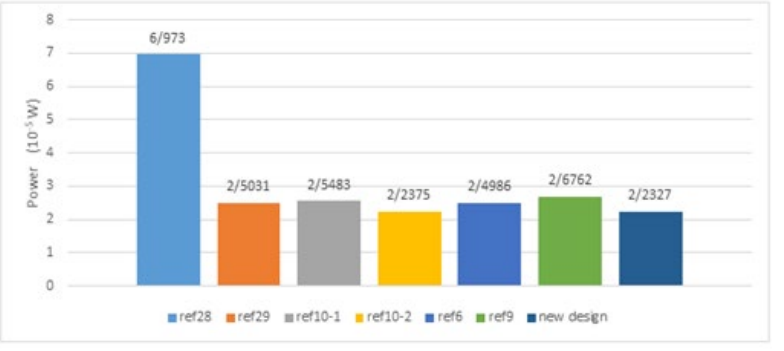

Fig. 11. Average power consumption of full adders.

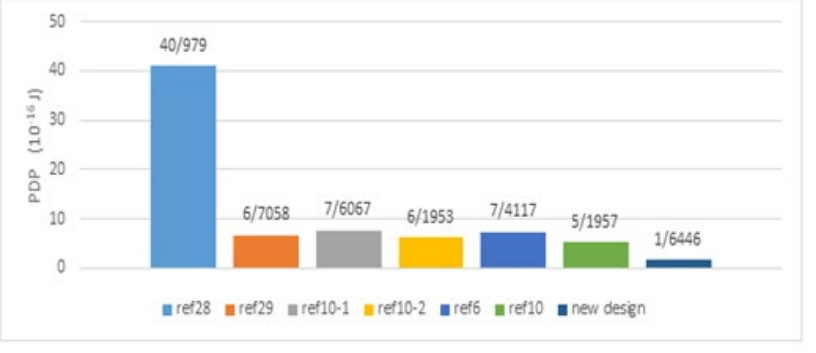

Fig. 12. PDP of full adders.

The circuit PDP, the product of the power consumption and the propagation delay, is a general criterion to evaluate the circuit performance, which has also been optimized in the proposed design.
The PDP value of the proposed design is 1.6446*10-16J. According to Fig. 13, the proposed circuit PDP has significantly decreased compared to other designs presented in the past.

Another important parameter for evaluating VLSI circuits is their sensitivity to temperature changes. The proposed design has been simulated in the temperature range of 0° to 100° to measure its sensitivity and performance to temperature changes. The simulation results are shown in Fig. (١٣), (١٤), and (١٥).

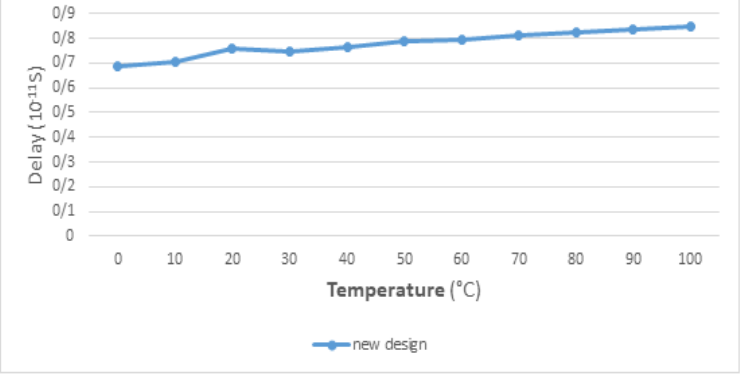

Fig. 13. Circuit delay vs. temperature changes.

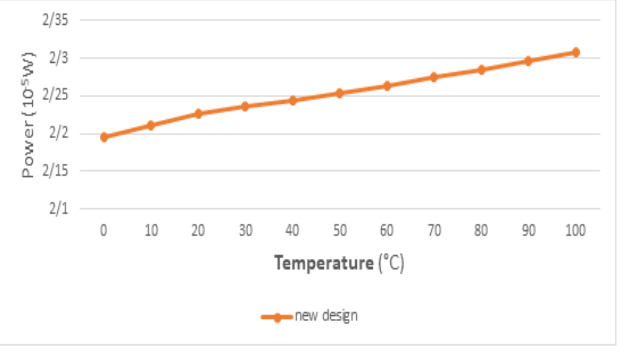

Fig. 14. Power consumption of the circuit vs. temperature changes.

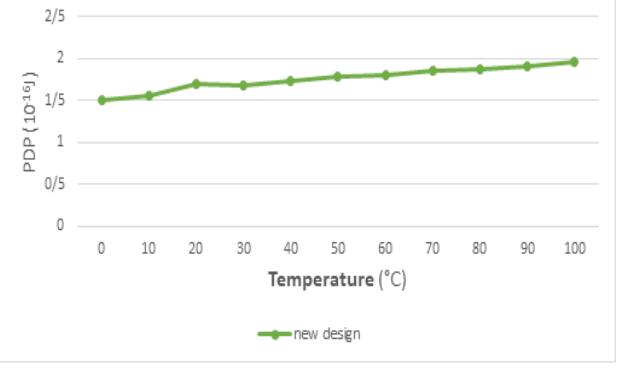

Fig. 15. PDP circuit vs. temperature changes

According to the designs provided so far, it can be concluded that with a good design, a compromise can be made between delay and power consumption, and the performance of the circuit can be brought to the optimal state.

3.2. The 4-bit RCA Full-Adder Simulation with The Proposed Design

RCA adder is made by serializing the full-adder blocks. Each full adder block is used to add two binary digits in each RCA class. The output carries a bit of each class and is directly connected to the input carry bit of the next class. This adder needs n elements of the adder to add two n-bit numbers. Fig. 16 shows an example of a four-bit RCA adder consisting of four full adders. Each bit A is added with a bit B that has the same position. Each addition operation generates an addition bit and an output carry bit. The output carry bit is transferred to the input carry bit of the higher class adder. The final result of a four-bit adder includes a four-bit adder number and an output carry bit.

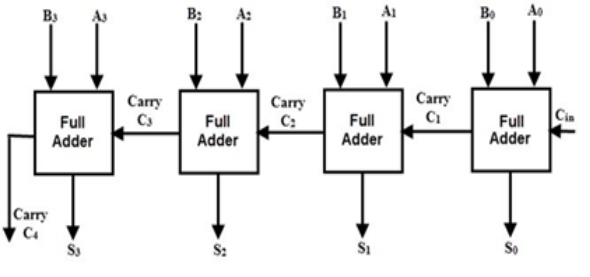

Fig. 16. RCA four-bit adder.

The proposed design is used as the blocks inside its structure in the simulation of the four-bit RCA adder. The transient response diagram and the analysis of the simulated circuit parameters are shown below.

Fig. 17 shows the transient response diagram of the four-bit RCA adder configured with all the proposed adders.

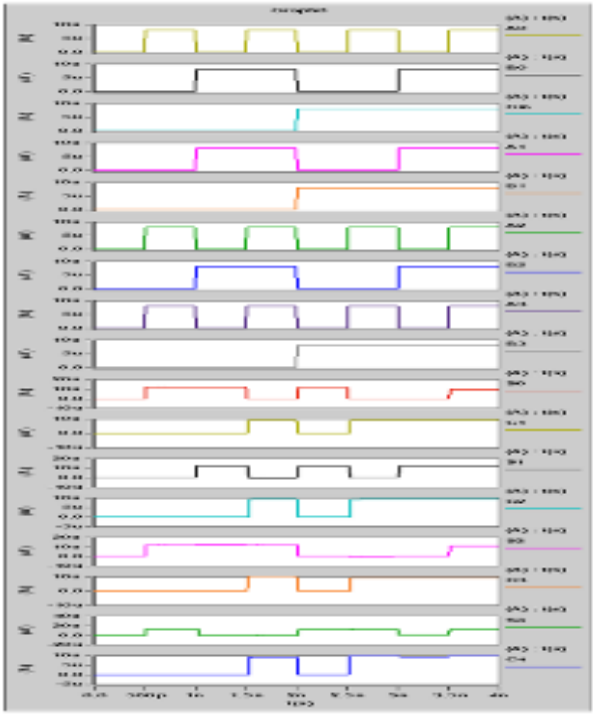

Fig. 17. The transient response diagram of the four-bit RCA adder configure with all proposed adders.

The four-bit RCA adder circuit has been simulated at a temperature of 27°, a frequency of 1 GHz, and a supply voltage of 0.9 V. According to the diagram, the four-bit circuit has stable performance, has a good FANOUT, and its outputs have full swing.

3.3. Comparison of the Performance of the Proposed RCA Circuits with the Previous Designs

The full adder design using ULPD [9] has improved well compared to previous designs in terms of delay, power consumption, and PDP. For this purpose, the proposed circuits of this thesis have been measured with the four-bit RCA adder circuit mentioned design to provide a comparison. The results can be seen in Table (7).

Table 7. Comparing the performance of the proposed design with other designs.

Full adder	Delay ($\times 10^{-11}$ s)	Power($\times 10^{-9}$ W)	PDP($\times 10^{-16}$ J)
New design 2	6.1254	6.9699	42.693
Ref. 9 ULPD (2021)	8.305	10.33	85.790

The delay parameter in the proposed circuit has improved by 26% compared to the ULPD design. The power consumption parameter in the proposed circuit has improved by 33% compared to the ULPD design. Finally, the PDP of the proposed circuit has improved by 50% compared to the ULPD design.

All proposed four-bit RCA adders have been simulated in different temperature ranges (0- 100°C). The PDP results can be seen in the diagram of Fig. 18.

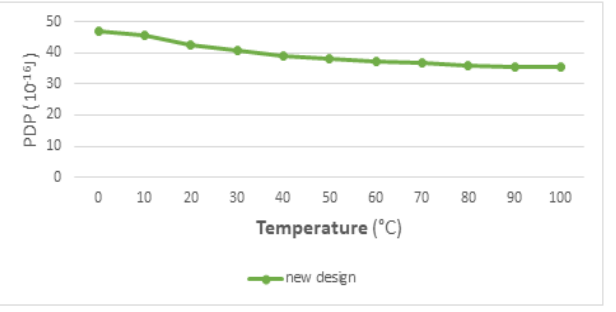

Fig. 18. PDP of the proposed circuits vs. temperature changes.

With increasing temperature, the PDP of the proposed circuit is decreasing, and this shows that the circuit has a good performance against temperature changes.

4. CONCLUSION

It is possible to reach better performance in VLSI circuits using new technologies such as CNTFET, good implementation methods, and suitable techniques. Unfortunately, the insistence on using voltage techniques in signal processing and circuit design has made it impossible to take full advantage of advanced technologies such as HBT, HEMT, GaAs, and MESFET (high speed and bandwidth). In the few actions that have been carried out to use the mentioned circuits in flow mode, the speed has been increased for more than a decade under similar conditions. On the other hand, capacitors, and resistors are considered destructive elements in the design of circuits that reduce the efficiency in power consumption, delay, the product of the two values, and in general, all the circuit parameters. Therefore, it is better not to use these two elements in the designs as much as possible.

Data Availability. Data underlying the results presented in this paper are available from the corresponding author upon reasonable request.

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Ethics. The authors declare that the present research work has fulfilled all relevant ethical guidelines required by COPE.

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