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Design of Binary-to-Quaternary Converters based on CNTFET Transistors

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ABSTRACT:
In order to connect two binary and quaternary systems, it is necessary to use binary-to-quaternary (B2Q) and quaternary-to-binary (Q2B) converters. These converters convert numbers from logic 2 to 4 and vice versa. In this paper, we designed a new binary-to-quaternary converter circuit using CNT transistors. In this circuit, the Power Delay Product (PDP) has been reduced to14.59% and 15.39% compared to best previous works. Also, this circuit has better driving ability and temperature stability than best previous works. The simulation results using Stanford's 32 nm CNTFET model in HSPICE software are at a voltage of 0.9 V.

KEYWORDS: CNTFET, Multi-Level Circuit, B2Q Converter, Mixed Radix System.

1. INTRODUCTION

The capabilities of integrated circuits and the rapid growth of technology have extended their application in modern life. Reducing dimensions and high speed in all equipment, including the design of microprocessor systems, is very essential. Therefore, researchers in this field are trying to provide new designs to increase the efficiency of such circuits [1].

Recently, nano-scale CMOS transistors have faced some design and manufacturing challenges, such as increased leakage current, reduced gate control, and large parametric variations [2]. To overcome the problems of CMOS transistors in the nanometer range, CNTFETs can be another option to reduce the size of transistors as well as develop new structures [3].

CNTFET is the best alternative to MOSFET-based circuits because it is most similar to MOSFET [3]. In the design of integrated logic circuits, multi-level circuits based on CNTFET are very popular due to their multiple threshold voltages. By tuning the required diameter of the CNTFET nanotubes, multiple threshold voltages can be provided.

Multi-level circuits based on CNTFET are quaternary and ternary circuits.

Any multi-level (quaternary) system can transfer more information than the binary system, which reduces the number of connections inside the chip.

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In quaternary circuits, the speed of information transmission increases dramatically. Therefore, in these circuits, power loss, especially static power consumption, as well as leakage, is significantly reduced [4-5].

A combination of binary and multi-level logic (MRS) is better than using only multi-level or binary logic [21]. Due to the simpler processing on binary basis, first, the numbers are taken from multi-level logic to binary logic using multi-level-to-binary converters, processed in binary logic, and then returned to multi-level logic by binary-to-multi-level converters. Therefore, the design of binary-to-multi-level converters is very important in these circuits.

In recent years, much research has been done on the multi-level logic circuits based on CNTFET: such as design of ternary logic circuits [6], multi-digit ternary to binary converter [7], quaternary full adder [8-10], ternary multiplexer [11], successors and predecessors [12], ternary adders [13-14] and ternary counter and flip-flop [15] and multi-valued logic comparator [16].

In this article, at first, a single-digit binary-to-quaternary converter based on CNTFET transistors is designed. Then the special design method and operation of this converter are described. Finally, the binary-to-quaternary converter is designed to be multi-digit. Also, this converter has been compared with the best previous works in this field [22] and [23]. In this structure, a diode connection is used. Normally, the desired voltages are produced at the output by resistive division. If the output resistance increases, the current decreases, so the power consumption decreases, and the delay increases. But by reducing the output resistance, the current and power consumption increases and the delay decreases. By using a diode connection in these circuits, a constant voltage drop can be created at the output, thus reducing the power delay product (PDP).

2. TERMINOLOGY

Carbon nanotubes are considered as sheets of graphite rolled in the form of cylinders with different diameters of several nanometers and lengths up to several micrometers [5]. CNTs are made in both single-walled (SWCNT) and multi-walled (MWCNT) forms [17-18]. The rolling direction is called the chirality vector. This vector defined by a pair (n, m) is called a chiral number. In the following equation, the diameter relationship based on the chirality coefficient for single-walled carbon nanotubes is given [19]:

$$D_{CNT} = \frac{a_0\sqrt{3}}{\pi}\sqrt{n^2 + m^2 + nm} \qquad (1)$$

Where, $a_0 = 0.142\ nm$ represents the atomic distance between each carbon and its adjacent atoms. The relations between chirality and CNT diameter are shown in Table 1.

Table 1. The relations between chirality and CNT diameter.

(n, m)	Diameter CNTs
(10, 0)	0.783nm
(19, 0)	1.487nm
(29, 0)	2.27nm

The minimum voltage required to turn on a transistor is called the threshold voltage. The voltage of the carbon nanotube transistor can be calculated by the following formula. [19]:

$$V_{th} \cong \frac{E_{bg}}{2e} = \frac{\sqrt{3}aV_{\pi}}{3eD_{CNT}} \cong \frac{0.436}{D_{CNT}(nm)} \qquad (2)$$

Here, a=2.49 Å, is the distance between the carbon atoms, Vπ = 3.033 eV is the carbon π-π bond energy of the tightly coupled model, e is the unit electron charge, and DCNT is the diameter of the CNT [19].

Carbon nanotubes are generally P-type parts. These parts are similar to Schottky barrier transistors in performance. If a negative voltage is applied to the gate, holes are electrostatically generated in the channel and the CNT becomes conductive. The electrical conductivity of the nanotube increases as the negative gate voltage increases, which is due to the increase in the number of holes injected into the CNT. Of course, this conductivity is limited to a certain level due to dams, this is what the holes encounter on their way. If the polarity is positive, it will empty the holes and reduce the conductivity [24].

To create a carbon nanotube field-effect transistor that acts as a MOSFET, the source and drain regions at both ends of the carbon nanotube must be heavily doped. This method of manufacturing MOSFET transistors results in a high accumulation of charge carriers in the source/drain region. The operation of the transistor due to the presence of an electric field around the gate causes the formation of a Schottky barrier at the points where the source and drain

terminals are connected to the nanotube [24].

An example of a single-wall CNFET transistor with four identical nanotubes is shown in Fig. 1.

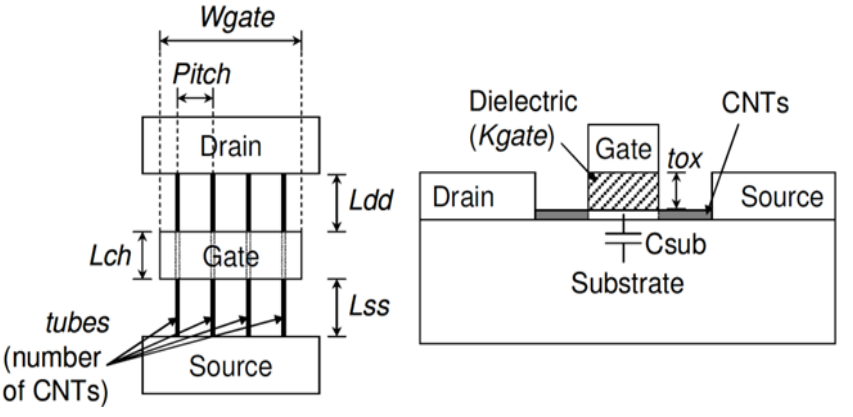

Fig. 1. Figure of CNTFET transistor [24].

A quaternary circuit is a type of multi-level circuit that contains four logic levels '0', '1', '2' and '3'. Table 2 shows the equivalent voltages of the four logical levels of quaternary circuits.

Table 2. Quaternary logic of its equivalent voltages.

Logic	Voltage
"0"	GND
"1"	VDD/3
"2"	2VDD/3
"3"	VDD

The basis of the quaternary logical operations can be defined as follows [20]:

$$x_i \text{ و } x_j \in \{1,2,3,4\} \quad (3)$$

$$x_i + xj = max\{x_i, x_j\} \quad (4)$$

$$x_i, xj = min\{x_i, x_j\} \quad (5)$$

$$\bar{x_i} = 3 - x_i \quad (6)$$

Operators "+", "." And "-" refer to OR, AND, and NOT in quaternary logic and logic gates have been accordingly designed. Quaternary NAND and NOR gates are two operators with multiple inputs used in quaternary circuits and are defined by the following two equations [7]:

$$\text{QNAND} = \overline{\text{Min(A and B)}} \quad (7)$$

$$\text{QNOR} = \overline{\text{Max(A and B)}} \quad (8)$$

3. THE PROPOSED CIRCUIT DESIGNS

MRS is combined with multi-valued and binary logic simultaneously. This structure is better than using only multi-value logic or using only binary logic [21]. Due to the simpler processing on binary basis, first, the numbers are taken from radix-R to radix-2 using R-to-2 converters, processed in radix-2, and then returned to radix-R by 2-to-R converters (Figure 2).

In this section, first, a new single-digit B2Q converter is introduced. This circuit is shown in Fig. 3.

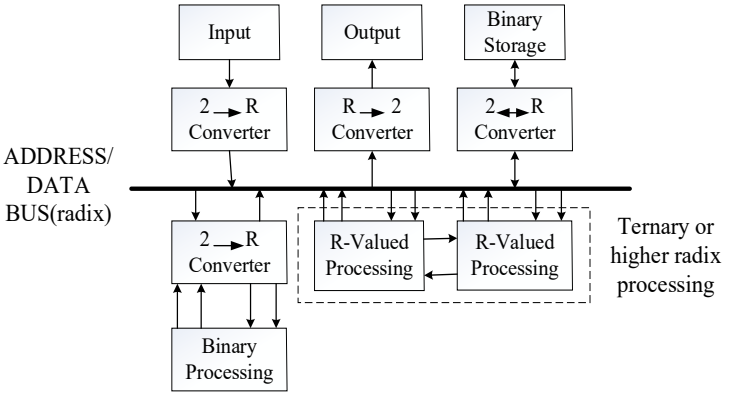

Fig. 2. Higher-radix data bus operating in bus structure systems with 2-R and R-2 converters [21].

3.1. Single-Digit B2Q Converter

A single-digit B2Q converter circuit converts two binary bits into one quaternary bit. Table 3 shows the operation of this circuit.

Table 3. B2Q truth value table

B1	B0	Q	Q(v)
'0'	'0'	'0'	0
'0'	'1'	'1'	VDD/3
'1'	'0'	'2'	2VDD/3
'1'	'1'	'3'	VDD

In this circuit, a diode connection is used. In normal mode, the desired voltages are produced at the output by resistive division. If the output resistance increases, the current decreases, so the power consumption decreases and the delay also increases. But by reducing the output resistance, the current and power consumption increases and the delay decreases. By using a diode connection in these circuits, a constant voltage drop can be created in the output, so the power delay product (PDP) is reduced.

In Table 4, we have described the working method of the proposed single-bit B2Q converter circuit.

When the input voltage is equal to GND; T2, T3, T10, T13, T14, and T15 are ON, and T1, T4, T5, T6, T7, T8, T9, T11, and T12 are OFF; so, the output node "Q" is connected to ground through T14 and T15 and becomes equal to GND or (logic '0').

When B0= '1' and B1= '0'; T1, T2, T6, T11, T12, T13, and T14 are ON, and T3, T4, T5, T7, T8, T9, T10 and T15 are OFF; Therefore, the output node "Q" becomes equal to VDD/3 or (logic '1') via a voltage division between T11, T12 and T13 on VDD.

When B0= '0' and B1= '1'; T1, T2, T6, T11, T12, T13, and T14 are OFF, and T3, T4, T5, T7, T8, T9, T10 and T15 are ON; Therefore, the output node "Q" becomes equal to 2VDD/3 or (logic '2') via a voltage division between T7, T8, T9 and T10 on VDD.

When the input voltage is raised to VDD; T1, T4, T5, T6, and T9 are ON, and T2, T3, T7, T8, T10, T11, T12, T13, T14, and T15 are OFF; the output node 'Q' is connected to VDD (logic '3').

3.2. Multi-Digit B2Q Converter

With the following simple algorithm, numbers can be converted from binary to quaternary logic and vice versa: If the binary number (X) has digits ($b_3b_2b_1b_0$) and (q_1q_0) are the digits of the same number in quaternary logic, to convert the number from binary to quaternary logic, its digits must be separated into two digits from the right side and put the quaternary equivalent of each of the two binary numbers:

$$(X)_2 = [(b_3b_2)\ (b_1b_0)]_2$$

$$(X)_4 = (\ q_1 \quad q_0\ )_4$$

To realize a multi-digit B2Q converter, single-digit B2Q converters can be used in parallel (figure 4).

Table 4. B2Q circuit performance.

case	Inputs		Transistors															Q
	B0	B1	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	13	T14	T15	
1	‘0’	‘0’	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	‘0’
2	‘1’	‘0’	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	‘1’
3	‘0’	‘1’	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	‘2’
4	‘1’	‘1’	ON	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	‘3’

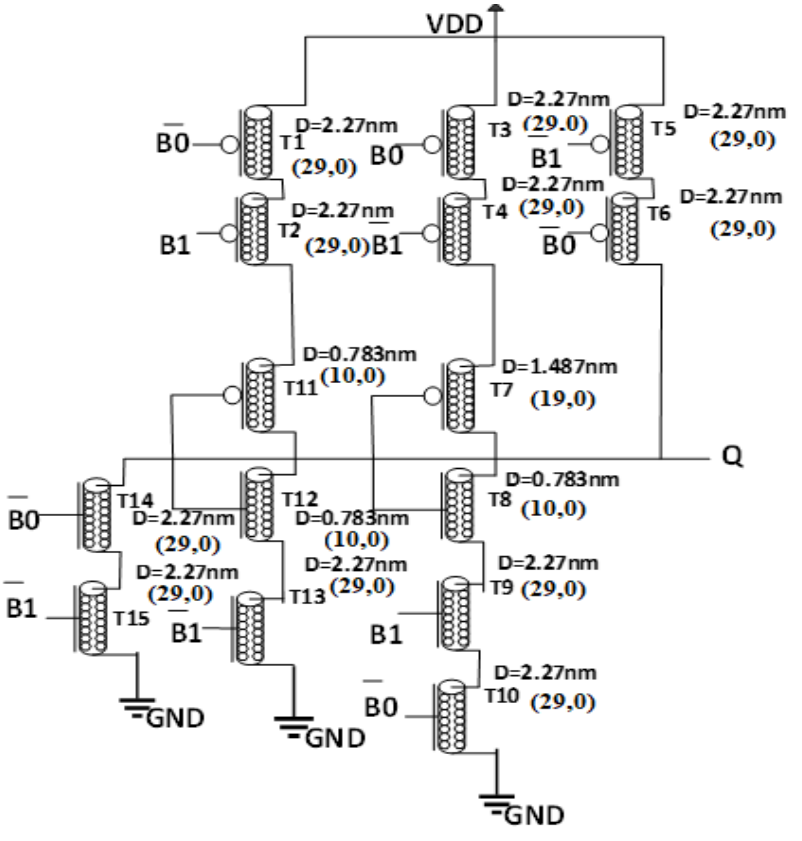

Fig. 3. The proposed B2Q converter circuit.

These converters can be designed for the desired higher number of bits.

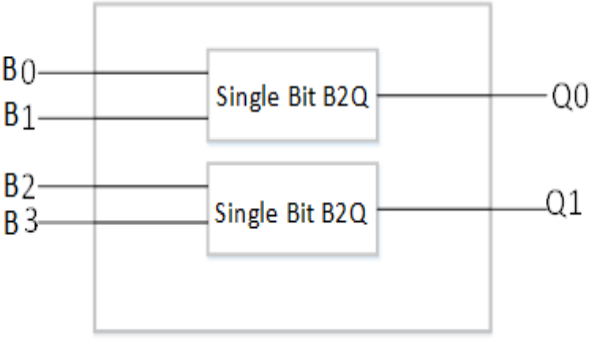

Fig. 4. The 2-bit B2Q converter circuit.

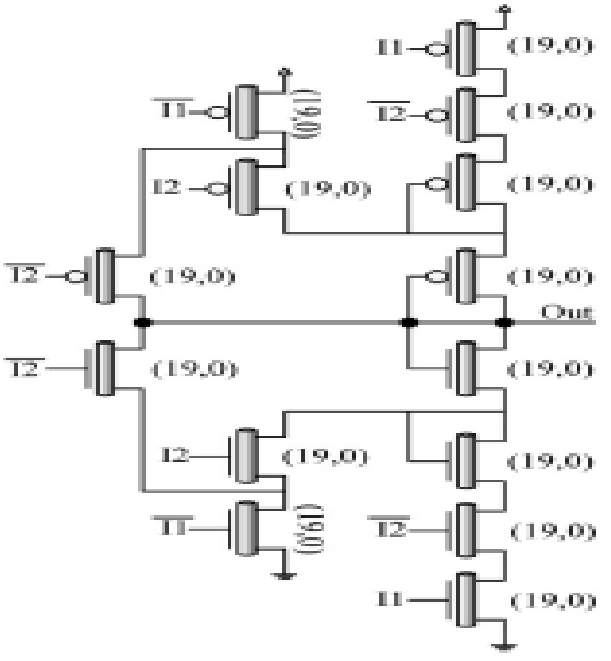

Fig. 5. The single-bit B2Q converter circuit [22].

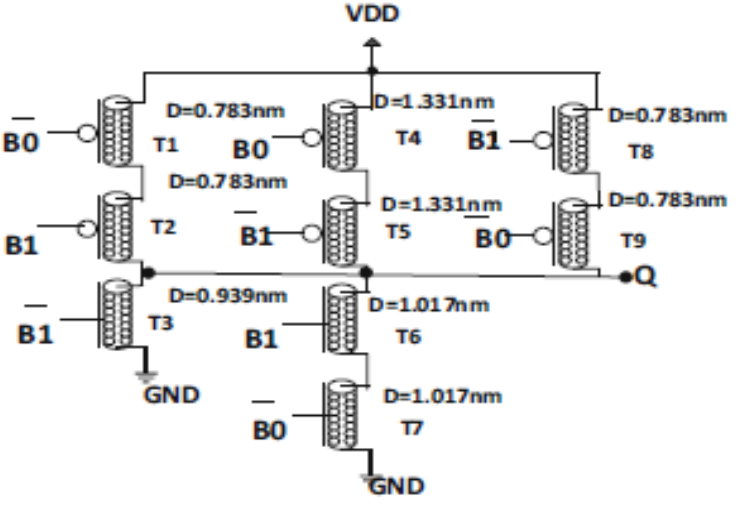

Fig. 6. The single-bit B2Q converter circuit [23].

4. SIMULATION RESULTS

The presented design is simulated by HSPICE software using the Stanford 32 nm CNTFET [25] and compared to other work already done in the field (Fig.5 and Fig. 6). The input waveform of the proposed single-bit B2Q converter, which is a two-level waveform, and its output waveform, which is a four-level waveform, are shown in Fig. 7. The waveforms represent the proper functioning of these circuits.

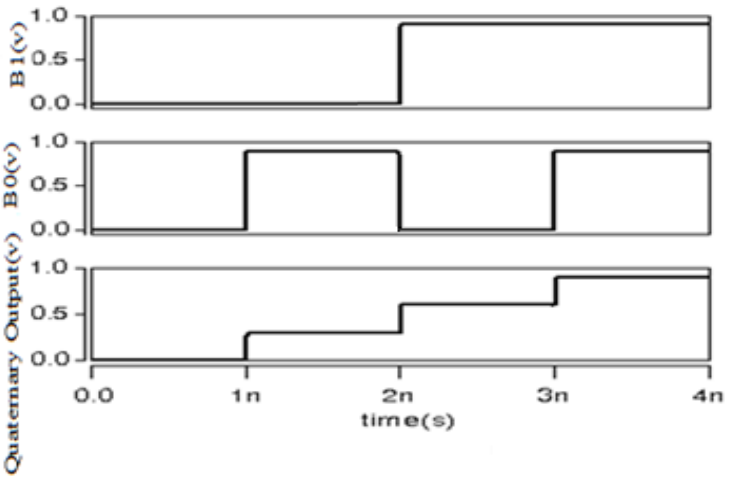

Fig. 7. The proposed B2Q converter circuit.

The results of the simulation of the proposed single-bit B2Q converter and previous works (Fig. 5 and Fig. 6) are compared in Table 5. As can be seen, the proposed single-bit B2Q converter has less delay and PDP in comparison to Ref [22] and Ref [23].

In the two-bit circuit, the effect of reducing delay and PDP is more obvious.

Table 5. PDP values of various studied B2Q converter circuits.

Design	The number of bits	Power ($\times 10^{-7}$W)	Delay ($\times 10^{-12}$s)	(PDP) ($\times 10^{-19}$J)
Proposed	Single-bit	7.83	2.4	18.792
Ref [22]		8.68	2.56	22
Ref[23]		4.83	4.6	22.21
Proposed	Two-bit	15.5	4.9	75.95
Ref [22]		16.5	5.11	84.315
Ref[23]		9.74	9.32	90.77

Driving ability is one of the most important parameters in digital circuits. The proposed circuit is tested under 0.5fF, 1fF, and 1.5fF loads. The results in Fig. 8 show that the proposed single-bit B2Q converter has better driving ability than Ref [22] and Ref [23].

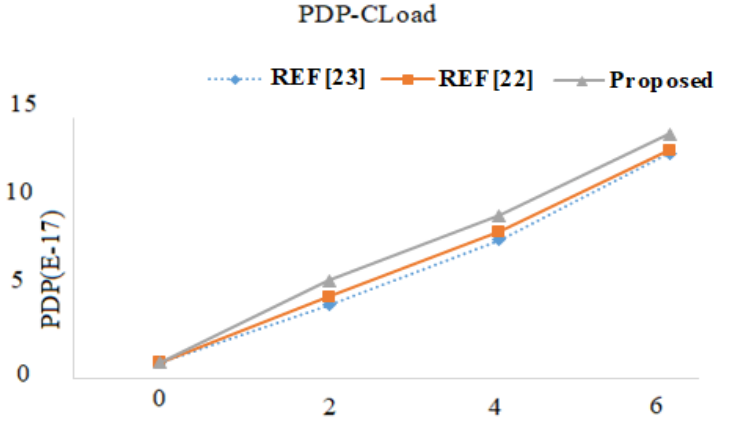

Fig. 8. Performance of the proposed single-bit B2Q converter against load capacitor variations.

Another important feature that should be considered in the design of circuits is their insensitivity to changes in ambient temperature. The temperature stability of the proposed single-bit B2Q is investigated in the range of 10°C to 100°C. Fig. 9 shows that the proposed single-bit B2Q circuit has better stability to temperature changes compared to Ref [22] and Ref [23].

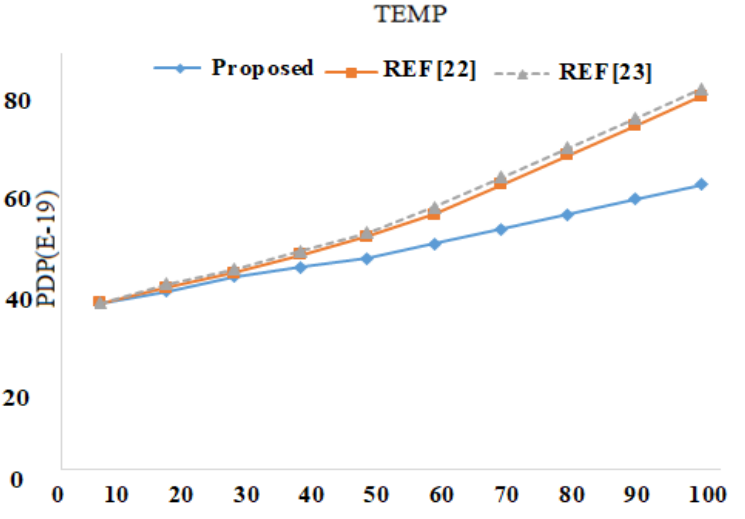

Fig. 9. Evaluation of PDP as a function of temperature in the studied single-bit B2Q converter circuits.

5. CONCLUSION

In nanotechnology, CNTFET is a suitable alternative to MOSFET [26]. Multi-level logic can reduce metal connections, chip area, and power dissipation on connections [27-29]. The structure of the MRS is a combination of multi-level and binary logic. This structure is much more suitable than a system based solely on multi-level or binary logic [23]. Multi-digit converters are needed in this structure. In this article, first, a single-bit B2Q converter circuit has been designed. Then a multi-bit B2Q converter circuit was presented. The proposed B2Q converter has less delay and PDP in comparison to Ref [22] and Ref [23]. Also, this proposed circuit has better driving ability and temperature stability than Ref [22] and Ref [23]. It turns out that multi-bit converters can be used to reduce bus interconnects and nanotechnology parallel data transfers.

Data Availability. Data underlying the results presented in this paper are available from the corresponding author upon reasonable request.

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Conflicts of interest. The authors declare no conflict of interest.

Ethics. The authors declare that the present research work has fulfilled all relevant ethical guidelines required by COPE.

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