A Low Complexity Multi-Valued Logic Successor and Predecessor in Nanoelectronics

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ABSTRACT:
Extremely efficient successor and predecessor circuits are suggested in this article using 4 CNTFETs. They have much fewer interconnections and complexity compared to the best previous circuits. The proposed circuits are designed by combining digital and analog techniques for the first time. They can be expanded for all MVLs like ternary, quaternary, pentaternary, and so on. The proposed designs for quaternary logic reduce the transistor count from 25 to 4 in comparison with the best previous works. Interestingly, in MVLs with more level logic, this difference will increase dramatically. This advantage leads to low complexity and costs. The accurate operation and great performance of introduced circuits are illustrated and their superiority is proved. Additionally, a quaternary half-adder is founded on the presented successor and predecessor. The simulation results, which are acquired by comprehensive simulations utilizing Synopsys HSPICE and the 32 nm plenary CNTFET model of Stanford, show that the proposed successor and predecessor circuits with only four transistors work accurately. According to these outcomes, in the proposed half-adder, not only was the transistor count reduced by 32%, but also it had 40% better PDP and 42.05% better EDP in comparison with the best previous work. Also, it is more stable against process variation and robust in a wide range of temperature variations.

KEYWORDS: Multi-valued logic, carbon nanotube FET, nanotechnology, successor/predecessor circuits.

1. INTRODUCTION

Large number of interconnections is a severe obstacle for binary circuits by increasing power consumption and chip area [1-4]. Multi-Valued Logic (MVL) is a feasible solution that decreases interconnections. In this manner, more data could be transferred on a line, more than one bit could be stored in each memory cell, and blocks have more processing ability. So, the amount of interconnections declines, and memory capacity enhances. In current technologies, reducing transistors' size encounters serious barriers like gate tunneling, quantum effects, increased leakage currents, high lithography costs, and so on, which convinced scientists to replace Complementary Metal Oxide Semiconductor transistor (CMOS) with a brand new technology. Carbon Nanotube Field-Effect Transistors (CNTFET) can be a proper substitute for (CMOS) circuits owing to their great performance and low power consumption [5-6].

The diameter of nanotubes in CNTFETs can control their threshold voltage, which is a precious advantage in MVL circuits, that leads to simple MVL designs [6–8]. It is noteworthy that, many researchers have been studying MVL circuits, developing ternary and multi-valued logic gates [9-11], ternary counters and flip-flops [12], quaternary full adders and logic gates [13-14], quaternary flip-flops [15], ternary logic gates [10] and full adders[16], multi-digit

ternary-to-binary [17] and quaternary-to-binary converters [18], quaternary logic functions [19], ternary memory cells [30-31].

To achieve MVL's purpose, these circuits should be low complex as much as possible to show their superiority over binary circuits. The successor and predecessor are significant circuits in MVL, which are used in half-adders, full-adders [13], flip-flops, and counters [12]. In this paper, innovative MVL successor and predecessor are designed with only four transistors. This successor and predecessor can be expanded for binary, ternary, quaternary, and so forth logics. In this study, the number of transistors for quaternary logic has been reduced drastically via analog design so needs only four transistors compared to the 25 transistors needed in one of the best former works [13]. It is noteworthy, that by increasing the level of logic (ternary, quaternary, pentaternary, and …), the difference between the numbers of transistors in the proposed idea compared to former works increases. The proposed successor and predecessor are used to design quaternary half-adder, and its performance will be shown by Synopsys HSPICE and the 32 nm CNTFET model of Stanford [20].

2. TERMINOLOGY

CNTFET is a brand-new generation of transistors made of carbon with a nano-cylindrical structure. These transistors are made by a graphene tab which is rolled into a cylindrical structure. The rolling's direction represents the chirality vector [21-22]. They can be divided in two groups, single-walled carbon nano-tube (SWCNT) and multi-walled carbon nano-tube (MWCNT) [20], [23]. It is notable that, a CNT can show both metallic and semiconducting characteristics according to its chiral vector [20], [23]. The chiral vector is represented by an integer pair (n, m). If n = m or n – m = 3i, where i is an integer, its behavior looks like a metal; unless it acts like a semiconductor. The most important superiorities of this technology are low power consumption, high speed, controllable threshold voltage, etc. The diameter of a CNT can control its threshold voltage. The equation (1) presents CNT's diameter in terms of (n, m) [24]:

$$D_{cnt} = \frac{\sqrt{3a_0}}{\pi} \sqrt{n^2 + m^2 + nm} \cong 0.0783 \sqrt{n^2 + m^2 + nm} \qquad (1)$$

Where $a_0 = 0.142$ *nm* represents the atomic distance between carbon atoms.
The proportion of CNT's diameter to the threshold voltage (V_{th}) is shown in (2) [25]:

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{cnt}} \approx \frac{0.436}{D_{cnt}\,(nm)} \qquad (2)$$

E_g shows the bandgap energy, $V_\pi \approx 3.033$eV demonstrates the carbon π–π bond energy in the tight-binding model, $a = 2.49$Å represents the carbon-to-carbon atomic distance, D_{CNT} shows the CNT's diameter and e expresses the charge of the unit electron.

MVL's levels are more than two ordinary '0' and '1' levels. Ternary logic has a significant third value more than binary logic. As described below, ternary levels are 0,1, and 2 that are relevant to 0, *Vdd/2*, and *Vdd*. Similarly, quaternary logic levels including 0, 1, 2 and 3 are related to 0, $V_{dd}/3$, $2V_{dd}/3$, and V_{dd}.

Equations (3-6) explain the basic operations on these logics [24]:

$$X_i, X_j \in \{0, 1, 2, 3, \ldots, n\} \qquad (3)$$
$$X_i + X_j = max\{X_i, X_j\} \qquad (4)$$
$$X_i . X_j = min\{X_i, X_j\} \qquad (5)$$
$$\bar{X}_i = n - X_i \qquad (6)$$

(+), ($^-$), (.), and (−) show OR, NOT, AND, also (−) is the arithmetic subtraction.

Equations (7-10) indicate quaternary inverters, including Positive Quaternary Inverter (PQI), Negative Quaternary Inverter (NQI), Standard Quaternary Inverter (SQI) and Intermediate Quaternary Inverter (IQI). Also they are shown in Table.1 [13].

$$NQI = \begin{cases} 3 \ if \ IN = 0 \\ 0 \ if \ IN \neq 0 \end{cases} \qquad (7)$$
$$IQI = \begin{cases} 3 \ if \ IN = 0 \ or \ 1 \\ 0 \ if \ IN \neq 2 \ ro \ 3 \end{cases} \qquad (8)$$

$$PQI = \begin{cases} 3 \; if \; IN = 3 \\ 0 \; if \; IN \; \neq 3 \end{cases} \tag{9}$$

$$SQI = 3 - IN \tag{10}$$

Table 1. The quaternary inverters' truth table.

Input	Output			
	PQI	NQI	SQI	IQI
0	3	3	3	3
1	3	0	2	3
2	3	0	1	0
3	0	0	0	0

Special forms of the cycle operators have been developed and nominated as successor and predecessor. The next level and previous level of the input level are produced by the successor and predecessor respectively. Also, their operations are described by equation (11), where p is a radix [26]. The other unary function is utilized in this article according to equation (12) [13].

$$x^k = (x + k) \; mod \, p \tag{11}$$

$$X_k = \begin{cases} 3 & X = K \\ 0 & X \neq K \end{cases} \tag{12}$$

Table 2 demonstrates the cycle operators' truth table.

Table 2. The truth table of quaternary successor and predecessor.

Input	Output					
X	Successor X^1	Predecessor X^2	X_0	X_1	X_2	X_3
0	1	3	3	0	0	0
1	2	0	0	3	0	0
2	3	1	0	0	3	0
3	0	2	0	0	0	3

3. PROPOSED DESIGN

An innovative successor by combining analog and digital techniques is introduced according to Fig. 1.

(a)   (b)
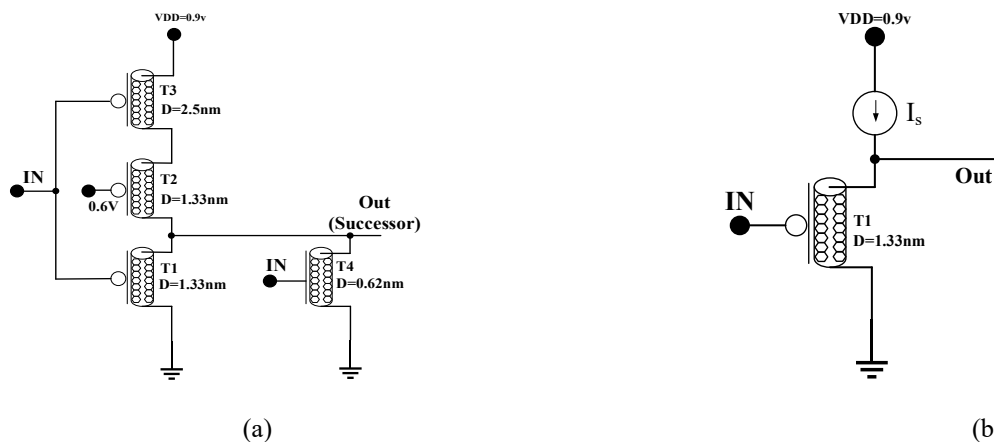
Fig. 1. (a)Proposed MVL successor (the nanotubes' diameters have been designed for quaternary special case) (b)level shifter.

The main core of the proposed successor which is made by a common drain amplifier as an analogue voltage level shifter is shown in Fig. 1(b) [27]. The current source supplies the current of T1, as T1 is in the saturation mode so its output voltage is according to equation (13):

$$V_o = V_{in} + V_{SG_{T1}} \qquad (13)$$

The $V_{SG_{T1}}$ is the certain amount that is added to the input voltage by which our successor's idea is developed.

The $V_{SG_{T1}}$ depends on transistor's threshold voltage (v_{th}) and the amount of current (I) of the current source according to equations (14). Equation (14) is for MOSFET [27].

$$I_D = \frac{1}{2}\mu_p c_{ox}\left(\frac{W}{L}\right)(v_{SG} - |v_{thp}|)^2 \quad \rightarrow \quad V_{SG} = \sqrt{\frac{2I_D}{\mu_p c_{ox}\left(\frac{W}{L}\right)}} + v_{thp} \qquad (14)$$

Where L is the gate length, W is the gate width, μ_p is the holes mobility, and c_{ox} is the gate oxide capacitance per unit area.

The equation for CNTFET is similar to MOSFET, but it is not the same. The equation for CNTFET is simplified here as a function of I_D and V_{th} according to (15):

$$V_{SG} = f(I_D, V_{th}) \qquad (15)$$

V_{SG} is controllable by adjusting I_D and V_{th} where v_{th} is adjustable by nanotube's diameter. In the proposed successor, we set the V_{GS} on the amount that output level is desired to increase compared to input level.

For instance, in quaternary logic with V_{DD}=0.9V, the circuit should shift up input signal to 0.3V so $V_{SG_{T3}}$ is set on 0.3V. This amount is 0.45V and 0.225V for ternary and pentaternary, respectively, in the same way. Generally, for M level logic, it is according to equation (16).

$$V_{SG_T} = \frac{V_{DD}}{M-1} \qquad (16)$$

Fig. 1(a) depicts the proposed successor whose parameters are designed for a special quaternary logic case; in this circuit, T2 plays the current source role. In the proposed successor, when input equals "0","1" or "2" T1, T2, and T3 are ON (level shifter is active), and T4 is OFF simultaneously. Note that T1, T2 are in saturation mode which are equivalent to the level shifter circuit, but T3 is in triode (linear) region so works as a switch.

Therefore, the output voltage is the input voltage shifted up for a certain amount specified by $V_{SG_{T1}} = 0.3V$. Additionally, when input is "3" T1, T2, and T3 are OFF (level shifter is inactive), and T4 is ON at the same time, so the output will be "0". This circuit is designed only with four transistors which is its most significant merit.

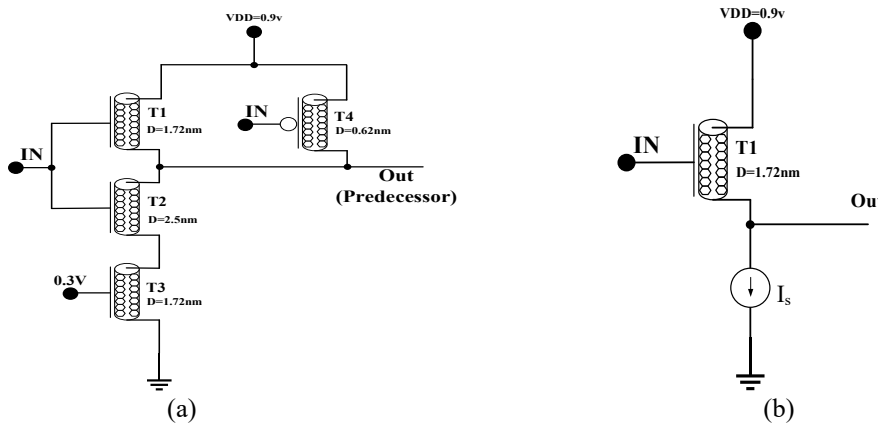The MVL predecessor is proposed in Fig. 2, which is designed by using analog and digital techniques.

(a)   (b)

Fig. 2. (a)Proposed predecessor(the nanotubes' diameters have been designed for special quaternary case) (b) level shifter.

Fig. 2(b) illustrates the main part of proposed predecessor made by an analog level shifter. The output voltage is by equation (17).

$$V_o = V_{in} - V_{Gs_{T1}} \qquad\qquad (17)$$

$$V_{GS} = f(I_D, V_{th}) \qquad\qquad (18)$$

The gate-source voltage of T1 is an essential parameter that relates to a threshold voltage (v_{th}) of the transistor and also the amount of current source, according to (18). Moreover, v_{th} varies by nanotube's diameter.

The proposed predecessor, whose parameters are designed for a quaternary logic special case, is presented in Fig. 2(a). The main core of this circuit is an analog-level shifter. In this design, T3 plays a current source role; the proposed predecessor's operation is described as below:

When input equals "3", "2" or "1", T1, T2, and T3 are ON (level shifter is active), and T4 is OFF. In these cases, the circuit shifts down the input value for a certain amount. This amount is specified by $V_{GS_{T1}}$. When the input is "0"; T1, T2, and T3 are OFF (level shifter is inactive). Also T4 is ON, so the output will be *0.9V* (logic 3). As explained before, this amount is *0.45V* and *0.225V* for ternary and pentaternary, respectively.

The proposed design is made only by four transistors which is its leading superiority. Additionally, this design can be expanded for all MVLs.

4. PROPOSED HALF-ADDER BASED ON INTRODUCED SUCCESSOR AND REDECESSOR

A quaternary half-adder is made up by proposed successor and predecessor in this section. First of all, we make A_0, A_1, A_2, and A_3 from input signal A by a unary function presented in equation (12) and Table1, using quaternary decoder depicted in Fig. 3 presented in [6].
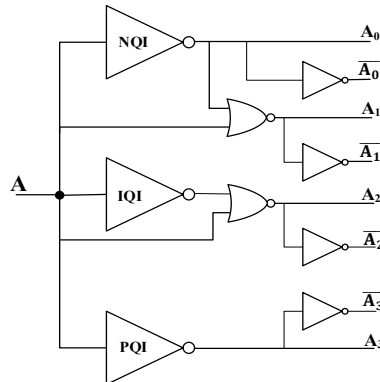

Fig. 3. Quaternary decoder [6].

Table 3, shows the operation of the sum for the suggested half-adder, which is obtained from quaternary half-adder's truth table [13]. It is described as below:

In case input $A=0$ ($A_0=3$, A_1, A_2, and A_3 are zero), the sum equals exactly B. When $A=1$ ($A_1=3$ and A_0, A_2, and A_3 are zero), the sum is the B^1. If $A=2$ ($A_2=3$ and A_0, A_1, and A_3 are zero), the sum will be B^2.

Finally, when $A=3$ ($A_3=3$ and A_0, A_1, and A_2 are zero), the sum equals B^3. Where B^1, B^2, and B^3 are outputs of the successor, double successor, and predecessor of input signal B, respectively.

Fig. 4(a) presents the proposed half-adder's sum circuit which is made up of a predecessor and two successors. In this circuit T1, T2, T7, and T8 make a predecessor, furthermore T9, T10, T15, T16, T17, T18, T23, and T24 make first and second successors, respectively. Additionally, T3, T4, T5, T6, T11, T12, T13, T14, T19, T20, T21, and T22 play transmission gates and pass transistors role by which predecessor or successors become active or inactive.

In case $A=0$ ($A_0=3$, A_1, A_2, and A_3 are zero); T4, T5, T20, and T21 are ON, and T3, T6, T11, T12, T13, T14, T19, and T22 are OFF simultaneously, so B goes out directly. The predecessor and both successors are inactive.

When $A=1$ ($A_1=3$ and A_0, A_2, and A_3 are zero); T11, T12, T13, T14, T20, and T21 are ON and T3, T4, T5, T6, T19, and T22 are OFF at the same time. As a result, B^1 pops out as the sum, which is the output of the successor made by T9, T10, T15, and T16. The predecessor and the second successor are inactive.

In case $A=2$ ($A_2=3$ and A_0, A_1, and A_3 are zero), T11, T12, T13, T14, T19, and T22 are ON also T3, T4, T5, T6, T20, and T21 are OFF. In this situation, two successors are active, but the predecessor is inactive. B^1 as the output of the first successor is used as the input of the second successor. B^2 is the output of the second successor (double successor).

Eventually when $A=3$ ($A_3=3$ and A_0, A_1, and A_2 are zero); T3, T6, T20, and T21 are ON, and T4, T5, T11, T12, T13, T14, T19, and T22 are OFF. In this status, only the predecessor made by T1, T2, T7, and T8 is active, and its output (B^3) goes out. It is notable that when each successor or predecessor is inactive, switches turn off, so power consumption is reduced. Fig. 4(b) depicts the carry generator circuit of the proposed half-adder. It is composed of quaternary inverters, including PQI, IQI, NQI, and four pass transistors.

When $A="0"$, T36 is ON, so carry is "0" and T27, T30, and T33 are OFF simultaneously. In case $A="1"$, PQI connects to IQI by T27, so carry is $\overline{PQI(B)}$, and T30, T33, and T36 are OFF. When $A="2"$ IQI connects to IQI via T30, so carry is $\overline{IQI(B)}$, and T27, T33, and T36 are OFF. If $A="3"$ NQI connects to IQI through T33, so carry is $\overline{NQI(B)}$, and T27, T30, T36 are OFF.

Fig. 4(c) shows the power supply distributing circuit. This circuit makes V1=0.6V and V2=0.3V from VDD=0.9V. As a result, the proposed half-adder uses only one power supply.

Table 3. The output (sum) of proposed Half-adder.

Input	Output (Sum)	Output (Carry)
A=0	B	0
A=1	B^1 (Successor of B)	$\overline{PQI(B)}$
A=2	B^2 (Double Successor of B)	$\overline{IQI(B)}$
A=3	B^3 (Predecessor of B)	$\overline{NQI(B)}$

(a)
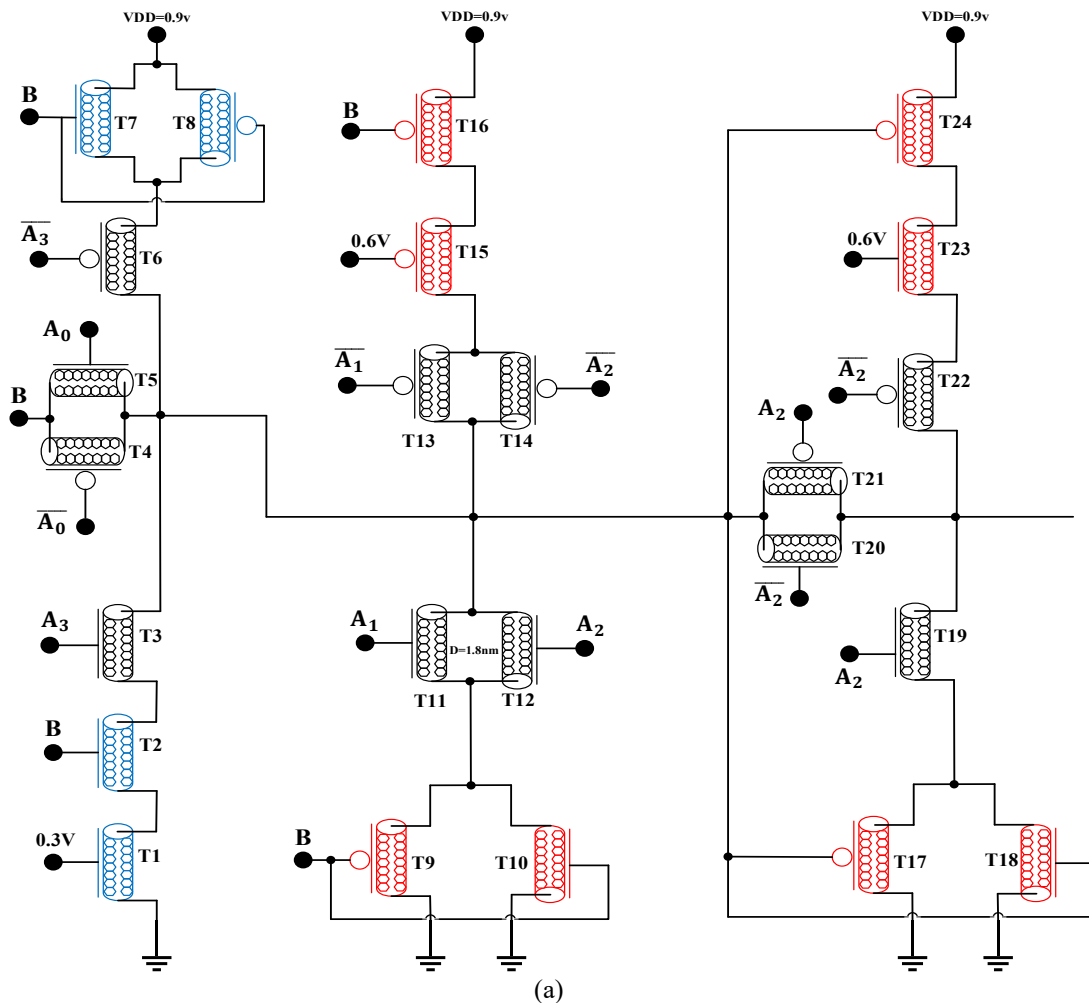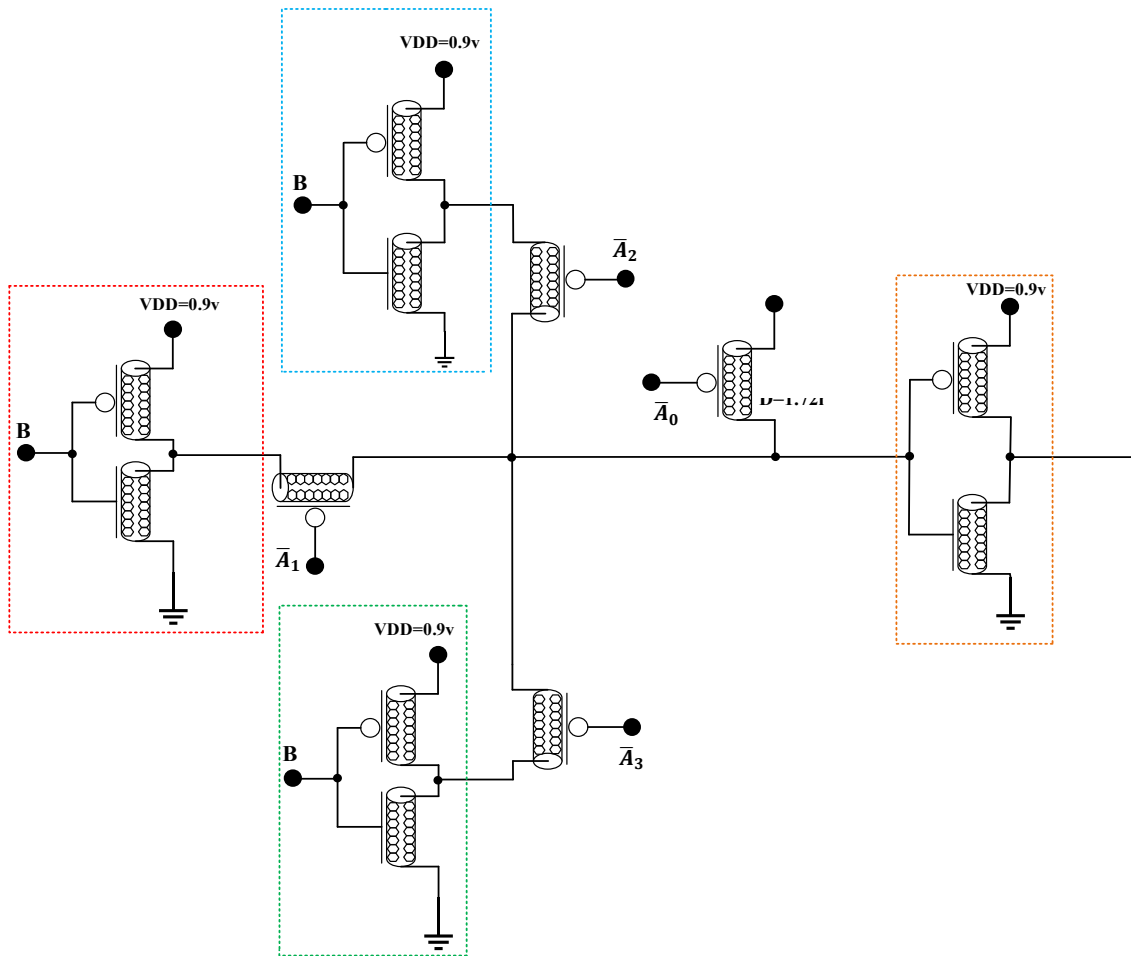
(b)
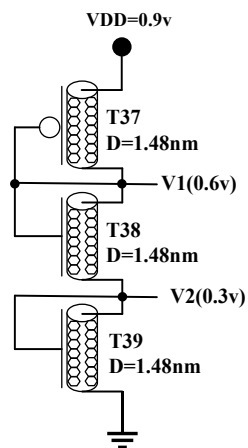
(c)

Fig. 4. Proposed half-adder, (a) sum circuit, blue-colored transistors make a predecessor, red-colored transistors make two successors, and black colored transistors are switches (b) carry circuit (c) power supply distributing circuit.

5. SIMULATION OUTCOMES AND COMPARISON

This part shows the simulation outcomes for introduced circuits which are obtained by Synopsys HSPICE using 32 nm CNTFET technology at 0.9 V CNTFET model of Stanford [20]. Additionally, the comparisons of the results with previous works are shown.

Fig. 5 shows the precise operations of the introduced successor and predecessor in quaternary special case for all possible input situations. Also, Fig. 6 demonstrates the introduced half-adder's accurate operation in the same conditions.
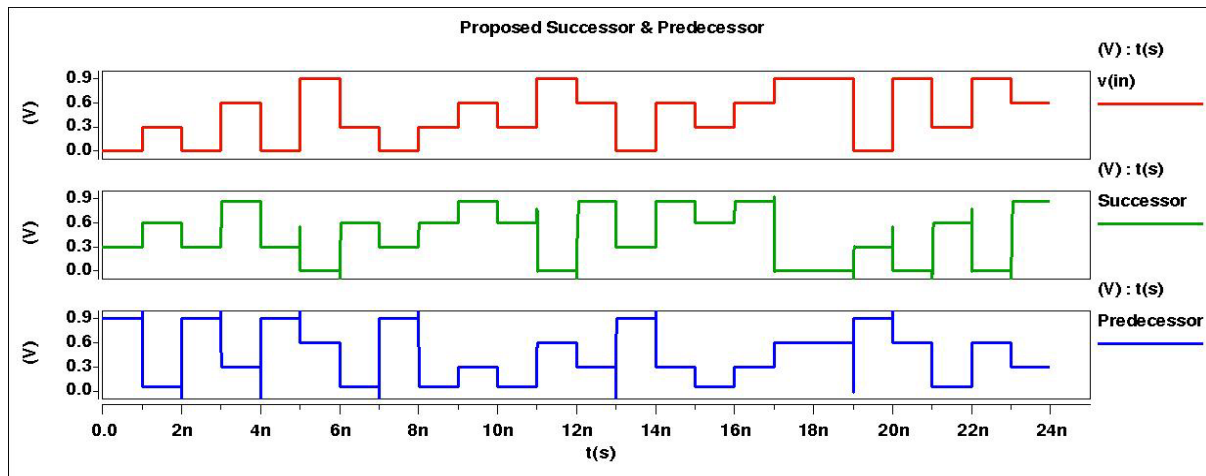

Fig. 5. The operation of the introduced successor and predecessor.
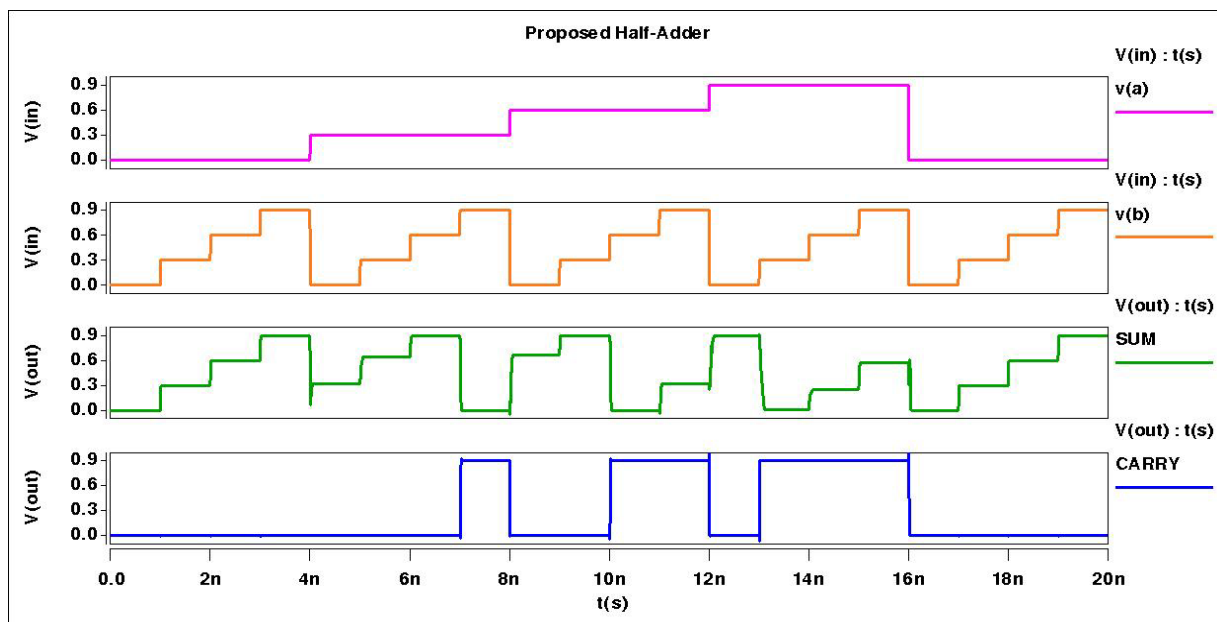
Fig. 6. The operation of the suggested half-adder.

In Tables 4 and 5, the transistor count, delay, power, PDP, and EDP for the proposed successor with different input frequencies (500MHz and 1GHz) and different loads (0fF, 0.5fF, 1fF, 1.5fF, and 2fF) are reported and compared with the successor of [13], respectively. It can be seen that the successor of [13] needs about 6 times more transistors compared to the proposed successor. It is crystal clear that more transistors lead to more complexity and more interconnections (more power consumption and more delay) which are in contrast with the MVL circuit's ambitions.

It is noteworthy that the difference between the number of required transistors for the proposed idea and previous works will increase for higher-level logics like pentaternary and so on. Additionally, the results were obtained only by transistors' simulation, so by considering interconnections, proposed circuits will have better power consumption and delay, which lead to better PDP.

Table 4. Parameter comparison and simulation outcomes of the suggested Successor and Successor of [13] in 500MHz frequency.

Load(fF)		Proposed Successor	Successor[13]
0	Power(µw)	1.3	0.34
	Delay(ps)	16.01	15.76
	PDP(10e-18 J)	20.88	5.41
	EDP(10e-28)	3.34	0.85
0.5	Power(µw)	1.32	0.42
	Delay(ps)	50.52	34.74
	PDP(10e-18 J)	66.89	14.77
	EDP(10e-28)	33.79	5.13
1	Power(µw)	1.33	0.5
	Delay(ps)	81.47	53.48
	PDP(10e-18 J)	109.16	27.18
	EDP(10e-28)	88.93	14.54
1.5	Power(µw)	1.35	0.58
	Delay(ps)	115.07	72.21
	PDP(10e-18 J)	156.31	42.51
	EDP(10e-28)	179.86	30.69
2	Power(µw)	1.37	0.67
	Delay(ps)	148.31	90.92
	PDP(10e-18 J)	203.53	61.07
	EDP(10e-28)	301.85	55.53
Transistor Count		4	25

Table 5. Parameter comparison and simulation outcomes for the introduced Successor and Successor of [13] in 1GHz frequency.

Load(fF)		Proposed Successor	Successor[13]
0	Power(µw)	1.3	0.42
	Delay(ps)	15.86	15.76
	PDP(10e-18 J)	20.75	6.77
	EDP(10e-28)	3.29	1.06
0.5	Power(µw)	1.34	0.58
	Delay(ps)	49.66	34.85
	PDP(10e-18 J)	66.71	20.42
	EDP(10e-28)	33.13	7.11
1	Power(µw)	1.37	0.75
	Delay(ps)	81.42	53.49
	PDP(10e-18 J)	112.15	40.37
	EDP(10e-28)	91.31	21.59
1.5	Power(µw)	1.41	0.92
	Delay(ps)	115.07	72.22
	PDP(10e-18 J)	162.57	67.14
	EDP(10e-28)	187.06	48.48
2	Power(µw)	1.43	1.09
	Delay(ps)	148.11	90.82
	PDP(10e-18 J)	213.24	99.76
	EDP(10e-28)	315.83	90.61
Transistor Count		4	25

Tables 6 and 7 show delay, the transistor count, power, PDP, and EDP for the proposed predecessor and the predecessor of [13] with different loads and different input frequencies, respectively. It is noteworthy that the predecessor of [13] needs approximately 5.7 times more transistors compared to the proposed predecessor. Also, the results have been obtained by simulating transistors which will be improved by including interconnection.

Table 6. Parameter comparison and simulation outcomes for the proposed Predecessor and Predecessor of [13] in 500MHz.

Load(fF)		Proposed predecessor	predecessor [13]
0	Power(μw)	1.86	0.35
	Delay(ps)	6.91	17.63
	PDP(10e-18 J)	12.93	6.17
	EDP(10e-28)	0.89	1.08
0.5	Power(μw)	1.91	0.44
	Delay(ps)	80.29	46.5
	PDP(10e-18 J)	153.87	20.63
	EDP(10e-28)	123.55	9.59
1	Power(μw)	1.96	0.52
	Delay(ps)	155.64	82.67
	PDP(10e-18 J)	305.97	43.63
	EDP(10e-28)	476.22	36.07
1.5	Power(μw)	2.01	0.61
	Delay(ps)	230.83	118.82
	PDP(10e-18 J)	465.1	73
	EDP(10e-28)	1073.6	86.73
2	Power(μw)	2.06	0.69
	Delay(ps)	306.33	154.96
	PDP(10e-18 J)	633.9	108.12
	EDP(10e-28)	1941.9	167.54
Transistor Count		4	23

Table 7. Parameter comparison and simulation outcomes for the proposed Predecessor and Predecessor of [13] in 1GHz.

Load(fF)		Proposed predecessor	predecessor [13]
0	Power(μw)	1.87	0.44
	Delay(ps)	6.91	17.61
	PDP(10e-18 J)	12.96	7.84
	EDP(10e-28)	0.89	1.38
0.5	Power(μw)	1.96	0.63
	Delay(ps)	80.29	46.5
	PDP(10e-18 J)	158.12	29.64
	EDP(10e-28)	126.96	13.78
1	Power(μw)	2.06	0.81
	Delay(ps)	155.64	82.67
	PDP(10e-18 J)	321.87	67.02
	EDP(10e-28)	500.96	55.4
1.5	Power(μw)	2.16	0.98
	Delay(ps)	230.83	118.82
	PDP(10e-18 J)	499.28	116.64
	EDP(10e-28)	1152.5	138.59
2	Power(μw)	2.25	1.15
	Delay(ps)	300	154.96
	PDP(10e-18 J)	675	178.29
	EDP(10e-28)	2025	276.27

Transistor Count		4	23

In Tables 8, transistor count, delay, power, PDP, and EDP for the suggested half-adder are compared with half-adders of [6], [28], and [29]. According to Table 8, proposed half-adder needs 32%, 34%, 43% less transistors in comparison with half-adder of [6], [28], [29] respectively. Table 8 shows that the proposed half adder's PDP is 40%, 87%, and 56% better than [6], [28], and [29], respectively. In the introduced half-adder, 22 transistors are used to produce A_0, $\overline{A_0}$, A_1, $\overline{A_1}$, A_2, $\overline{A_2}$, and A_3, $\overline{A_3}$ furthermore, 39 transistors make the proposed circuit according to Fig. 4. As a result, 61 transistors are used in total.

Table 8. Parameter comparison and simulation outcomes for the suggested Half-Adder and ones for [6], [28], and [29].

Load(fF)		Proposed HA	HA [6]	HA [28]	HA [29]
0	Power(μw)	1.1	1.75	11.2	5.88
	Delay(ps)	47.79	49.89	38.07	20.57
	PDP(10e-18 J)	52.98	87.6	426.4	121.01
	EDP(10e-28)	25.32	43.7	162.32	24.89
2	Power(μw)	1.3	1.9	11.6	5.96
	Delay(ps)	350.45	251.33	52.58	42.45
	PDP(10e-18 J)	458.6	479.55	610	253.1
	EDP(10e-28)	1607.2	1205.25	320.73	107.44
Transistor Count		61	89	92	106
Power Supply count		1	1	1	3

The diameter of a CNT can control its threshold voltage, which is a precious privilege of it. On the other hand, CNT is sensitive to process variation, so its efficiency and robustness can be affected. As a result, these circuits' performances are evaluated in regard to process variation. For analyzing these issues Monte Carlo simulations are utilized. Its parameters are $\pm 15\%$ Gaussian distributions and $\pm 3\sigma$ level variations. Fig. 7 compares the suggested half-adder' robustness with the ones introduced in [6], [28], and [29]. It is visible that the suggested design has more stability in process variation.
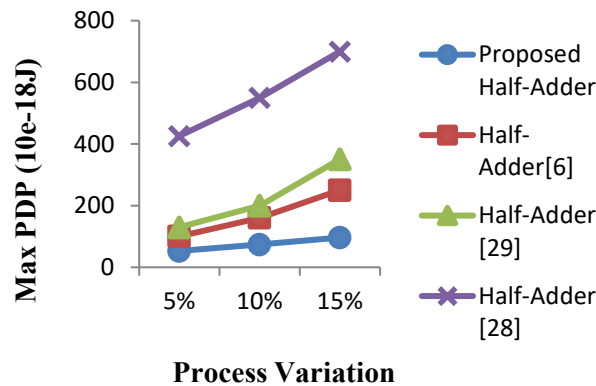

Process Variation

Fig. 7. PDP variation comparison for suggested Half-Adder and Half-Adder of [6],[28], and[29] with regard to process variation.

Fig. 8 compares PDP variations for the suggested Half-Adder with ones for [6], [28], and [29] in several different temperatures. The PDP of the proposed design is robust in a wide range of temperature variations.
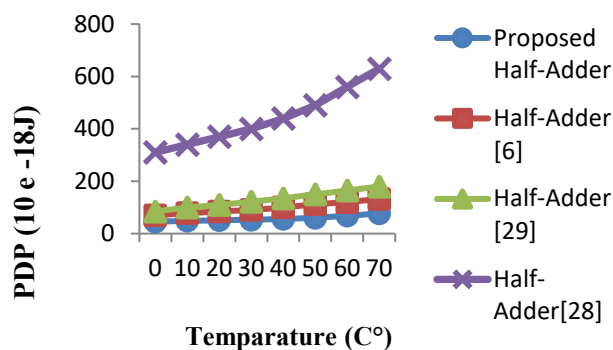
Fig. 8. PDP variation comparison for proposed Half-Adder and Half-Adder of [6],[28], and [29] in the presence of temperature variation,

6. CONCLUSION AND DISCUSSION

The unique specifications of nano-electronics encourage scientists to research MVL circuits. To achieve the superiority of MVL against binary logic, they should be designed with the lowest complexity as much as possible. In this paper, the multi-valued successor and predecessor by combining digital and analog techniques were designed for the first time. In these circuits, the transistor count was reduced from 25 to 4 for quaternary logic. As a result, the applied circuits such as half-adder, full-adder, counter, flip flop, and …, which are composed of successors and predecessors, require fewer transistors so complexity decreases. Therefore to achieve the MVL's advantages, the proposed successor and predecessor can be used in new designs in nano-electronics with lower complexity and chip area.

Conflicts of interest. The authors declare no conflict of interest.

Ethics. The authors declare that the present research work has fulfilled all relevant ethical guidelines required by COPE.

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